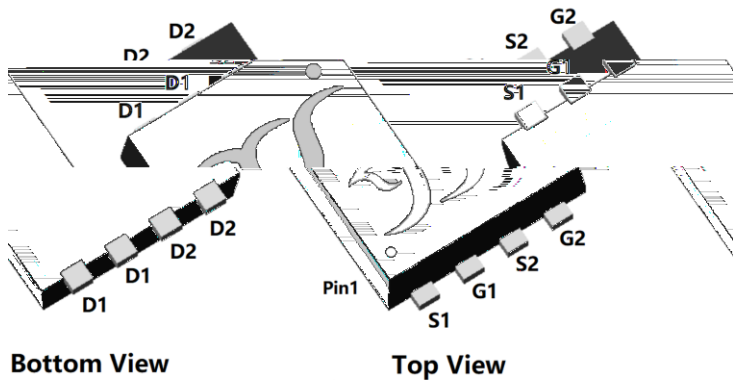
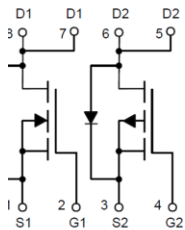


N-Channel and P-Channel Complementary MOSFET



Bottom View

Top View



PDFN3030-8L

Product Summary

NMOS

- V_{DS} 30V
- I_D 4A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <35m Ω
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <55m Ω

PMOS

- V_{DS} -30V
- I_D -3A
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) <75m Ω
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <110m Ω

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation

Applications

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	NMOS	PMOS	Unit
Drain-source Voltage		V_{DS}	30	-30	V
Gate-source Voltage		V_{GS}	± 20	± 20	V
Drain Current	$T_A=25$	I_D	4	-3	A
	$T_A=100$		2.5	-1.9	
Pulsed Drain Current ^A		I_{DM}	20	-20	A
Total Power Dissipation ^B	$T_A=25$	P_D	1.1	1.25	W
	$T_A=100$		0.45	0.5	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	-55~+150	

■ Thermal resistance

Parameter		Symbol	NMOS		PMOS		Units
			Typ	Max	Typ	Max	
Thermal Resistance Junction-to-Ambient ^C	Steady-State	$R_{\theta JA}$	90	110	80	100	$^\circ C/W$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJU3724A	/	Q3724A	3000	30000	120000	7" reel



YJU3724A

■ NMOS Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
		V _{DS} =30V, V _{GS} =0V, T _J =150°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =4A	-	26	35	mΩ
		V _{GS} =4.5V, I _D =3A	-	41	55	
Diode Forward Voltage	V _{SD}	I _S =4A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	2.5	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	4	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHz	-	230	-	pF
Output Capacitance	C _{oss}		-	45	-	
Reverse Transfer Capacitance	C _{rss}		-	35	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =4A	-	6	-	nC
Gate-Source Charge	Q _{gs}		-	1.4	-	
Gate-Drain Charge	Q _{gd}		-	1.2	-	
Reverse Recovery Charge	Q _{rr}	I _F =4A, di/dt=100A/us	-	1.0	-	nC
Reverse Recovery Time	t _{rr}		-	5.5	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =15V, I _D =4A R _{GEN} =3Ω	-	5	-	ns
Turn-on Rise Time	t _r		-	30	-	
Turn-off Delay Time	t _{D(off)}		-	8	-	
Turn-off fall Time	t _f		-	24	-	

■ PMOS Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V	-	-	-1	μA
		V _{DS} =-30V, V _{GS} =0V, T _J =150°C	-	-	-100	



YJU3724A

Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.5	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-3A$	-	58	75	m Ω
		$V_{GS}=-4.5V, I_D=-3A$	-	85	110	
Diode Forward Voltage	V_{SD}	$I_S=-3A, V_{GS}=0V$	-	-	-1.2	V
Gate resistance	R_G	$f=1MHz$	-	18	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	-3	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$	-	260	-	pF
Output Capacitance	C_{oss}		-	50	-	
Reverse Transfer Capacitance	C_{rss}		-	40	-	
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=-10V, V_{DS}=-15V, I_D=-3A$	-	7	-	nC
Gate-Source Charge	Q_{gs}		-	2	-	
Gate-Drain Charge	Q_{gd}		-	1	-	
Reverse Recovery Charge	Q_{rr}	$I_F=-3A, di/dt=100A/us$	-	4	-	nC
Reverse Recovery Time	t_{rr}		-	12	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=-10V, V_{DD}=-15V, I_D=-3A$ $R_{GEN}=3\Omega$	-	5	-	ns
Turn-on Rise Time	t_r		-	23	-	
Turn-off Delay Time	$t_{D(off)}$		-	21	-	
Turn-off fall Time	t_f		-	30	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. P_d is based on max. junction temperature, using junction-case thermal resistance.

C. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in the still air environment with $T_A=25$. The maximum allowed junction temperature of 150 . The value in any given application depends on the user's specific board design.



NMOS Typical Electrical and Thermal Characteristics Diagrams

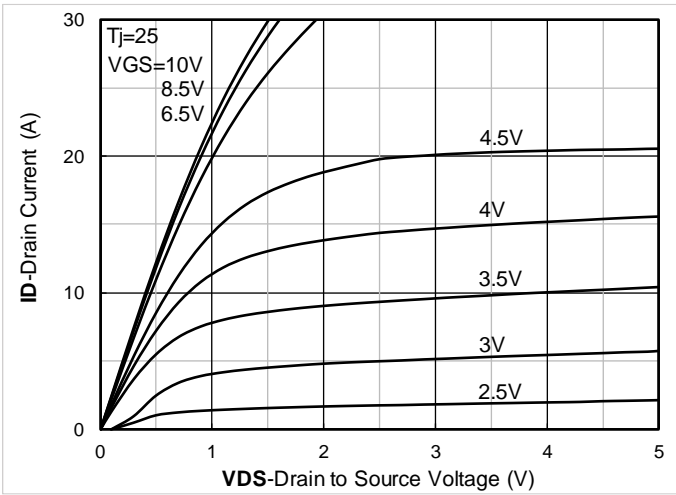


Figure 1. Output Characteristics

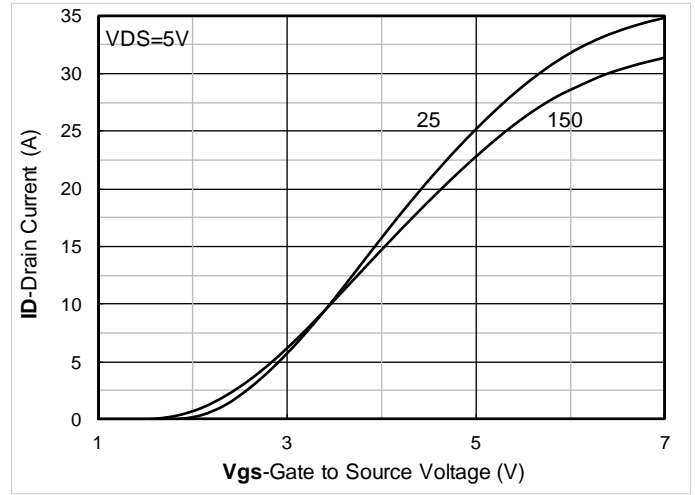


Figure 2. Transfer Characteristics

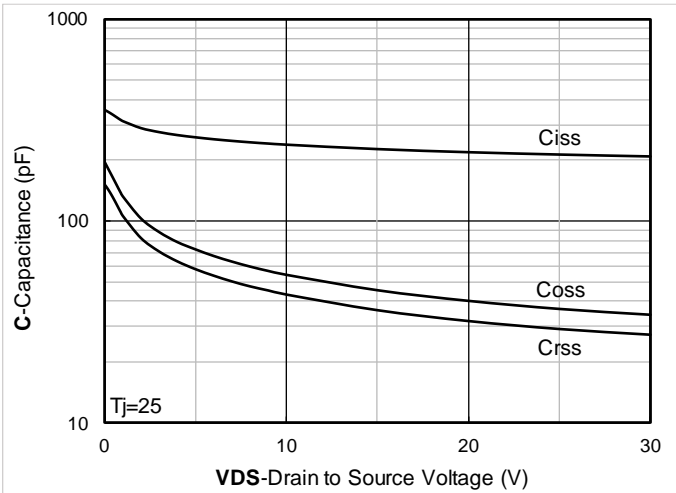


Figure 3. Capacitance Characteristics

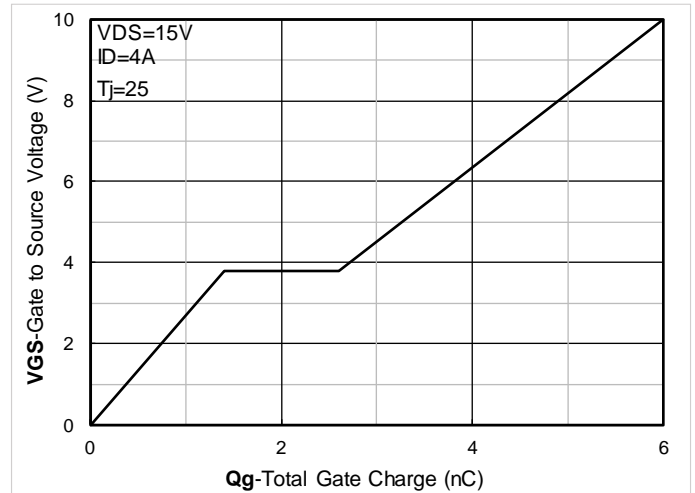


Figure 4. Gate Charge

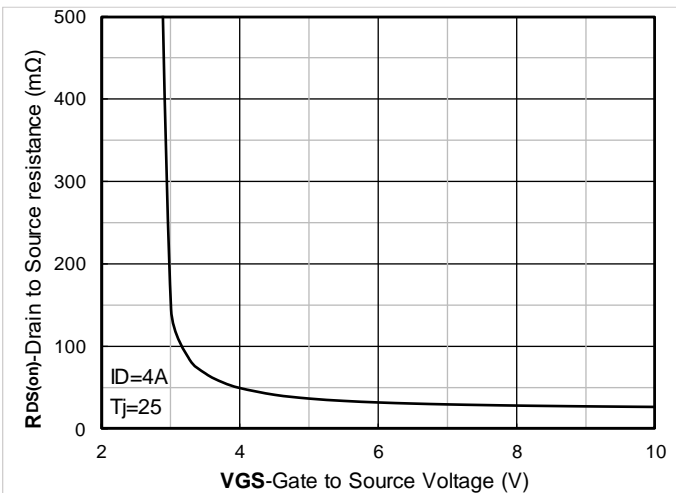


Figure 5. On-Resistance vs Gate to Source Voltage

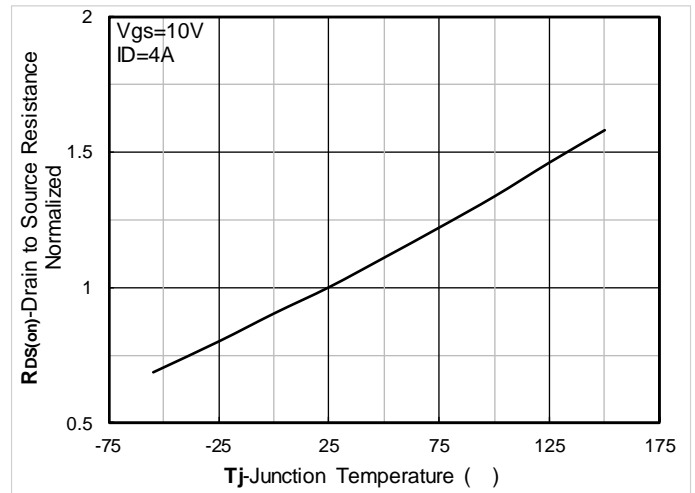


Figure 6. Normalized On-Resistance

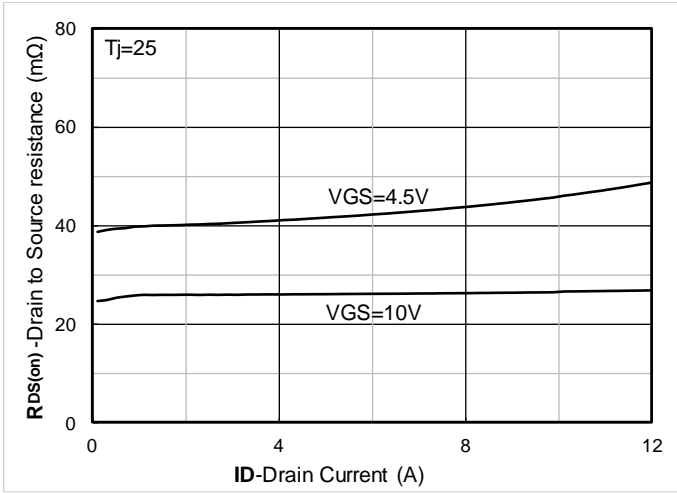


Figure 7. $R_{DS(on)}$ VS Drain Current

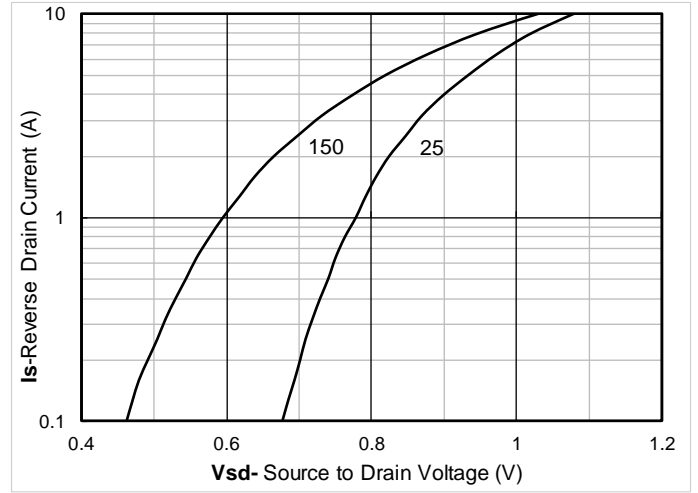


Figure 8. Forward characteristics of reverse diode

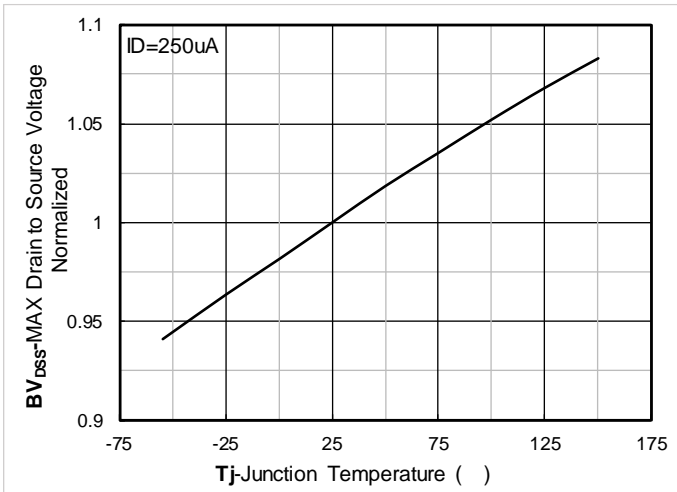


Figure 9. Normalized breakdown voltage

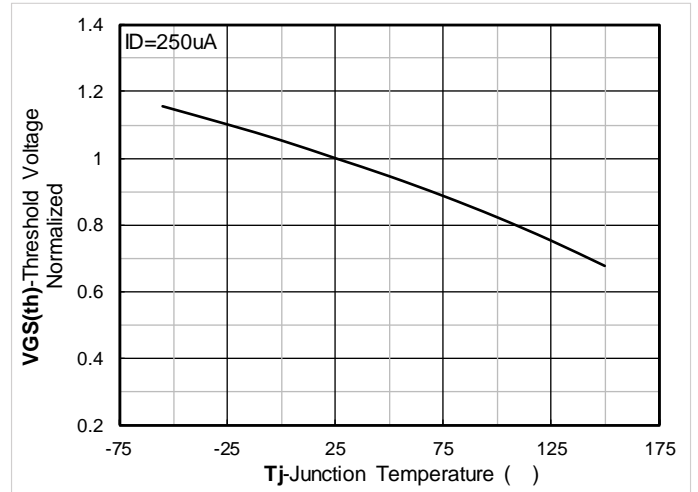


Figure 10. Normalized Threshold voltage

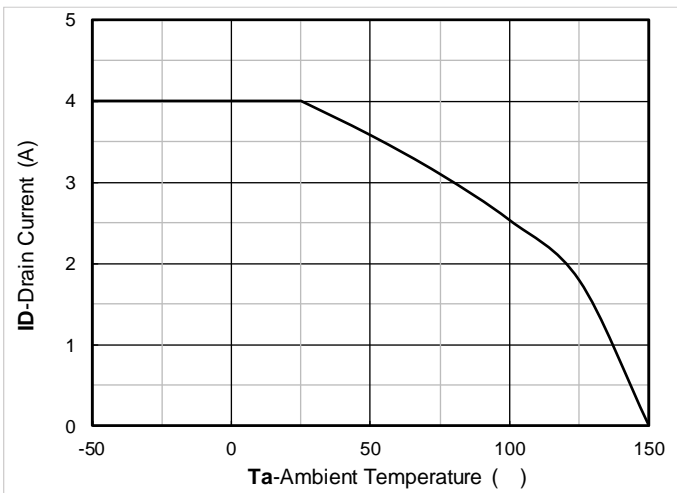


Figure 11. Current dissipation

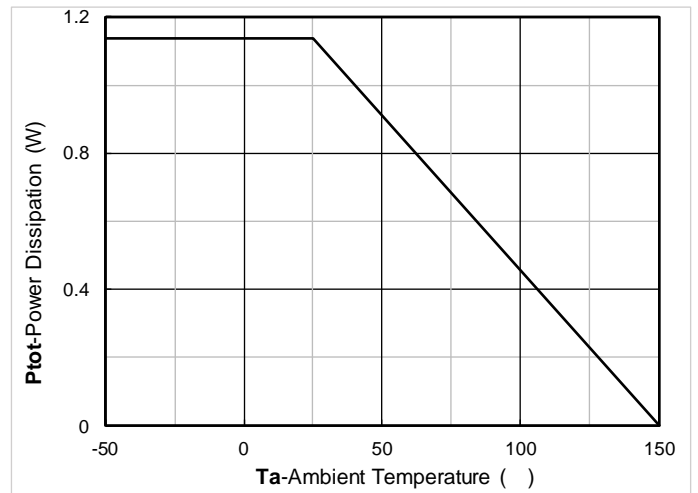


Figure 12. Power dissipation

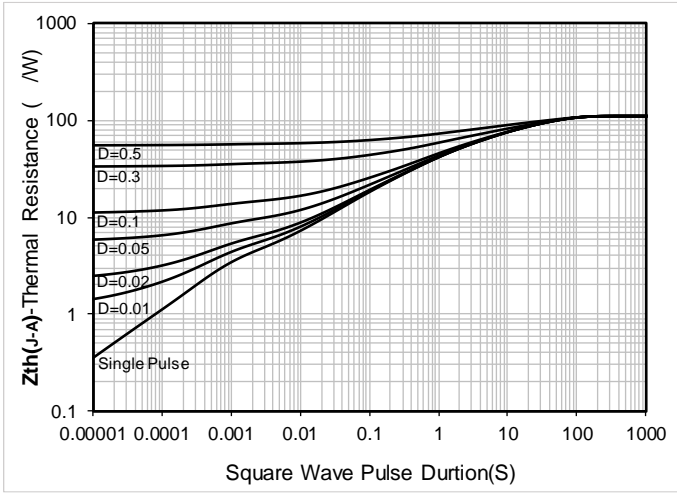


Figure 13. Maximum Transient Thermal Impedance

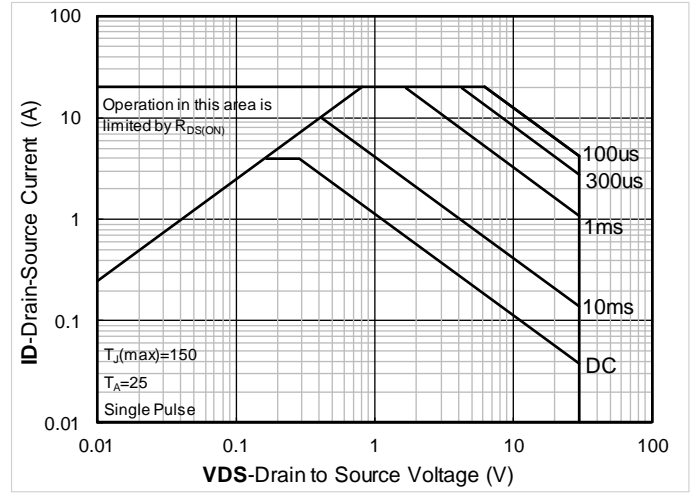


Figure 14. Safe Operation Area

PMOS Typical Electrical and Thermal Characteristics Diagrams

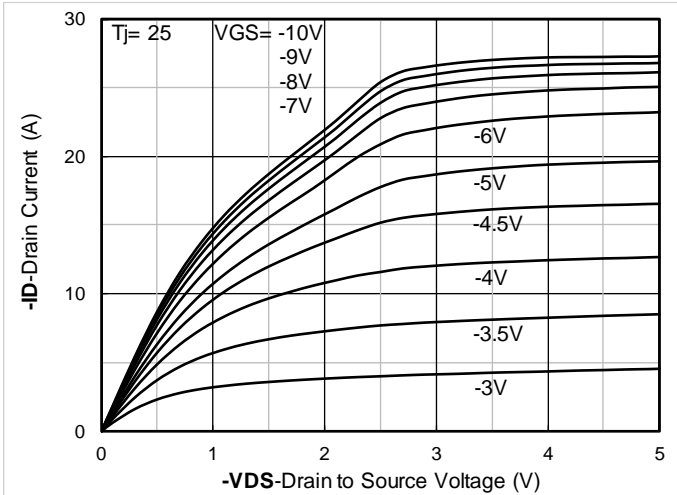


Figure 1. Output Characteristics

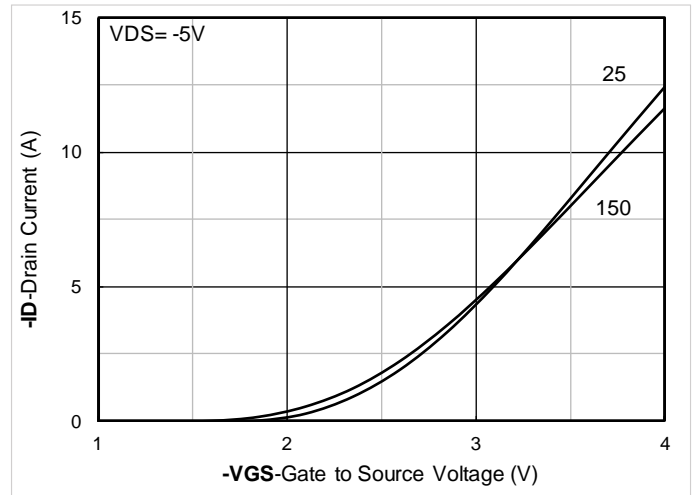


Figure 2. Transfer Characteristics

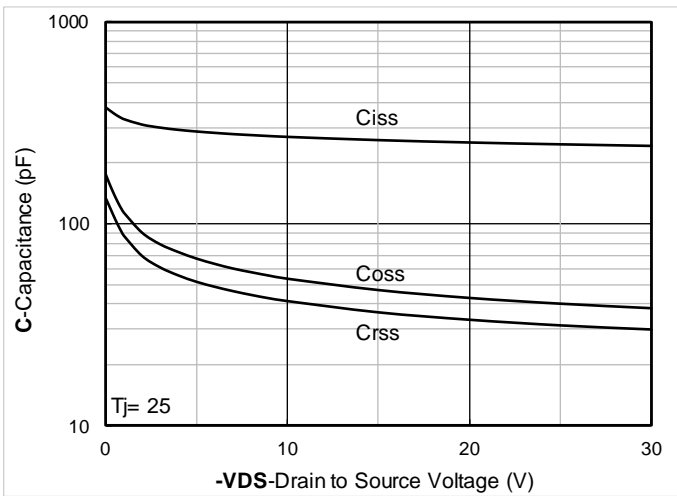


Figure 3. Capacitance Characteristics

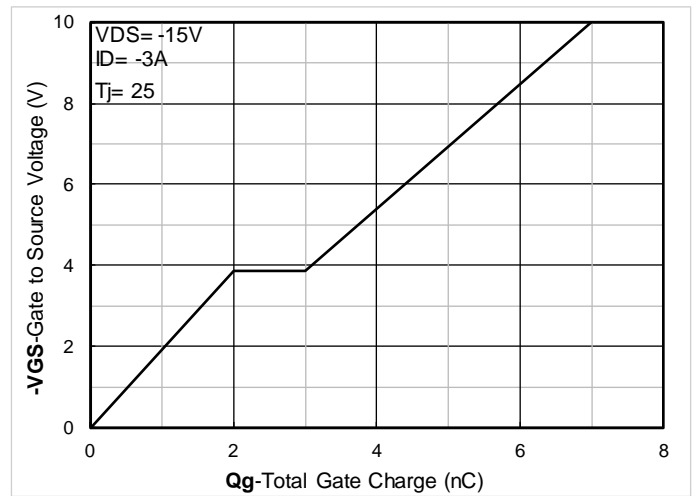


Figure 4. Gate Charge

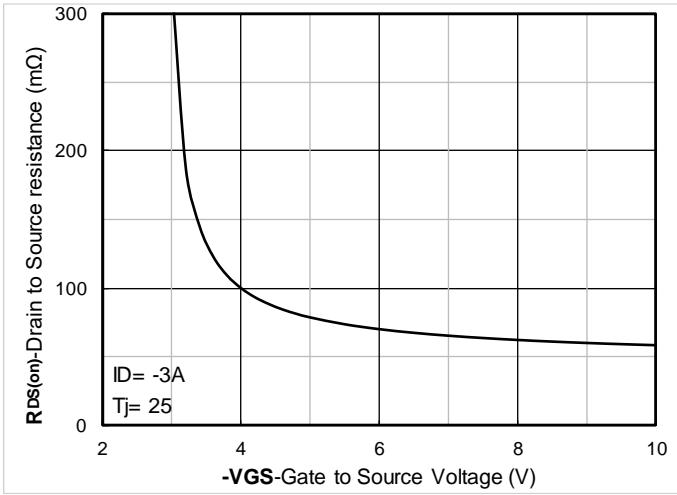


Figure 5. On-Resistance vs Gate to Source Voltage

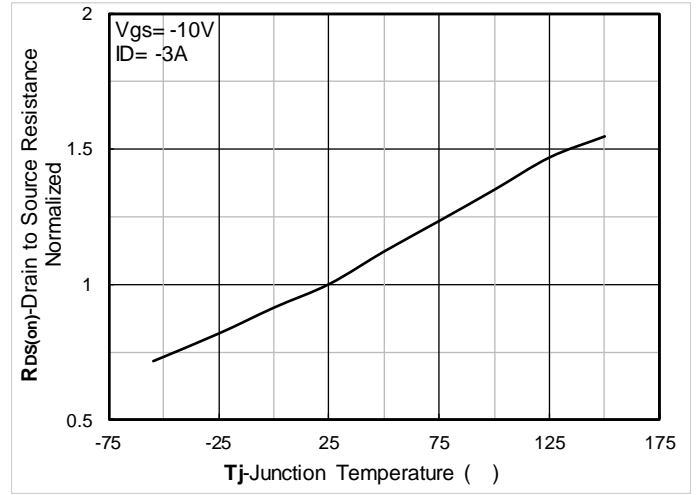


Figure 6. Normalized On-Resistance

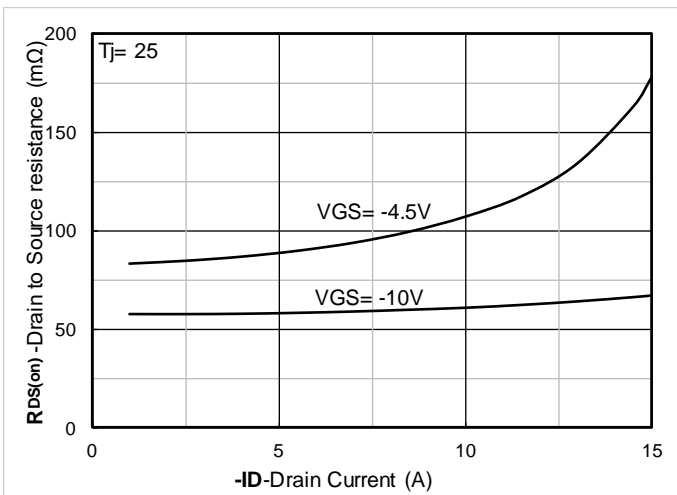


Figure 7. RDS(on) VS Drain Current

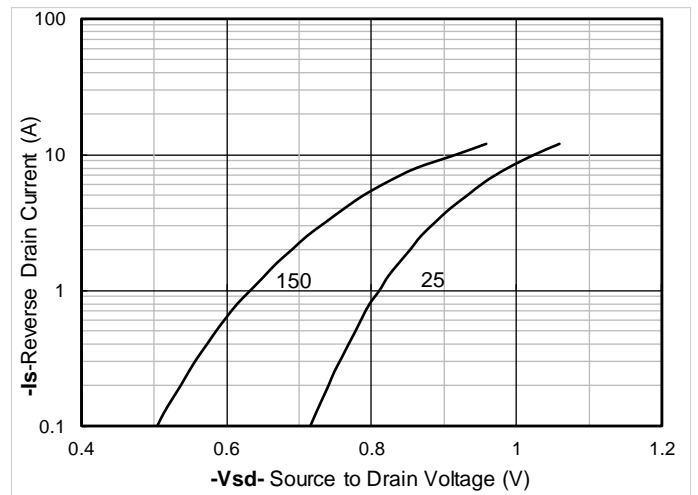


Figure 8. Forward characteristics of reverse diode

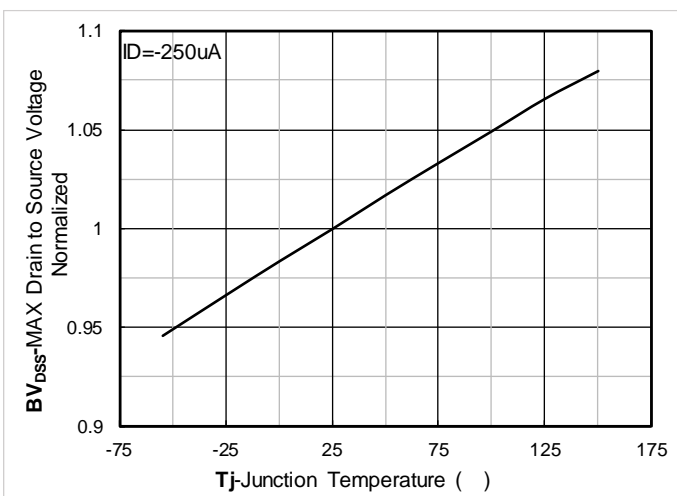


Figure 9. Normalized breakdown voltage

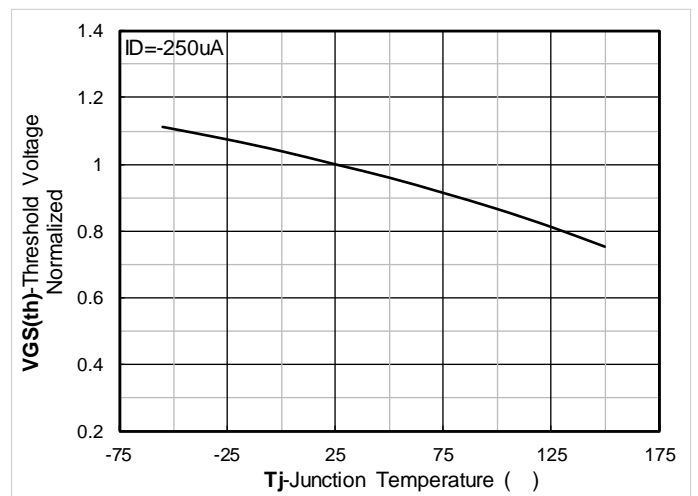


Figure 10. Normalized Threshold voltage

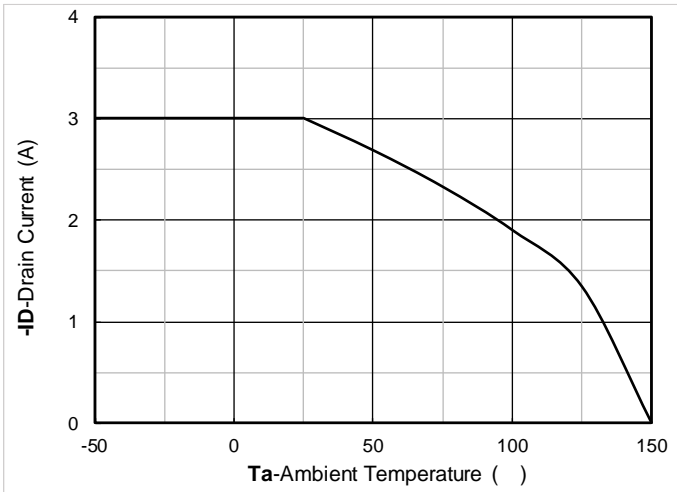


Figure 11. Current dissipation

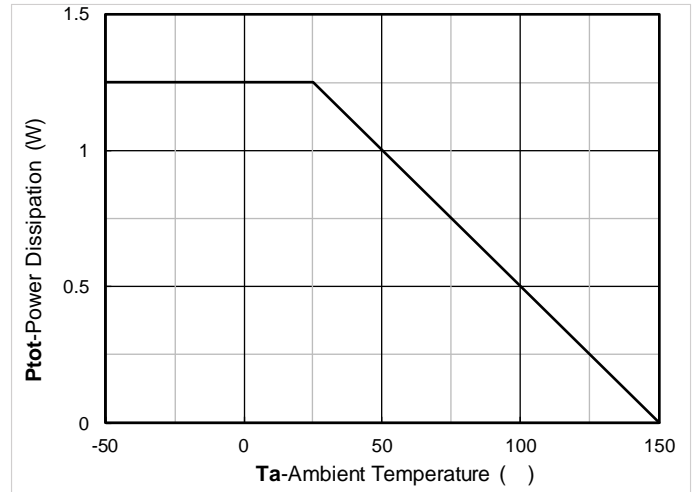


Figure 12. Power dissipation

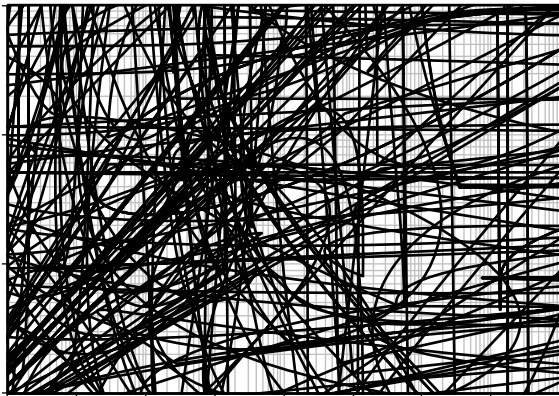


Figure 13. Maximum Transient Thermal Impedance

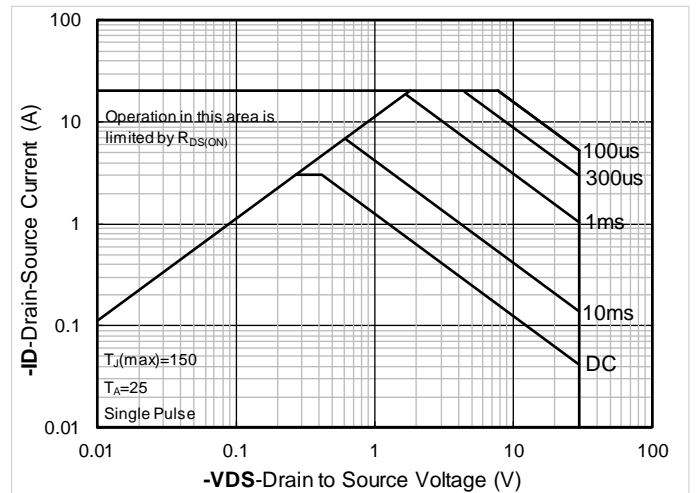
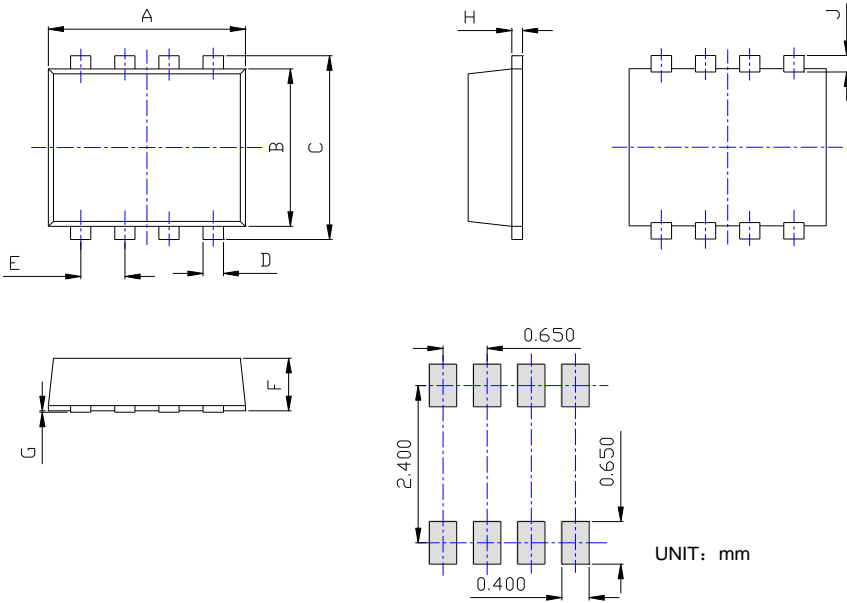


Figure 14. Safe Operation Area



YJU3724A

■ PDFN3030-8L Package information



DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.108	0.120	2.750	3.050
B	0.089	0.100	2.250	2.550
C	0.104	0.116	2.650	2.950
D	0.008	0.016	0.200	0.400
E	0.026 TYP		0.650 TYP	
F	0.028	0.035	0.700	0.900
G	0.000	0.004	0.000	0.100
H	0.004	0.012	0.100	0.300
J	0.007	0.015	0.190	0.390

NOTE:
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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