



N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- V_{DS} 100V
- I_D 280A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<2.3m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=6V$) $<3.5m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Double trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen



YJT280G10HJ

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
		V _{DS} =100V, V _{GS} =0V, T _J =150°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =140A	-	1.7	2.3	mΩ
		V _{GS} =10V, I _D =50A	-	1.7	2.3	
		V _{GS} =6V, I _D =50A	-	2.4	3.5	
Diode Forward Voltage	V _{SD}	I _S =140A, V _{GS} =0V	-	0.9	1.2	V
Gate resistance	R _G	f=1MHz, Open drain	-	1.3	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	280	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	15200	-	pF
Output Capacitance	C _{oss}		-	1850	-	
Reverse Transfer Capacitance	C _{rss}		-	50	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V,				



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Typical Electrical and Thermal Characteristics Diagrams

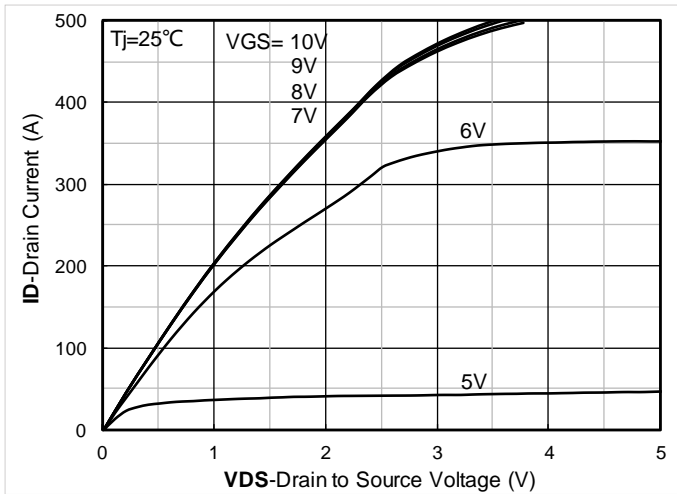


Figure 1. Output Characteristics

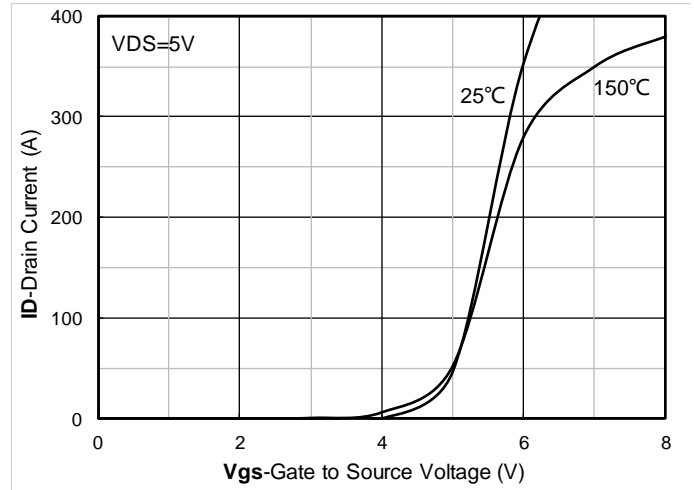


Figure 2. Transfer Characteristics

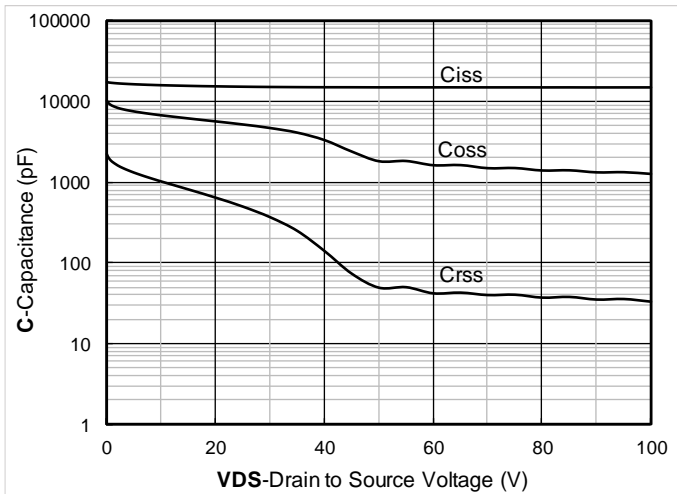


Figure 3. Capacitance Characteristics

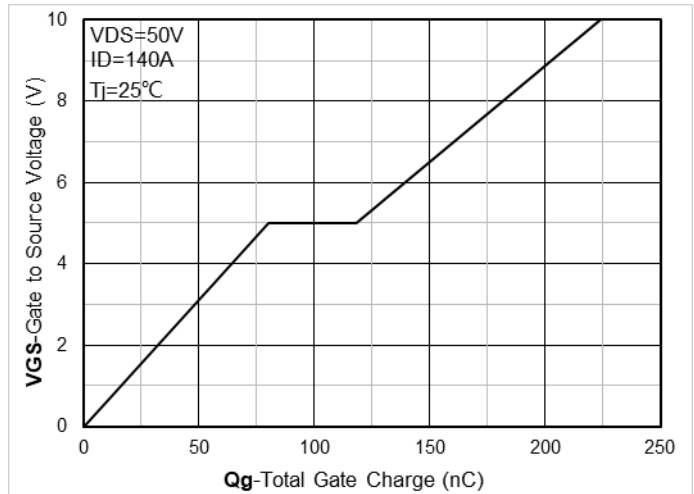


Figure 4. Gate Charge

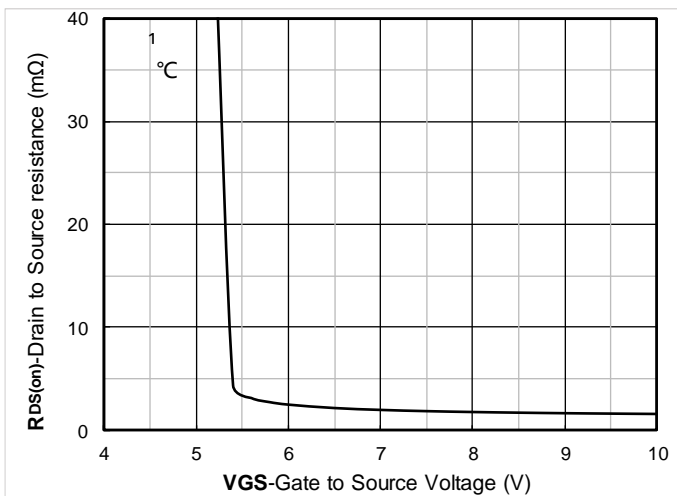


Figure 5. On-Resistance vs Gate to Source Voltage

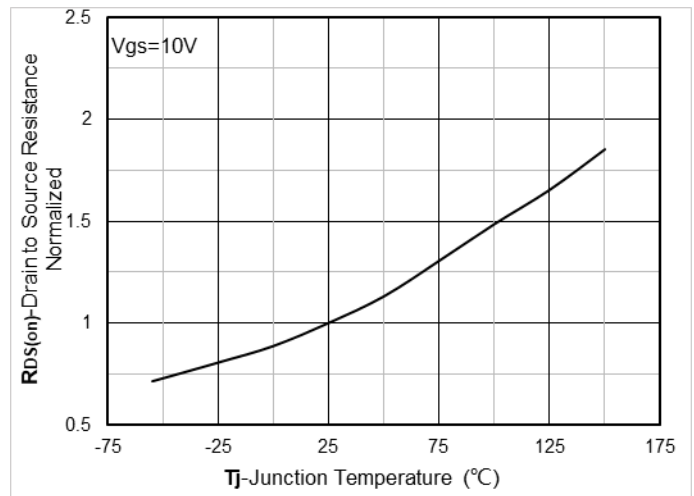


Figure 6. Normalized On-Resistance



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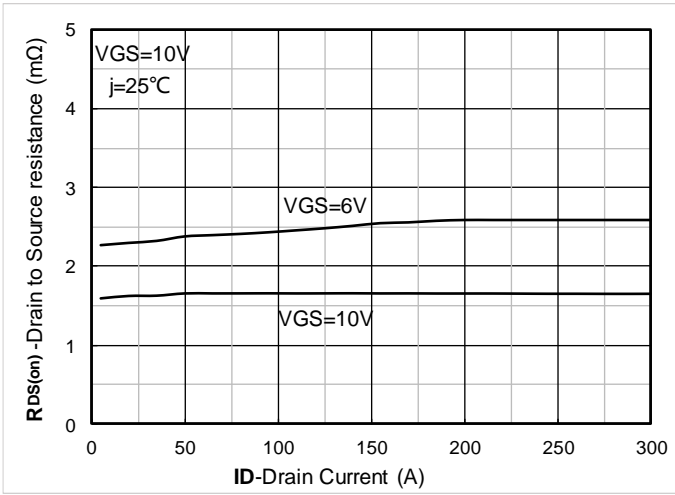


Figure 7. $R_{DS(on)}$ VS Drain Current

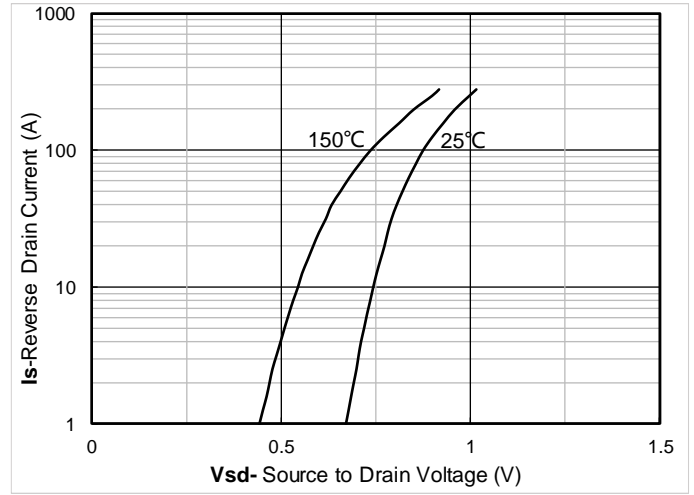


Figure 8. Forward characteristics of reverse diode

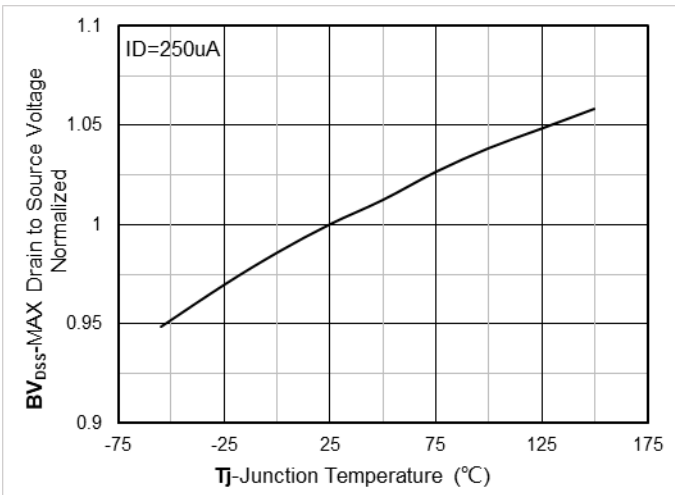


Figure 9. Normalized breakdown voltage

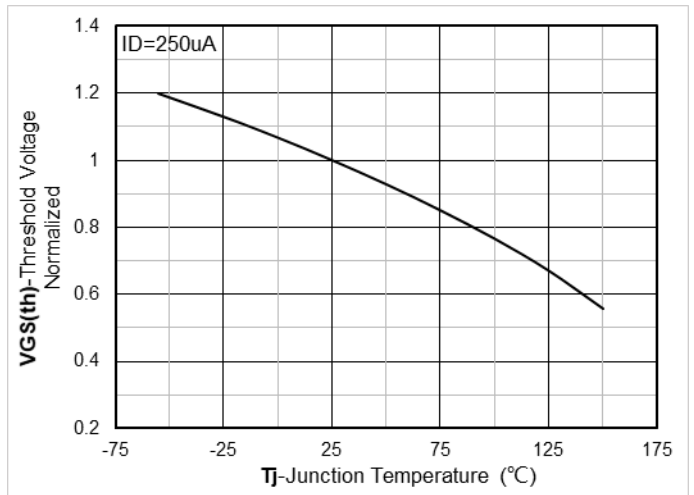


Figure 10. Normalized Threshold voltage

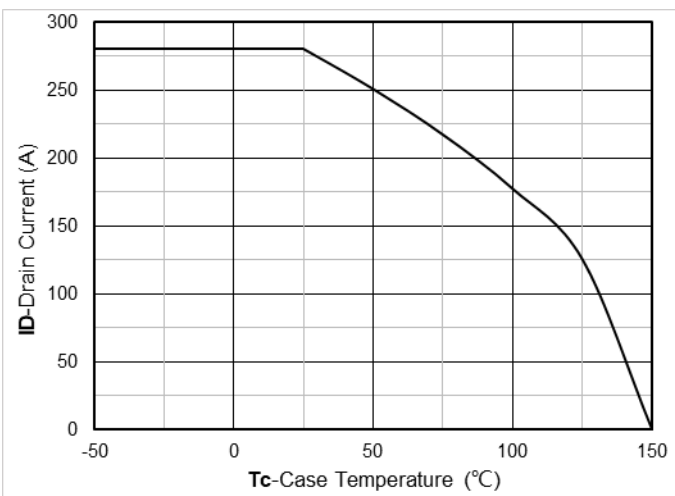


Figure 11. Current dissipation

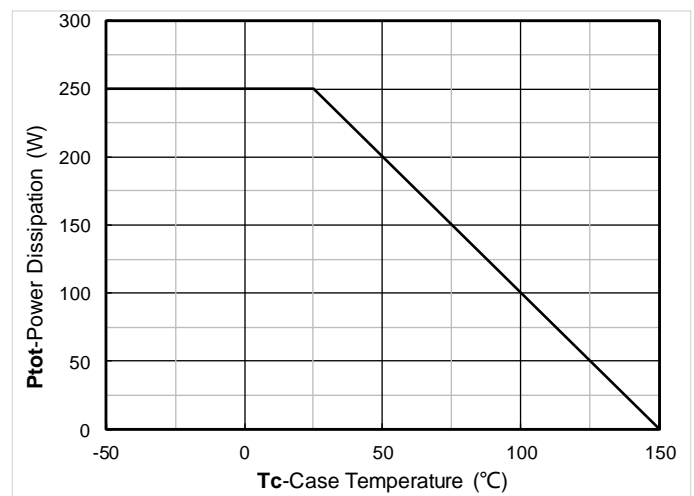


Figure 12. Power dissipation

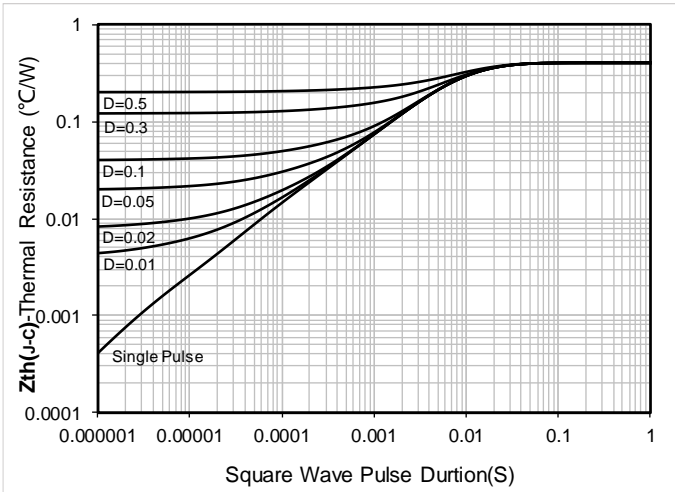


Figure 13. Maximum Transient Thermal Impedance

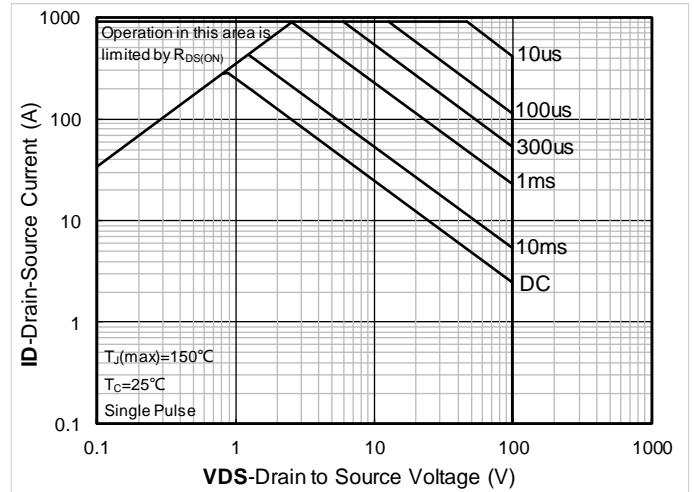


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

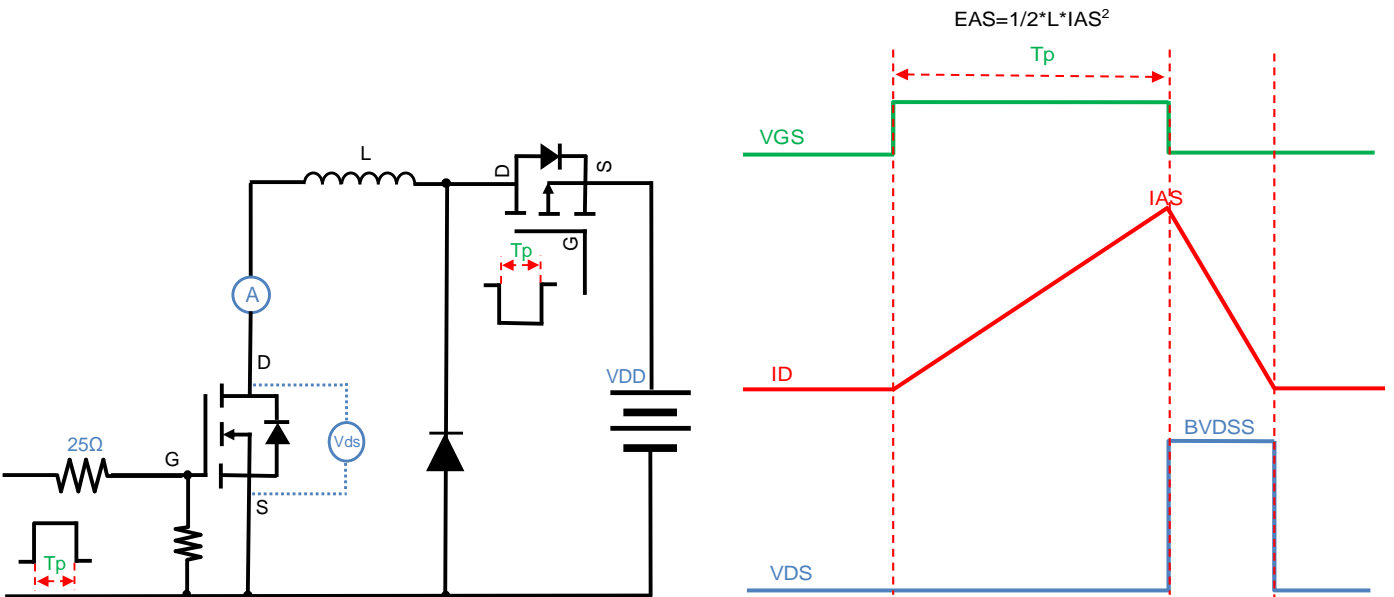


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

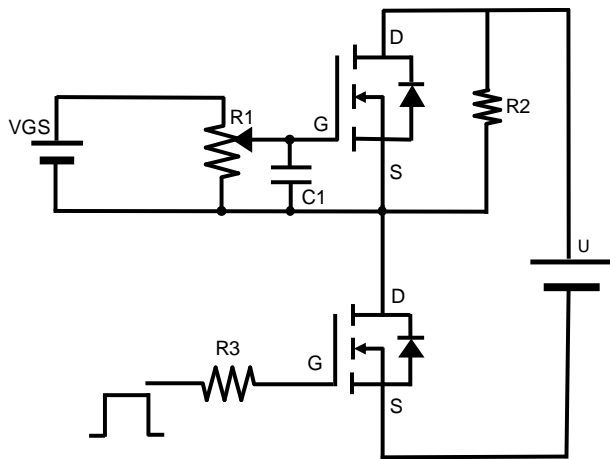


Figure B. Gate Charge Test Circuit & Waveform

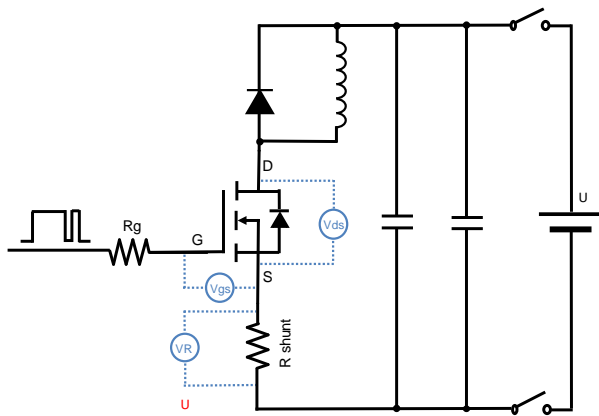


Figure C. Resistive Switching Test Circuit & Waveform

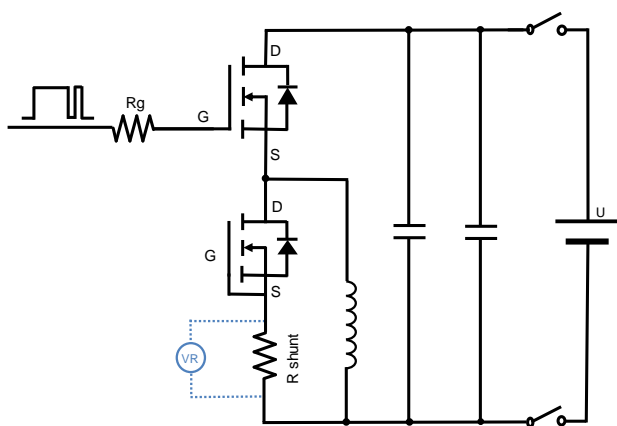
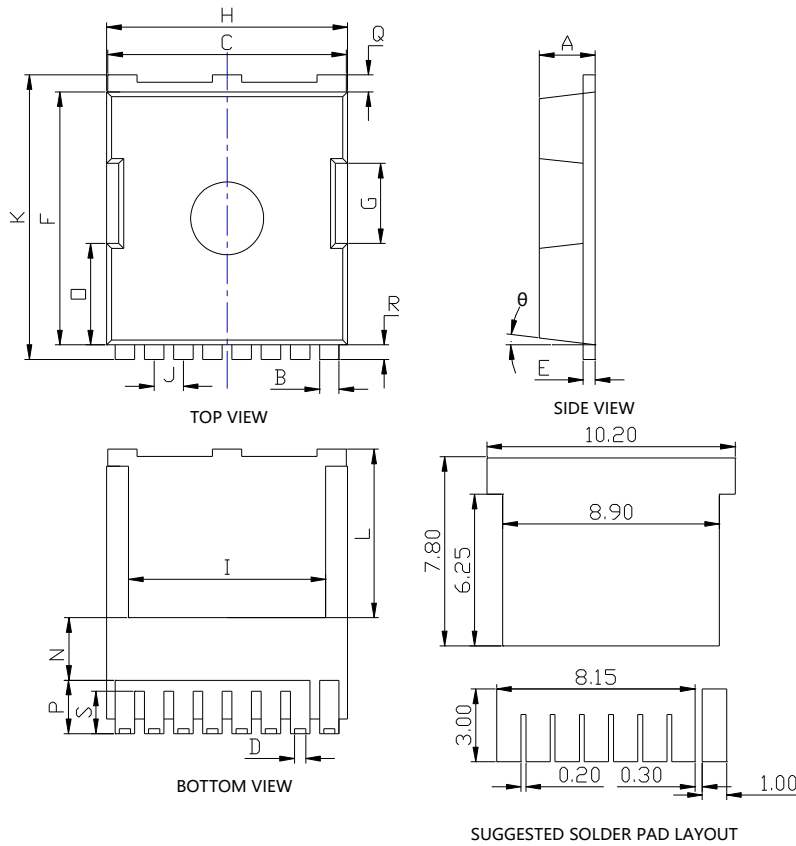


Figure D. Diode Recovery Test Circuit & Waveform



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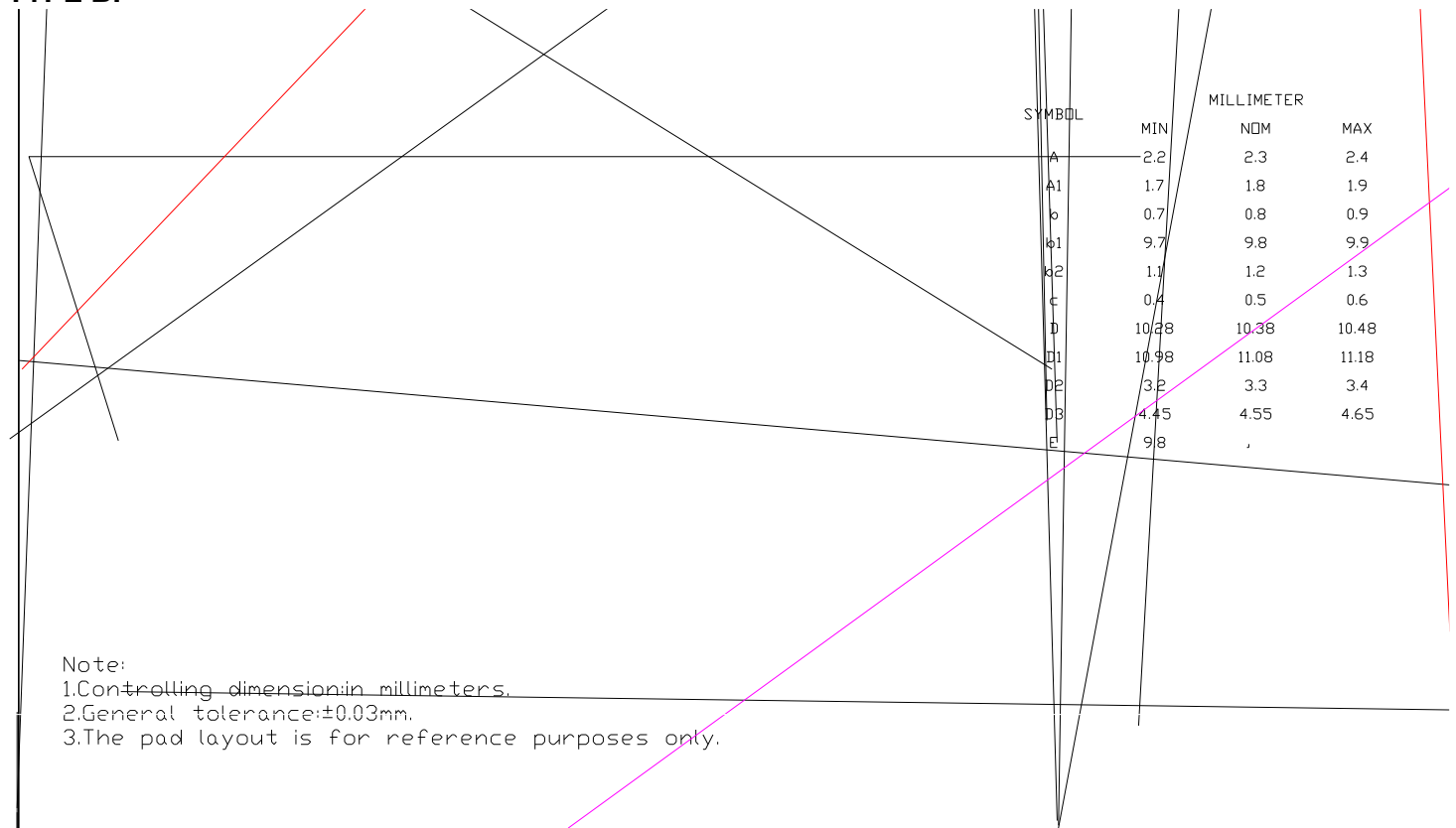
■TOLL Package information TYPE A:



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.087	0.094	2.20	2.40
B	0.028	0.035	0.70	0.90
C	0.382	0.390	9.70	9.90
D	0.017	0.020	0.42	0.50
E	0.016	0.024	0.40	0.60
F	0.405	0.417	10.28	10.58
G	0.122	0.138	3.10	3.50
H	0.382	0.398	9.70	10.10
I	0.311	0.327	7.90	8.30
J	0.047BSC.		1.20BSC.	
K	0.452	0.468	11.48	11.88
L	0.266	0.281	6.75	7.15
N	0.118	0.130	3.00	3.30
Q	0.157	0.172	3.98	4.38
P	0.055	0.071	1.40	1.80
R	0.024	0.031	0.60	0.80
S	0.039	0.051	1.00	1.30
θ	4°	10°	4°	10°

NOTE:
 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.

TYPE B:





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