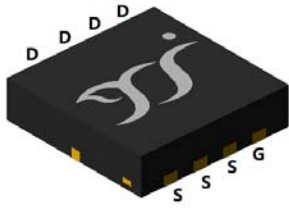
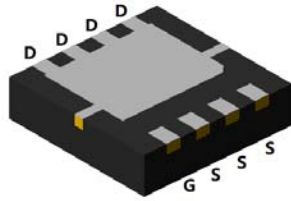


## N-Channel Enhancement Mode Field Effect Transistor

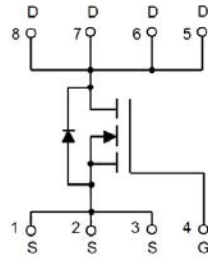


Top View



Bottom View

**DFN3333-8L**



### Product Summary

- $V_{DS}$  60V
- $I_D$  70A
- $R_{DS(ON)}$ ( at  $V_{GS}=10V$ )  $<5.5m\Omega$
- $R_{DS(ON)}$ ( at  $V_{GS}=4.5V$ )  $<9.5m\Omega$
- 100% EAS Tested

### General Description

- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Part no. with suffix "Q" means AEC-Q101 qualified

### Applications

- Power switching application
- Uninterruptible power supply
- DC-DC converter
- 12V and 24V Automotive systems

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	60	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_C=25^\circ C$	$I_D$	70	A
	$T_C=100^\circ C$		49	
	$T_A=25^\circ C$		13	
	$T_A=100^\circ C$		9.6	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	270	A
Avalanche energy <sup>B</sup>		EAS	144	mJ
Total Power Dissipation <sup>C</sup>	$T_C=25^\circ C$	$P_D$	96	W
	$T_C=100^\circ C$		48	
	$T_A=25^\circ C$		2.9	
	$T_A=100^\circ C$		1.4	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.56	$^\circ C/W$
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State	$R_{\theta JA}$	51	$^\circ C/W$
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+175	$^\circ C$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ70G06AQ	F1	Q70G06A	5000	10000	100000	13" reel



# YJQ70G06AQ

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.7	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		4.6	5.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		6.5	9.5	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V		0.8	1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz		1.6		Ω
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz	-	1780		pF
Output Capacitance	C <sub>oss</sub>		-	1000		
Reverse Transfer Capacitance	C <sub>rss</sub>		-	81		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =30A	-	38.5	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	9	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	8.2	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=100A/us	-	31.5	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	37	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =30V, I <sub>DS</sub> =10A, R <sub>G</sub> =3Ω	-	14.2	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	54.6	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	28	-	
Turn-off fall Time	t <sub>f</sub>		-	10.5	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V<sub>DD</sub>=30V, V<sub>GS</sub>=10V, L=1mH, I<sub>AS</sub>=17A.

C. P<sub>d</sub> is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in the still air environment with T<sub>A</sub>=25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design..



## Typical Electrical and Thermal Characteristics Diagrams

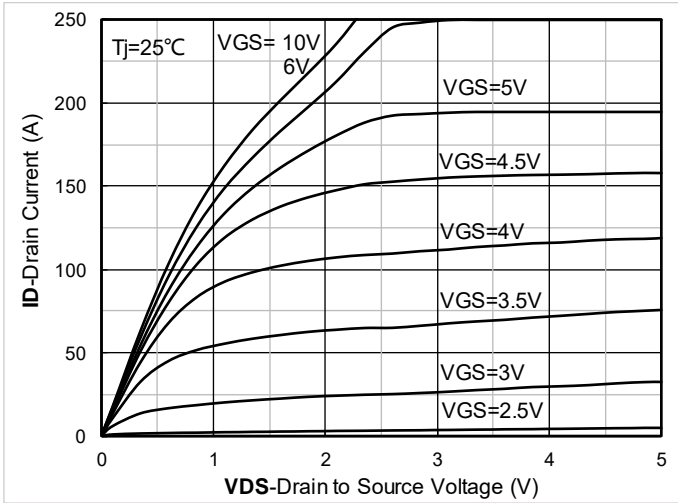


Figure 1. Output Characteristics

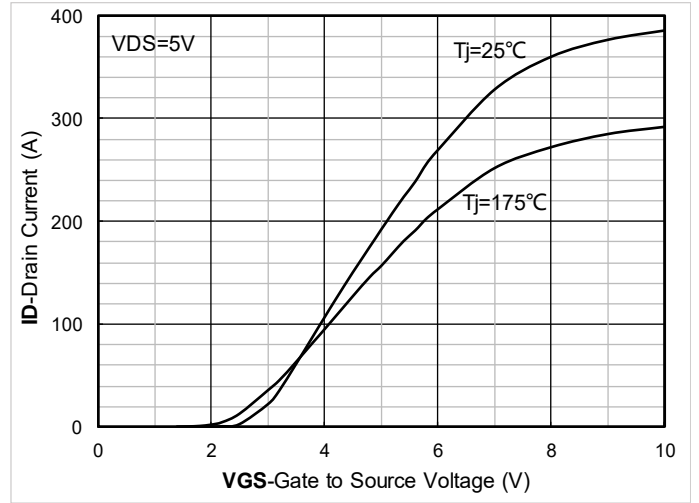


Figure 2. Transfer Characteristics

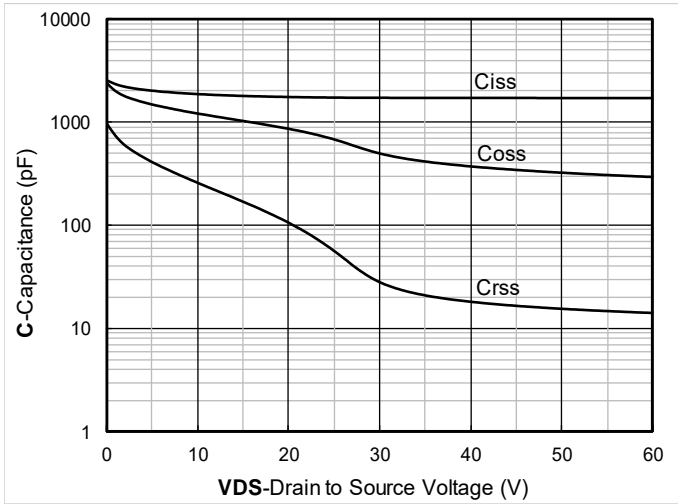


Figure 3. Capacitance Characteristics

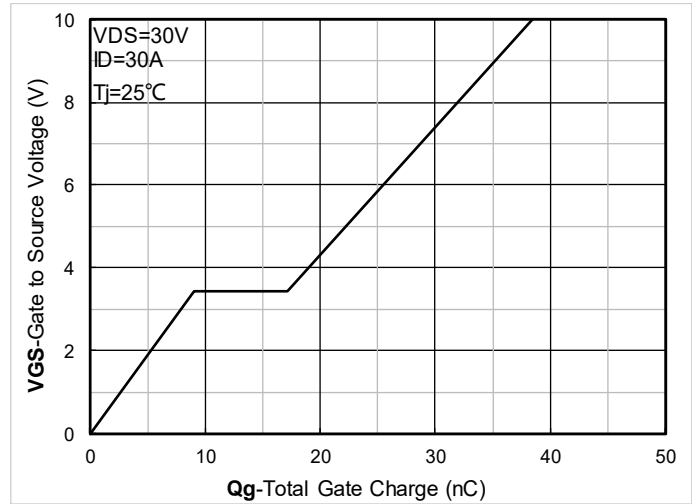


Figure 4. Gate Charge

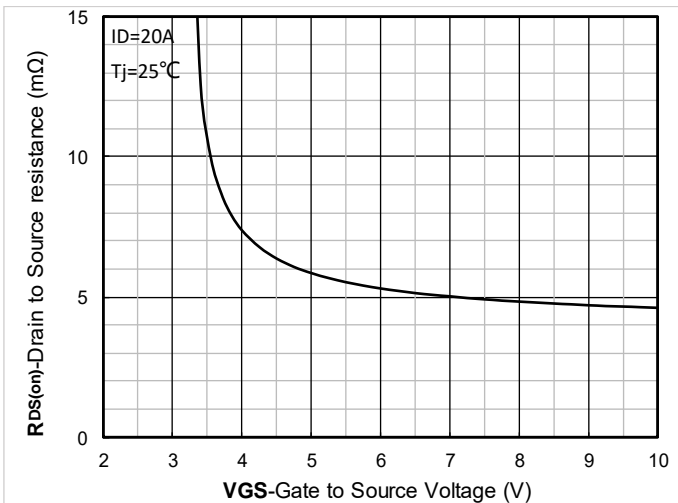


Figure 5. On-Resistance vs Gate to Source Voltage

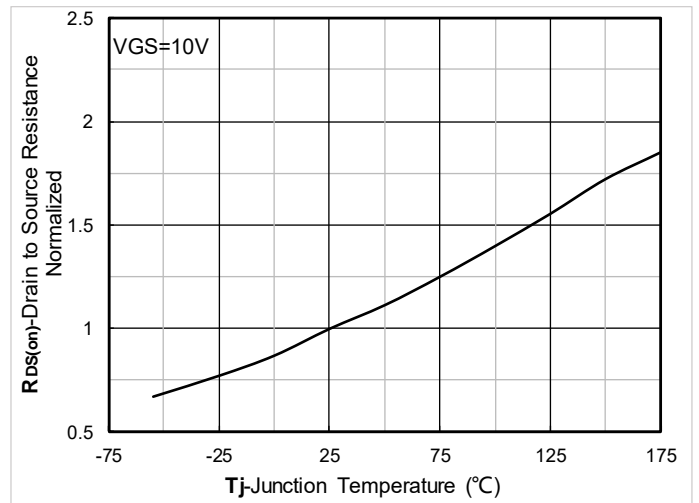


Figure 6. Normalized On-Resistance



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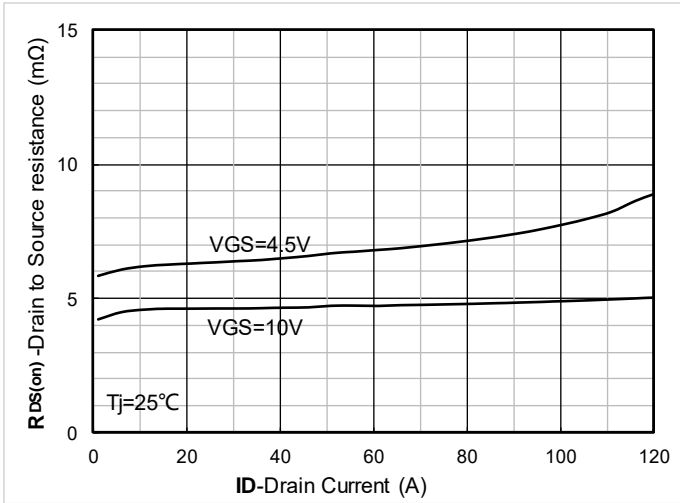


Figure 7.  $R_{DS(on)}$  VS Drain Current

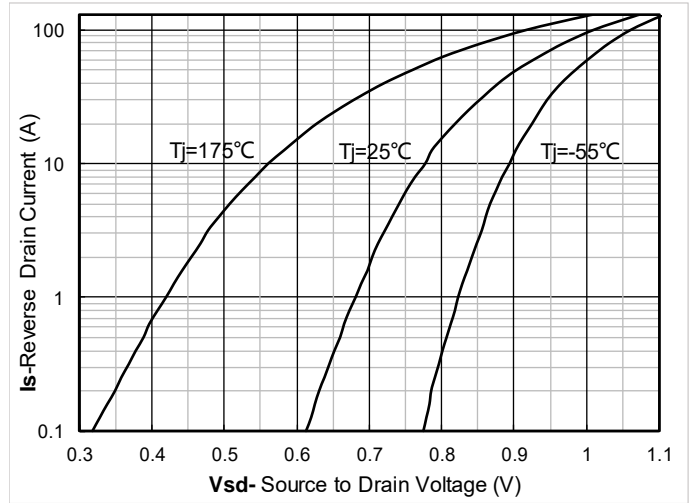


Figure 8. Forward characteristics of reverse diode

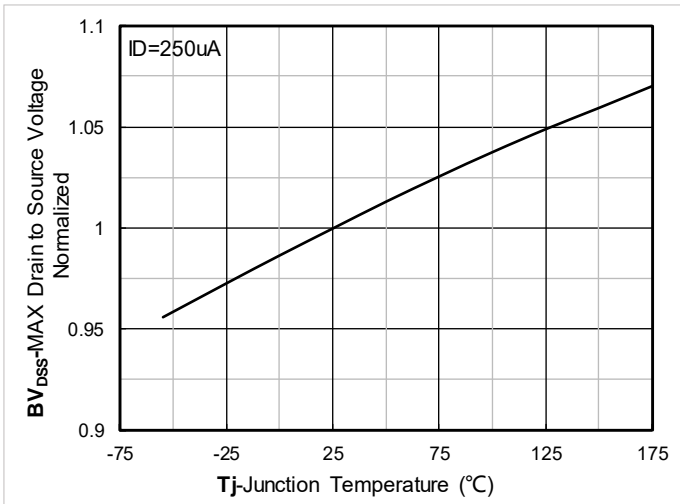


Figure 9. Normalized breakdown voltage

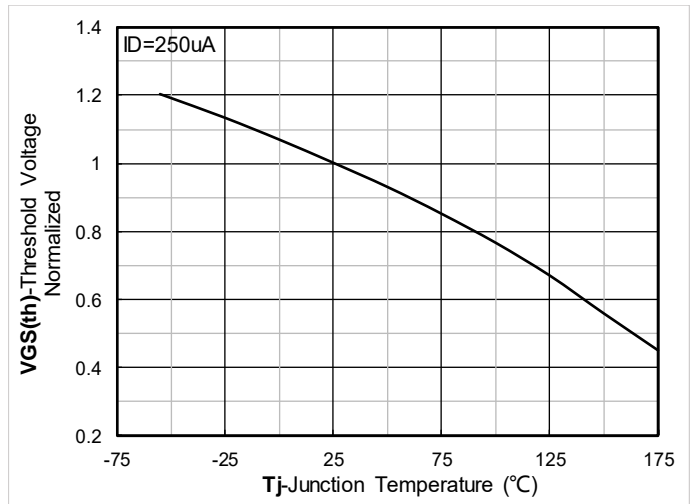


Figure 10. Normalized Threshold voltage

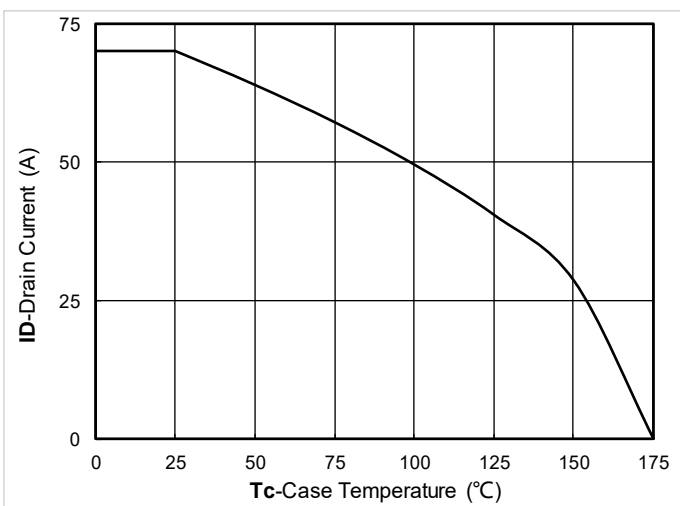


Figure 11. Current dissipation

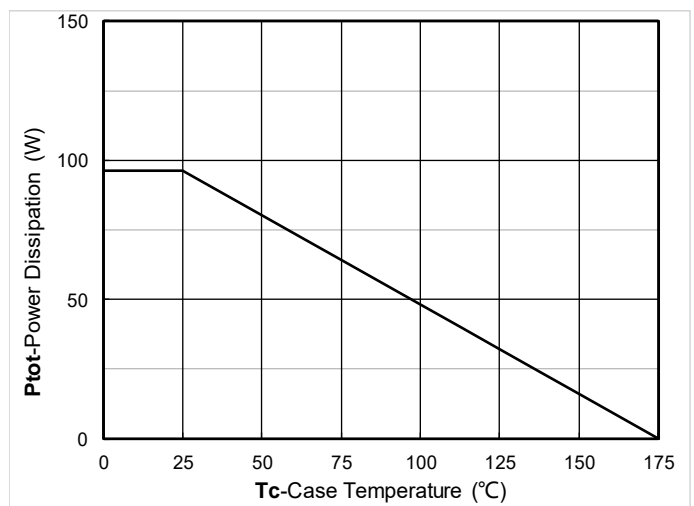


Figure 12. Power dissipation



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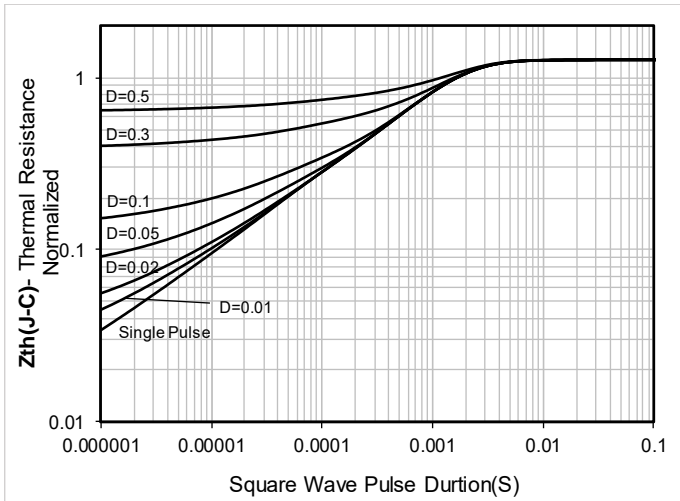


Figure 13. Maximum Transient Thermal Impedance

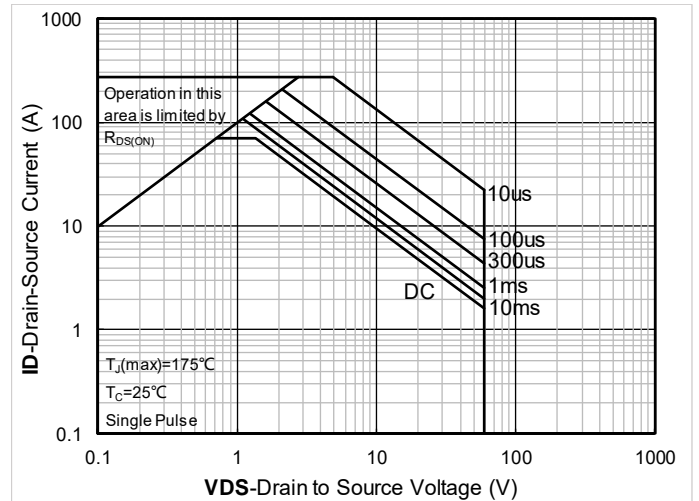
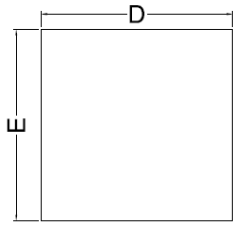


Figure 14. Safe Operation Area

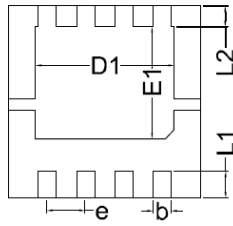


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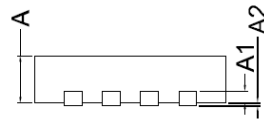
## DFN3333-8L Package information



Top View  
正面视图

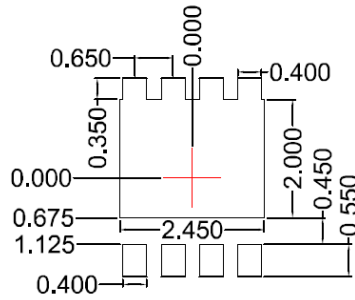


Bottom View  
背面视图



Side View  
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout  
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10\text{mm}$ .
3. The pad layout is for reference purposes only.



## YJQ70G06AQ

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