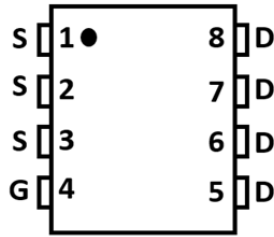
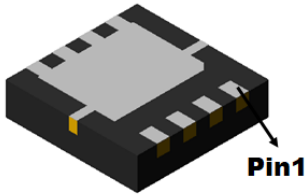
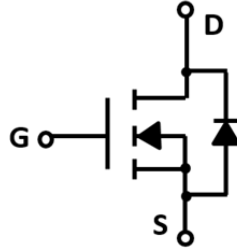


N-Channel Enhancement Mode Field Effect Transistor



DFN3333



Product Summary

V_{DS}	30 V
I_D	60 A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	<3.2 mohm
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<4.0 mohm
100% UIS Tested	
100% ∇V_{DS} Tested	

General Description

Trench Power LV MOSFET technology
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$

Applications

DC-DC Converters
Power management functions
Backlighting

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	60	A
	$T_C=100^\circ\text{C}$		38	
Pulsed Drain Current ^A		I_{DM}	240	A
Total Power Dissipation @ $T_C=25^\circ\text{C}$ ^B		P_D	75	W
Total Power Dissipation @ $T_C=100^\circ\text{C}$ ^B		P_D	30	W
Total Power Dissipation @ $T_A=25^\circ\text{C}$ ^C		P_D	6.2	W
Single Pulse Avalanche Energy ^D		E_{AS}	400	mJ
Thermal Resistance Junction-to-Case		R_{JC}	1.67	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Ambient		R_{JA}	20	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ60N03A	F1	Q60N03A	5000	10000	100000	13" reel



YJQ60N03A

Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =20A		2.6	3.2	m
		V _{GS} = 4.5V, I _D =20A		3.4	4.0	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V		0.85	1.2	V
Gate resistance	R _g	F=1 MHz, Open drain		2.9		Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHZ		4498		pF
Output Capacitance	C _{oss}			800		
Reverse Transfer Capacitance	C _{rss}			643		
Switching Parameters						
Total Gate Charge	Q _g (10V)	V _{GS} =10V, V _{DS} =15V, I _D =20A		92.7		nC
Total Gate Charge	Q _g (4.5V)			46		
Gate-Source Charge	Q _{gs}			13.5		
Gate-Drain Charge	Q _{gd}			22.8		
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=500A/us		3.0		nC
Reverse Recovery Time	t _{rr}			15		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =20V, I _D =4A, R _L =0.75 R _{GEN} =3		11		ns
Turn-on Rise Time	t _r			80		
Turn-off Delay Time	t _{D(off)}			39		
Turn-off fall Time	t _f			92		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. The value of R_{JA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.

D. T_J=25°C, V_{DD}=20V, V_G=10V, L=2.0mH, I_{AS}=20A.



■ Typical Performance Characteristics

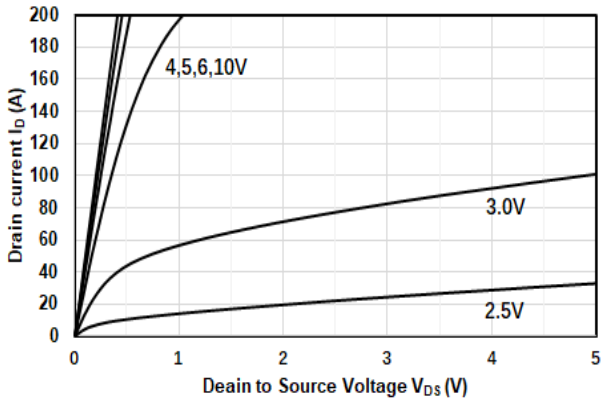


Figure1. Output Characteristics

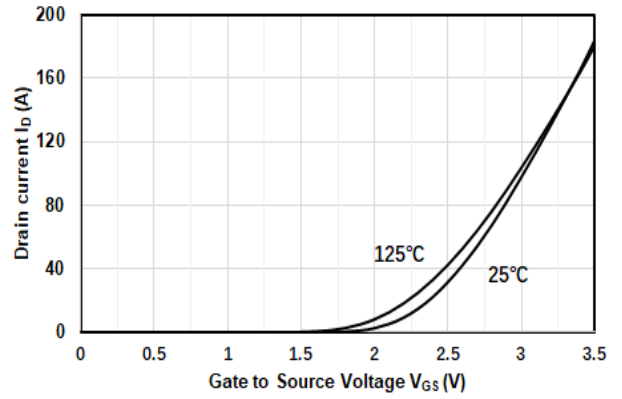


Figure2. Transfer Characteristics

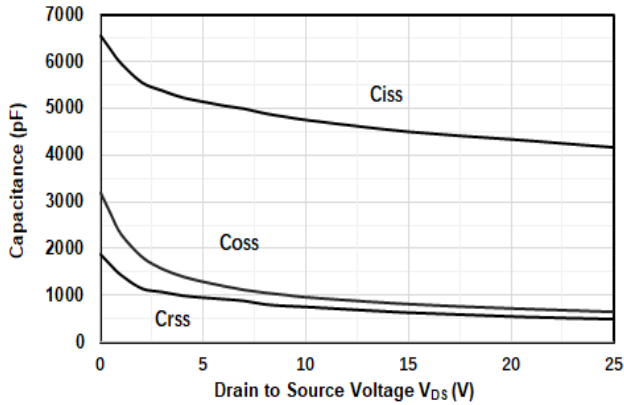


Figure3. Capacitance Characteristics

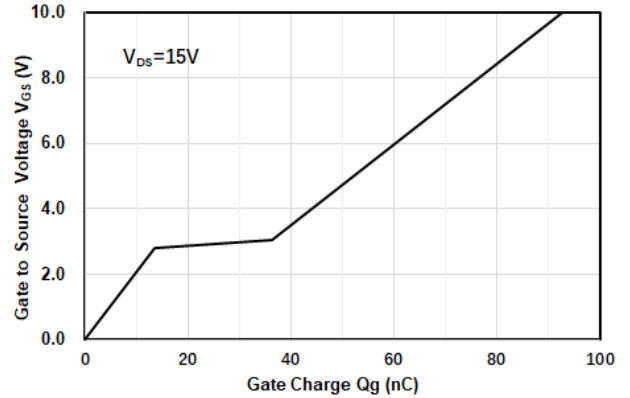


Figure4. Gate Charge

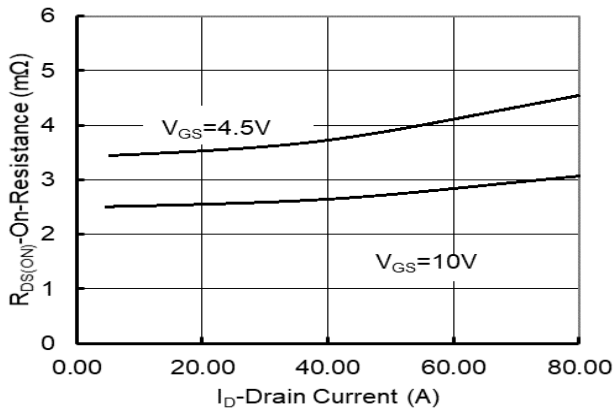


Figure5. Drain-Source on Resistance

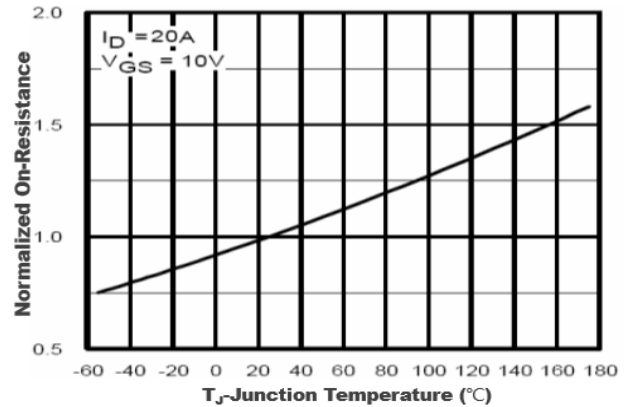


Figure6. Drain-Source on Resistance



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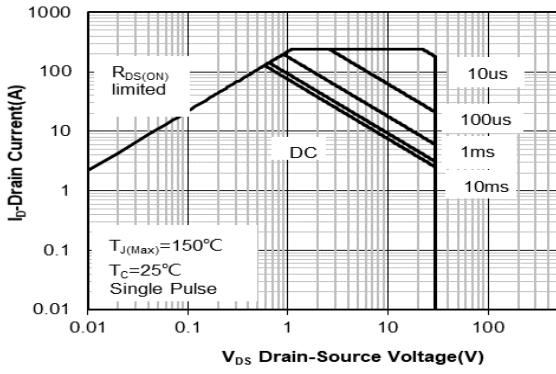


Figure7. Safe Operation Area

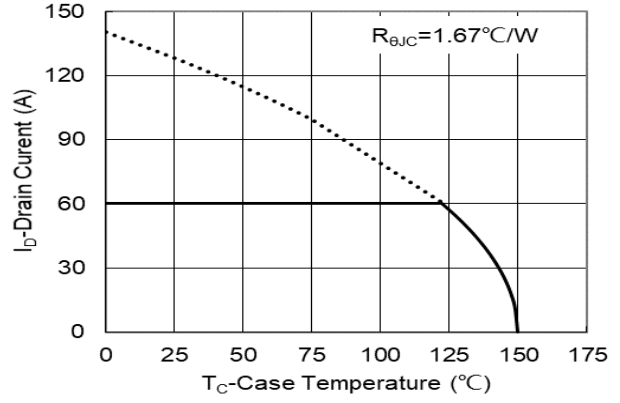


Figure8. Drain current vs. Case Temperature

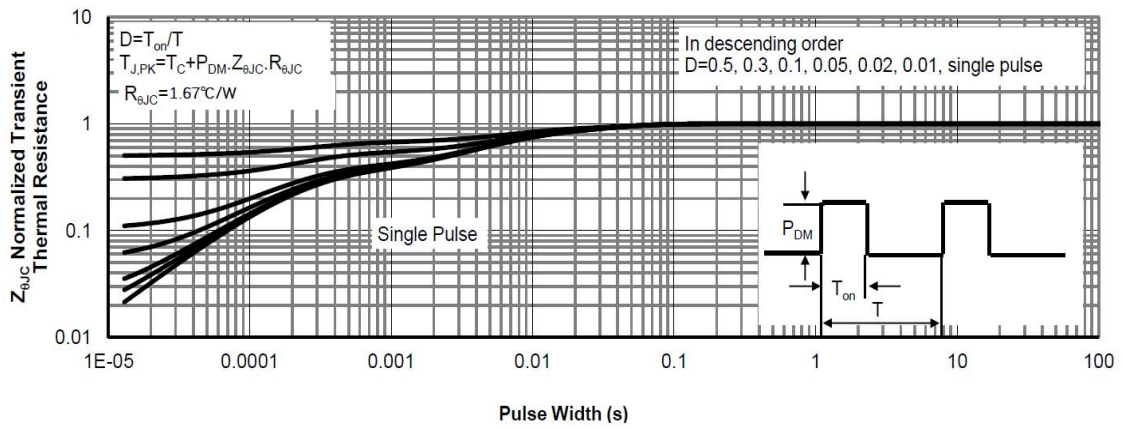
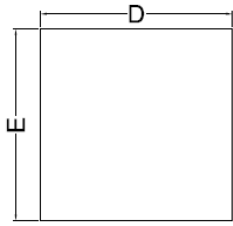


Figure9. Normalized Maximum Transient Thermal Impedance

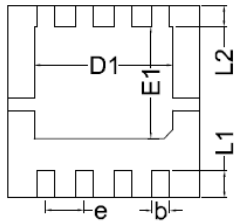


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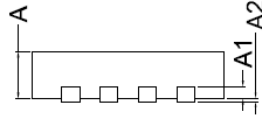
DFN3333 Package information



Top View
正面视图

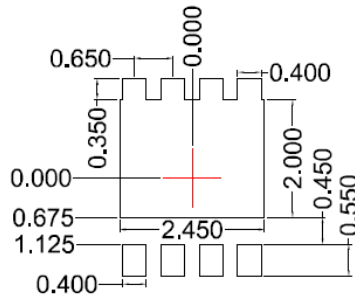


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.



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