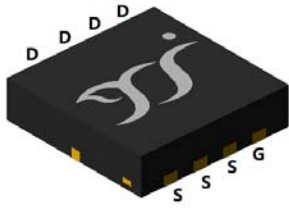
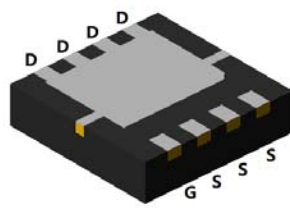


N-Channel Enhancement Mode Field Effect Transistor

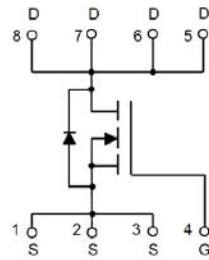


Top View



Bottom View

DFN3333-8L



Product Summary

V_{DS}	100V
I_D	40A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 18.5m
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 22.5m
100% EAS Tested	

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC converter
- 12V, 24V and 48V Automotive systems

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	8	A
	$T_A=100^\circ C$		5	
	$T_C=25^\circ C$		40	
	$T_C=100^\circ C$		25	
Pulsed Drain Current ^A		I_{DM}	110	A
Avalanche energy ^B		EAS	81	mJ
Total Power Dissipation ^C	$T_A=25^\circ C$	P_D	2	W
	$T_A=100^\circ C$		0.9	
	$T_C=25^\circ C$		43	
	$T_C=100^\circ C$		17.2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	R_{JA}	45	55	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	R_{JC}	2.4	2.9	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ40G10AQ	F1	Q40G10A	5000	10000	100000	13" reel



YJQ40G10AQ

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA



YJQ40G10AQ

Typical Electrical and Thermal Characteristics Diagrams

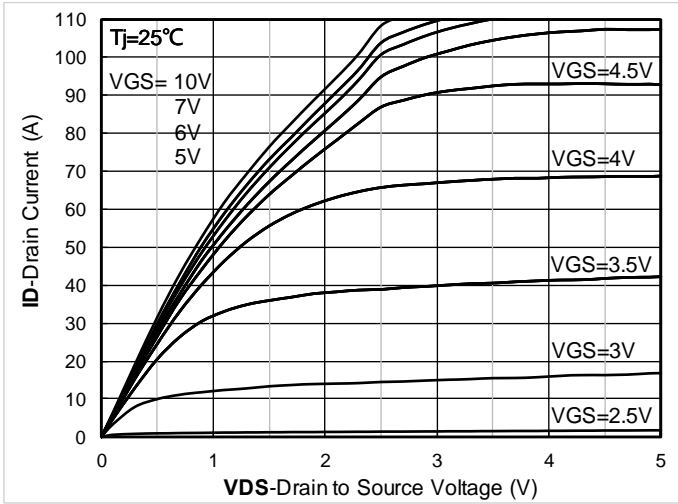


Figure 1. Output Characteristics

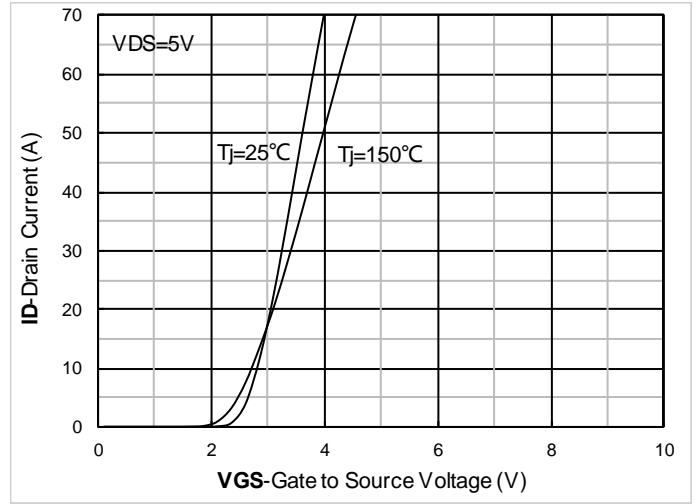


Figure 2. Transfer Characteristics

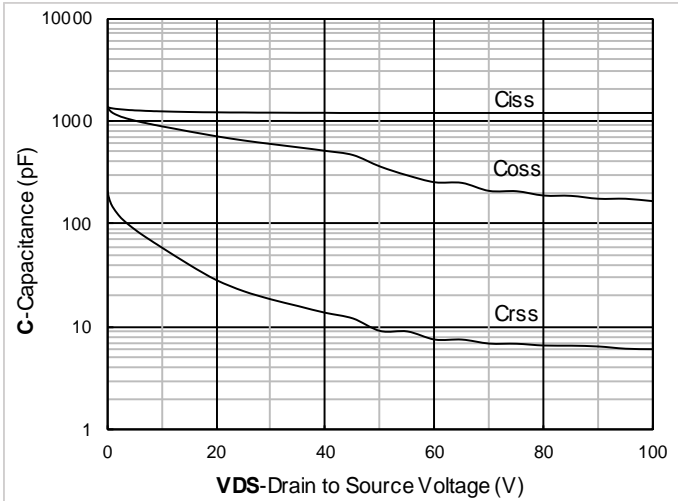


Figure 3. Capacitance Characteristics

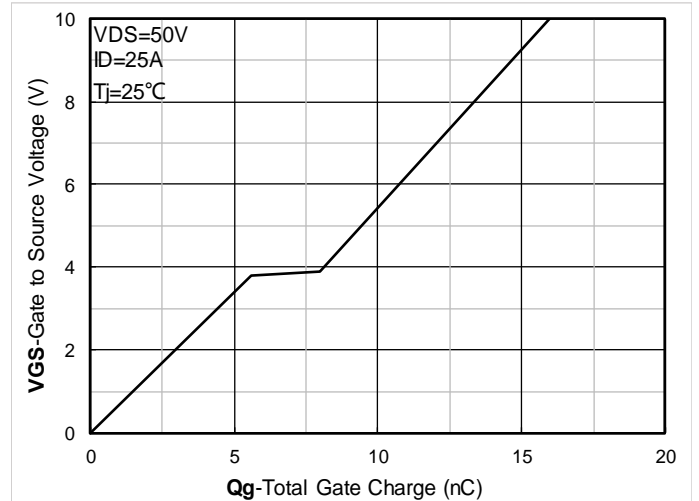


Figure 4. Gate Charge

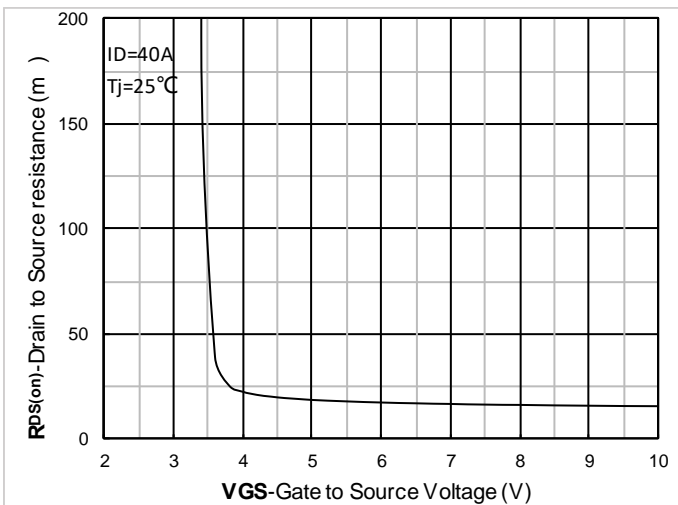


Figure 5. On-Resistance vs Gate to Source Voltage

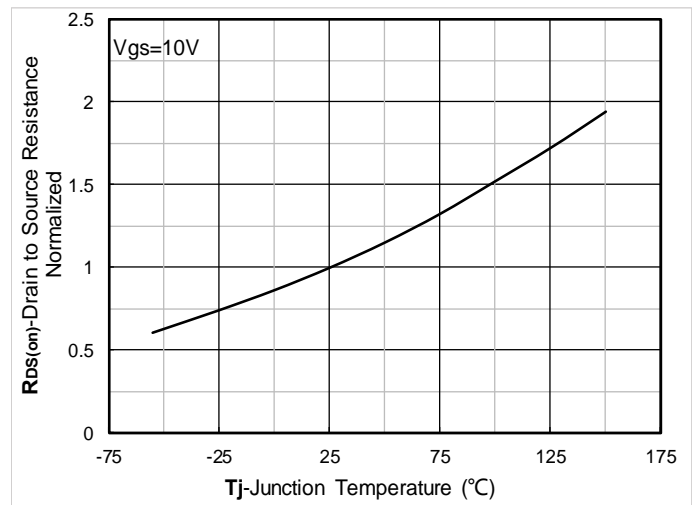


Figure 6. Normalized On-Resistance



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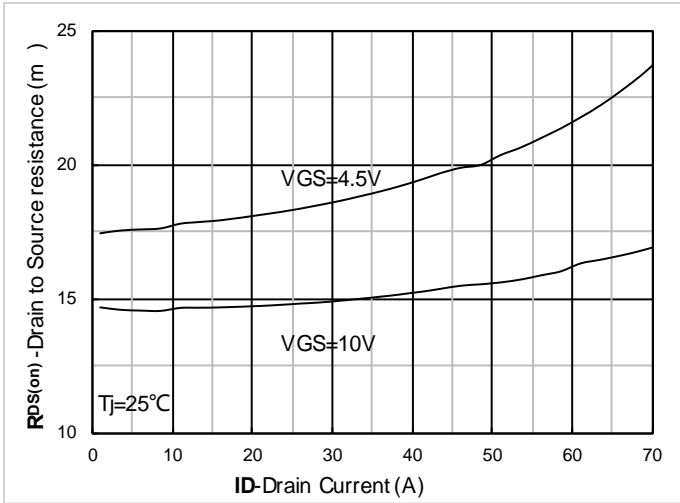


Figure 7. $R_{DS(on)}$ VS Drain Current

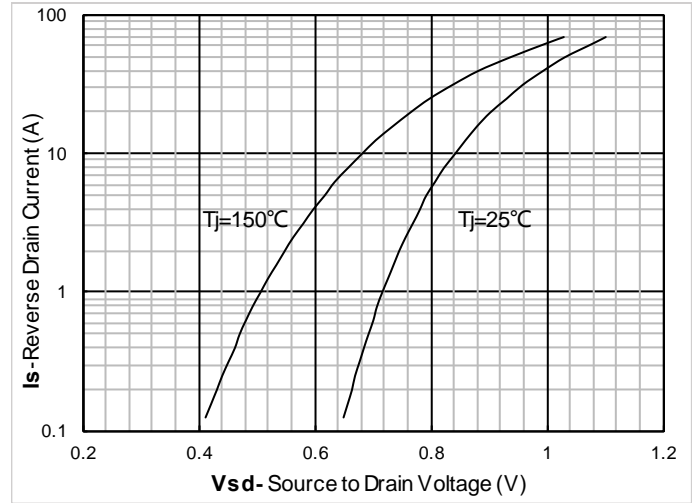


Figure 8. Forward characteristics of reverse diode

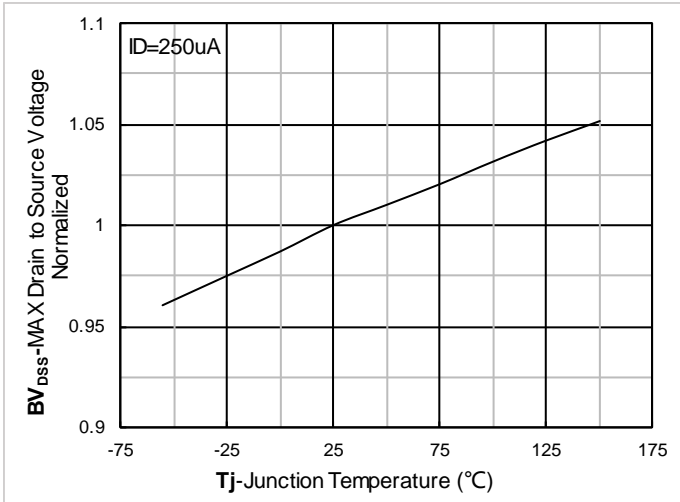


Figure 9. Normalized breakdown voltage

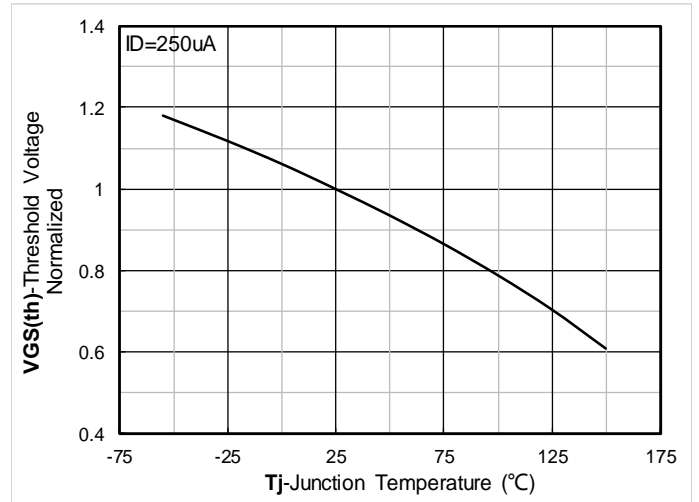


Figure 10. Normalized Threshold voltage

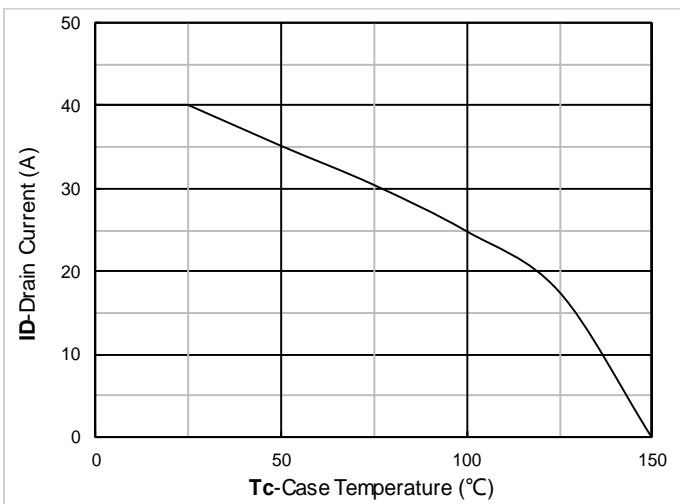


Figure 11. Current dissipation

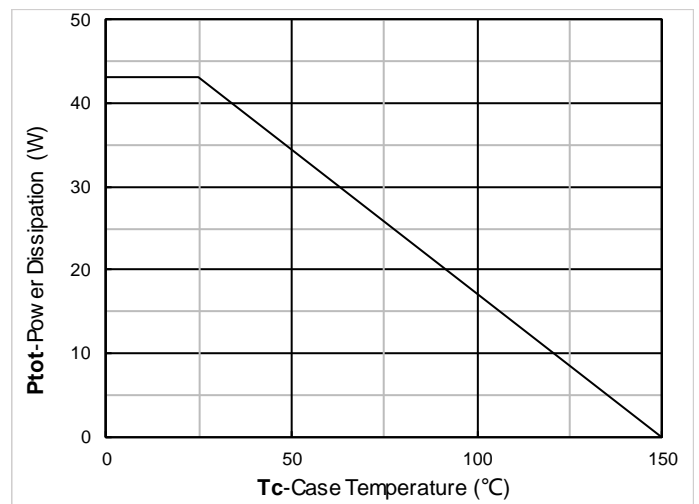


Figure 12. Power dissipation



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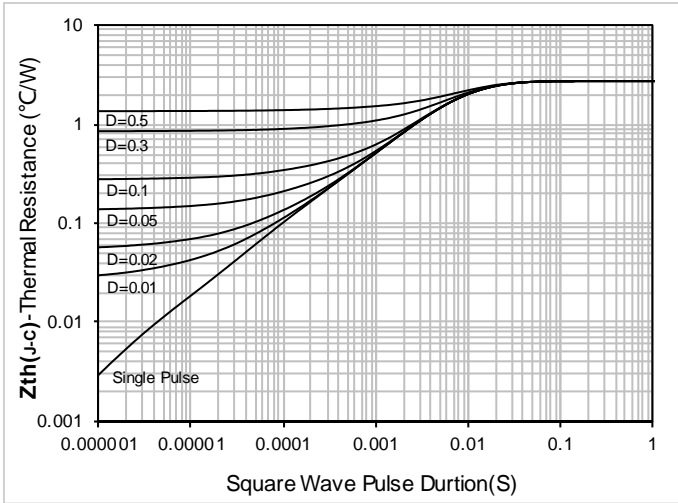


Figure 13. Maximum Transient Thermal Impedance

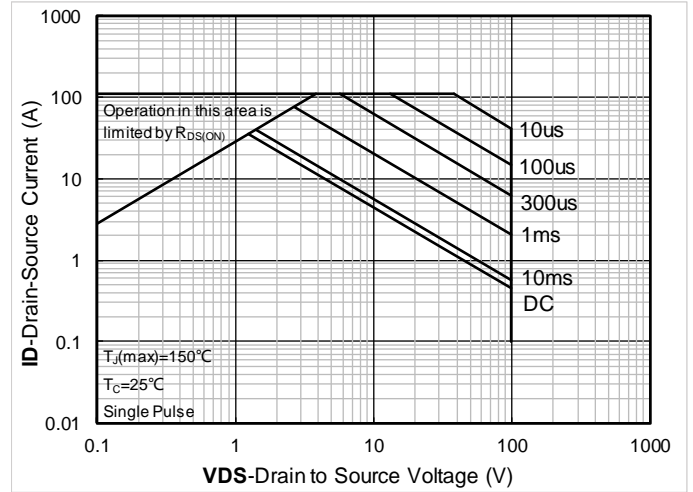


Figure 14. Safe Operation Area

Test Circuits & Waveforms

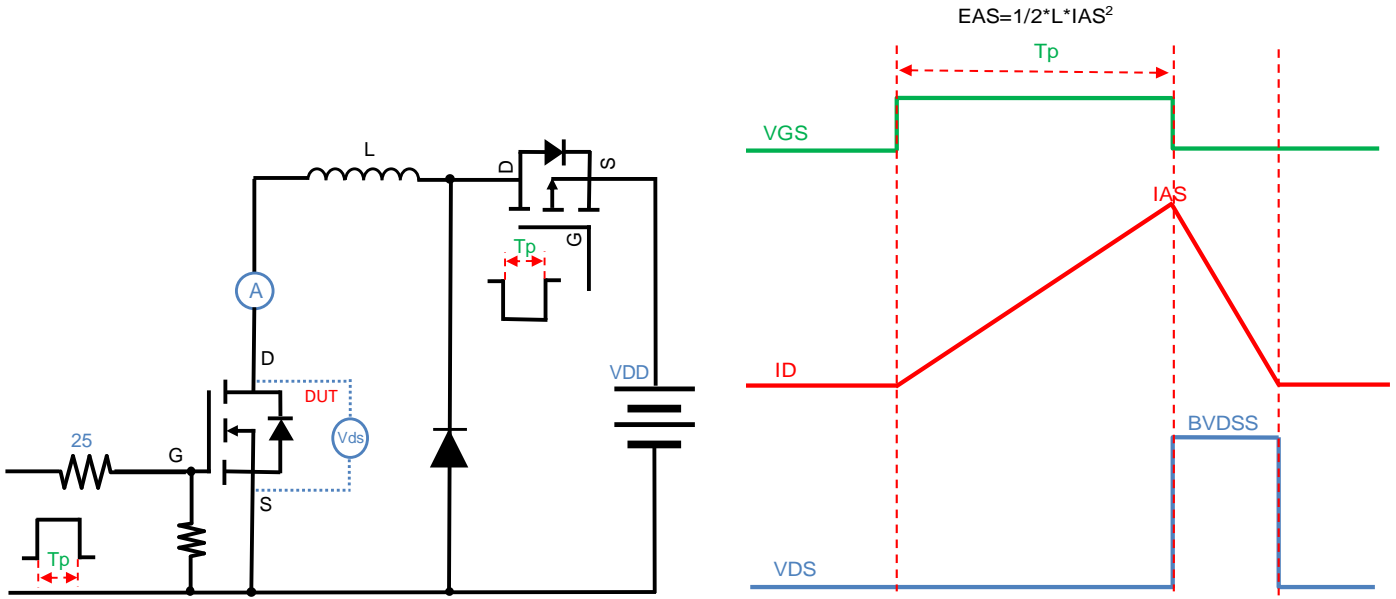


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

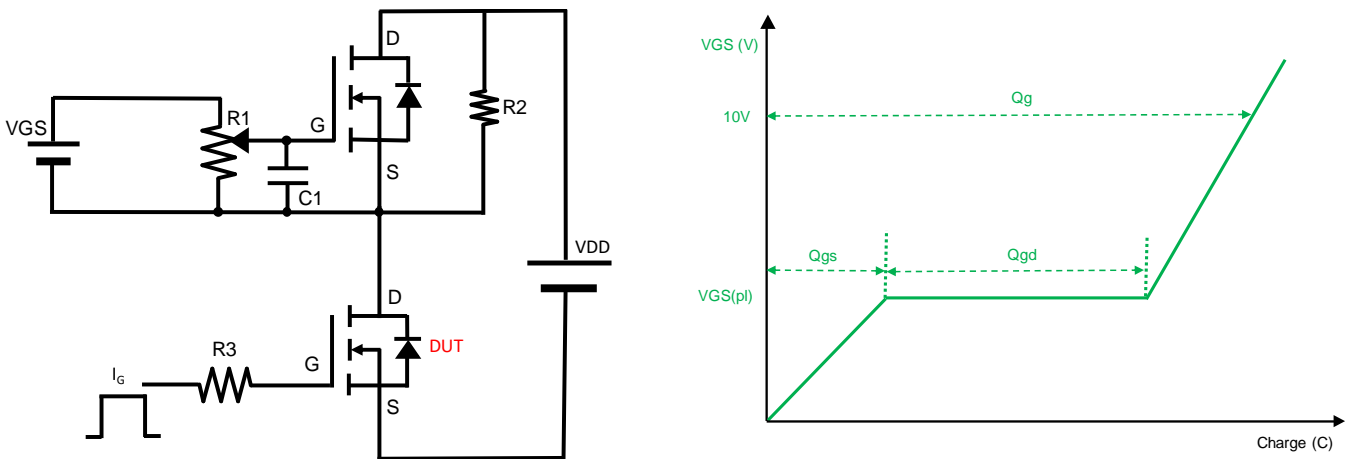


Figure B. Gate Charge Test Circuit & Waveform

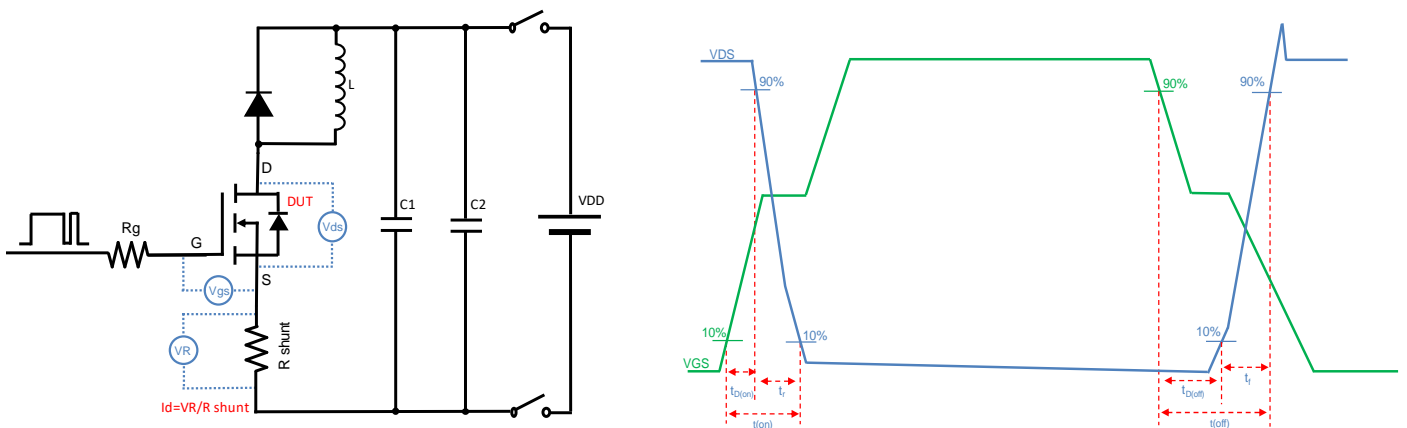


Figure C. Resistive Switching Test Circuit & Waveform

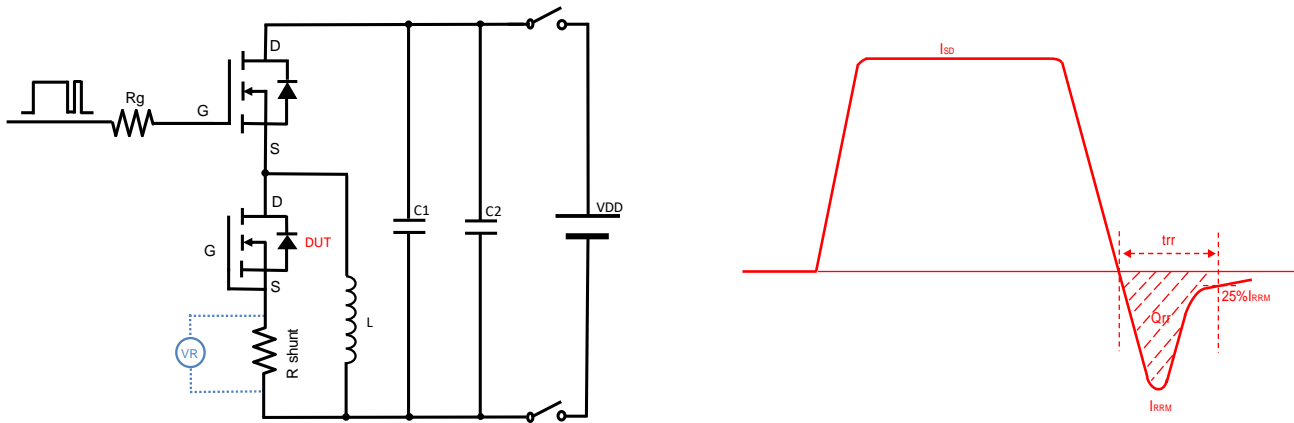
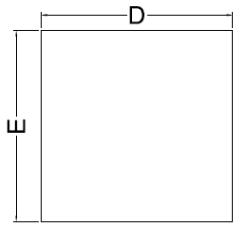


Figure D. Diode Recovery Test Circuit & Waveform

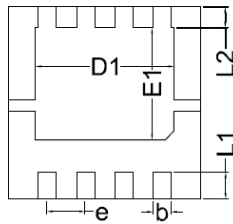


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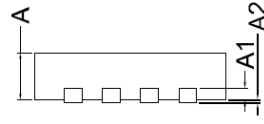
DFN3333-8L Package information



Top View
正面视图

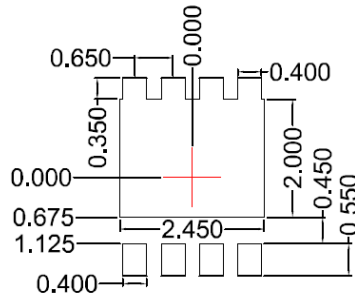


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout
Top View

- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.10\text{mm}$.
 3. The pad layout is for reference purposes only.



YJQ40G10AQ

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