



N-Channel and P-Channel Complementary MOSFET

Product Summary

NMOS

V_{DS}	30V
I_D	20A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	30m
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	50m

PMOS

V_{DS}	-30V
I_D	-20A
$R_{DS(ON)}$ (at $V_{GS}=-10V$)	40m
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	60m
100% EAS Tested	

General Description

High density cell design for low $R_{DS(ON)}$
 High Speed switching
 Moisture Sensitivity Level 3
 Epoxy Meets UL 94 V-0 Flammability Rating
 Halogen Free

Applications

Wireless charger
 Load switching
 Power management

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	NMOS	PMOS	Unit
Drain-source Voltage		V_{DS}	30	-30	V
Gate-source Voltage		V_{GS}	± 20	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	5	-5	A
	$T_A=100^\circ C$		3	-3	
	$T_C=25^\circ C$		20	-20	
	$T_C=100^\circ C$		12	-12	
Pulsed Drain Current ^A		I_{DM}	30	-40	A
Avalanche energy ^B		EAS	9	16	mJ
Total Power Dissipation ^C	$T_A=25^\circ C$	P_D	1.6	2	W
	$T_A=100^\circ C$		0.6	0.8	
	$T_C=25^\circ C$		16	27	
	$T_C=100^\circ C$		6	11	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	-55 +150	$^\circ C$

Thermal resistance

Parameter		Symbol	NMOS		PMOS		Units
			Typ	Max	Typ	Max	
Thermal Resistance Junction-to-Ambient ^D	Steady-State	R	60	75	50	62.5	/W
Thermal Resistance Junction-to-Case	Steady-State	R	6	7.5	3.5	4.5	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ3611B	F1	Q3611B	5000	10000	100000	1 reel



YJQ3611B

NMOS Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	
		V _{DS} =30V, V _{GS} =0V, T _J =150	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = 20V, V _{DS} =0V	-	-	100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250	1.0	1.5	2.2	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =10A	-	22	30	m
		V _{GS} =4.5V, I _D =3A	-	37	50	
Diode Forward Voltage	V _{SD}	I _S =10A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	8	-	
Maximum Body-Diode Continuous Current	I _S		-	-	20	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHz	-	235	-	pF
Output Capacitance	C _{oss}		-	43	-	
Reverse Transfer Capacitance	C _{rss}		-	35	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =4A	-	6	-	nC
Gate-Source Charge	Q _{gs}		-	1.25	-	
Gate-Drain Charge	Q _{gd}		-	1.3	-	
Reverse Recovery Charge	Q _{rr}	I _F =4A, di/dt=100A/us	-	1.7	-	nC
Reverse Recovery Time	t _{rr}		-	17	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =15V, I _D =4A R _{GEN} =	-	4	-	ns
Turn-on Rise Time	t _r		-	23	-	
Turn-off Delay Time	t _{D(off)}		-	7	-	
Turn-off fall Time	t _f		-	19	-	



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PMOS Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250$	-30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1	
		$V_{DS}=-30V, V_{GS}=0V, T_J=150$	-	-	-100	
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250$	-1.0	-1.5	-2.4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-10A$	-	31	40	m
		$V_{GS}=-4.5V, I_D=-5A$	-	45	60	
Diode Forward Voltage	V_{SD}	$I_S=-10A, V_{GS}=0V$	-	-	-1.2	V
Gate resistance	R_G	$f=1MHz$	-	15	-	
Maximum Body-Diode Continuous Current	I_S		-	-	-20	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$	-	490	-	pF
Output Capacitance	C_{oss}		-	75	-	
Reverse Transfer Capacitance	C_{rss}		-	60	-	
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=-10V, V_{DS}=-15V, I_D=-10A$	-	9	-	nC
Gate-Source Charge	Q_{gs}		-	2.5	-	
Gate-Drain Charge	Q_{gd}		-	2.3	-	
Reverse Recovery Charge	Q_{rr}	$I_F=-10A, di/dt=100A/us$	-	15	-	nC
Reverse Recovery Time	t_{rr}		-	35	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=-10V, V_{DD}=-15V, I_D=-10A$ $R_{GEN}=2.5$	-	9	-	ns
Turn-on Rise Time	t_r		-	3.5	-	
Turn-off Delay Time	$t_{D(off)}$		-	30	-	
Turn-off fall Time	t_f		-	18	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. NMOS: $T_J=25^\circ C, V_{DD}=25V, V_{GS}=10V, R_G=0.5mH, I_{AS}=6A$.
PMOS: $T_J=25^\circ C, V_{DD}=-25V, V_{GS}=-10V, R_G=0.5mH, I_{AS}=-8A$.

C. P_d is based on max. junction temperature, using junction-case thermal resistance.

D. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in the still air environment with $T_A=25^\circ C$.
The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



NMOS Typical Electrical and Thermal Characteristics Diagrams

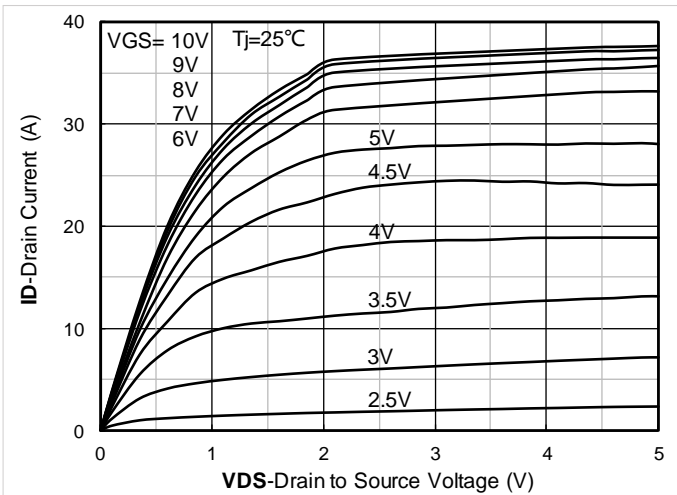


Figure 1. Output Characteristics

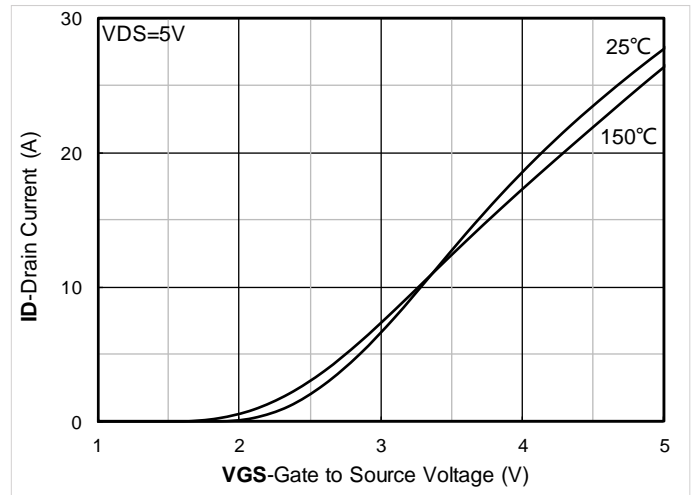


Figure 2. Transfer Characteristics

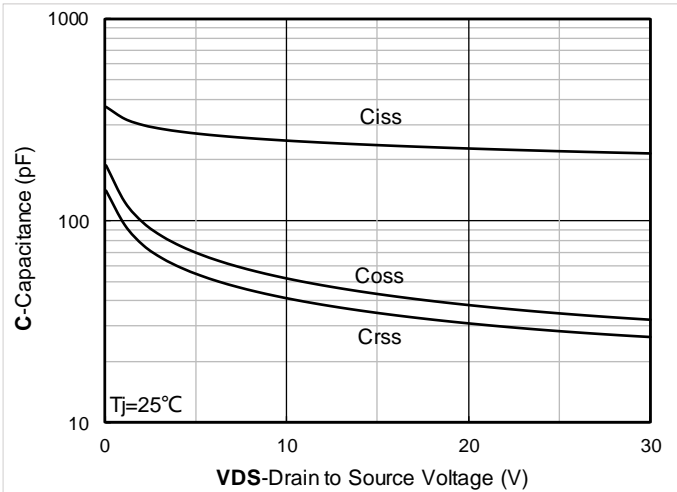


Figure 3. Capacitance Characteristics

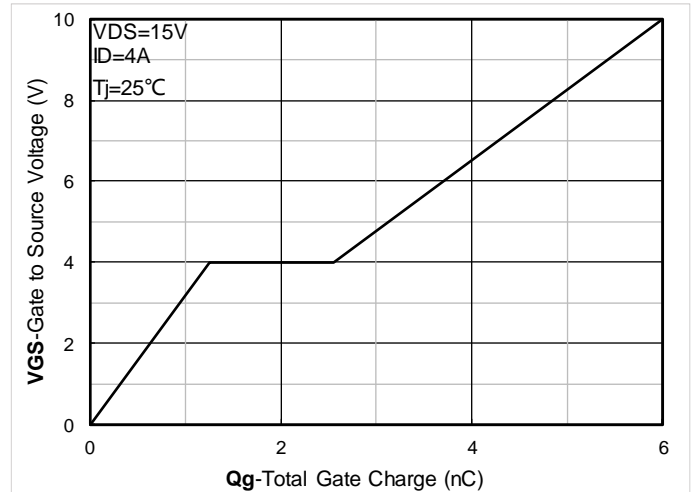


Figure 4. Gate Charge

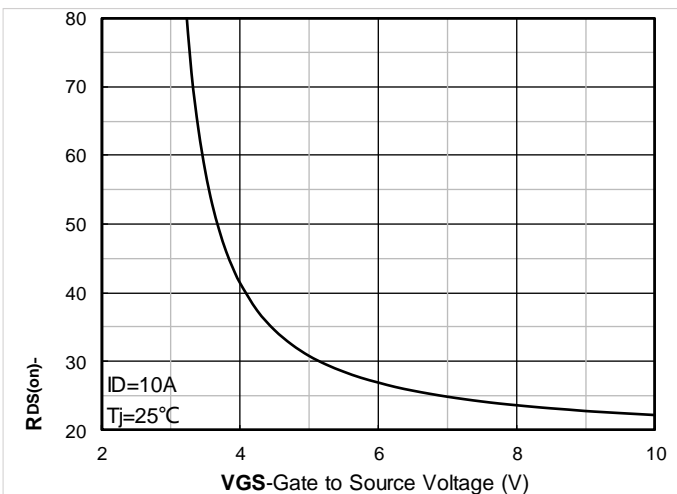


Figure 5. On-Resistance VS Gate to Source Voltage

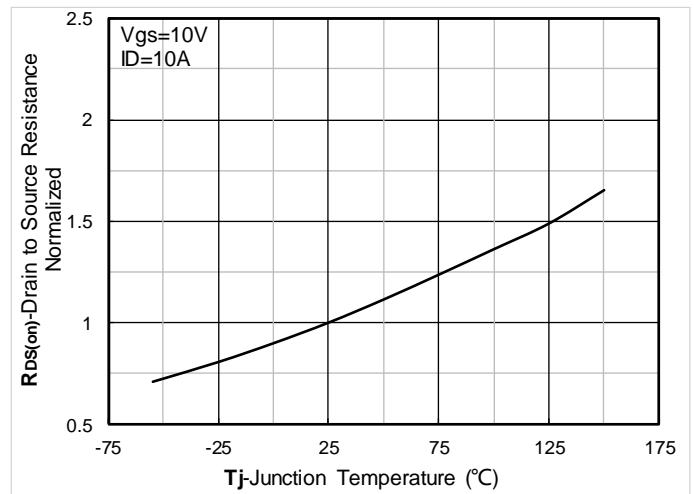


Figure 6. Normalized On- Resistance

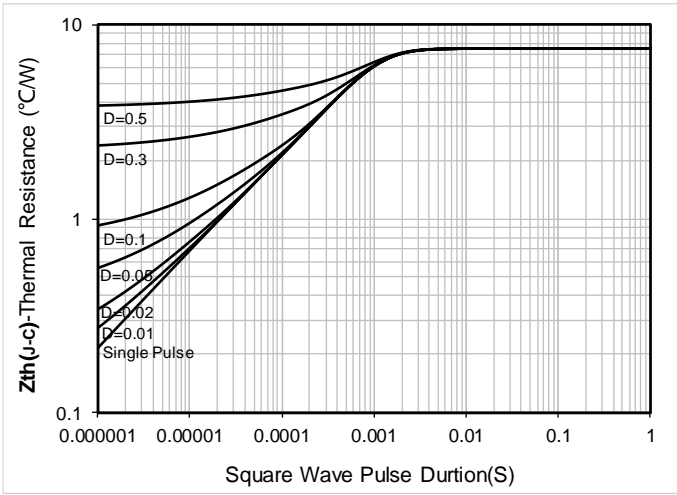


Figure 13. Maximum Transient Thermal Impedance

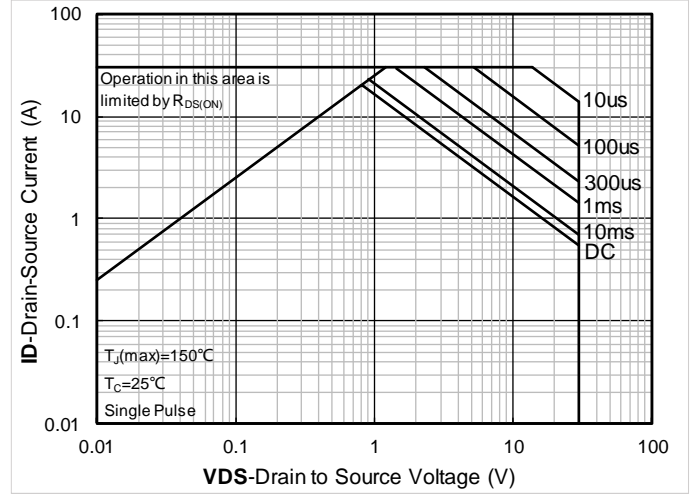


Figure 14. Safe Operation Area

PMOS Typical Electrical and Thermal Characteristics Diagrams

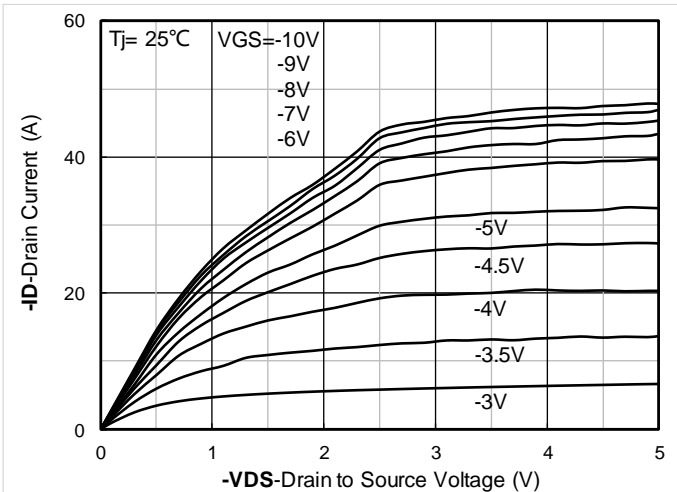


Figure 1. Output Characteristics

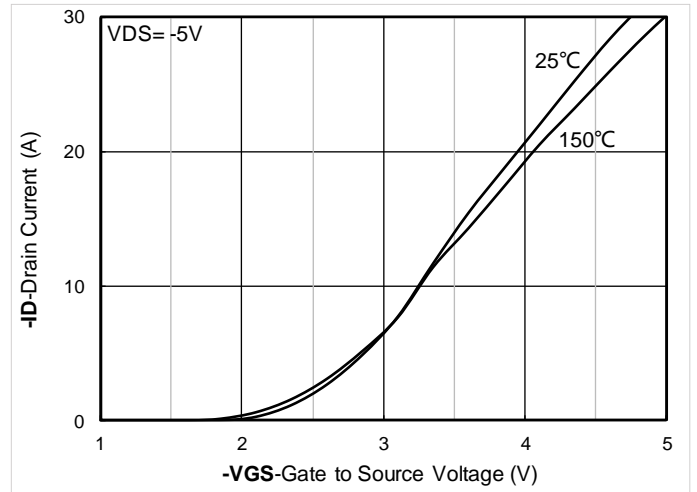


Figure 2. Transfer Characteristics

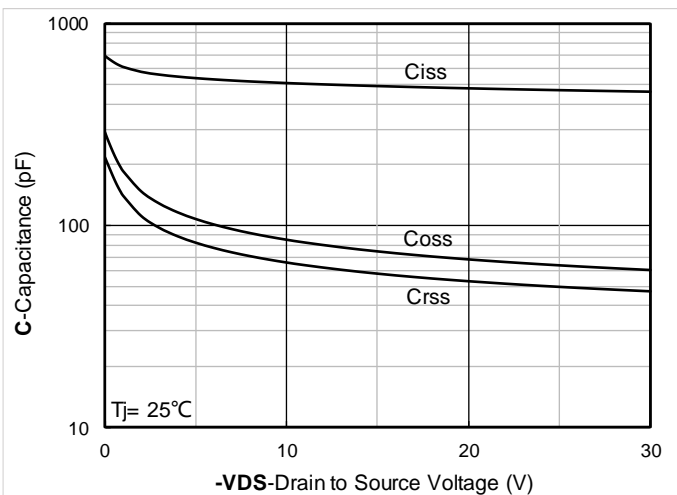


Figure 3. Capacitance Characteristics

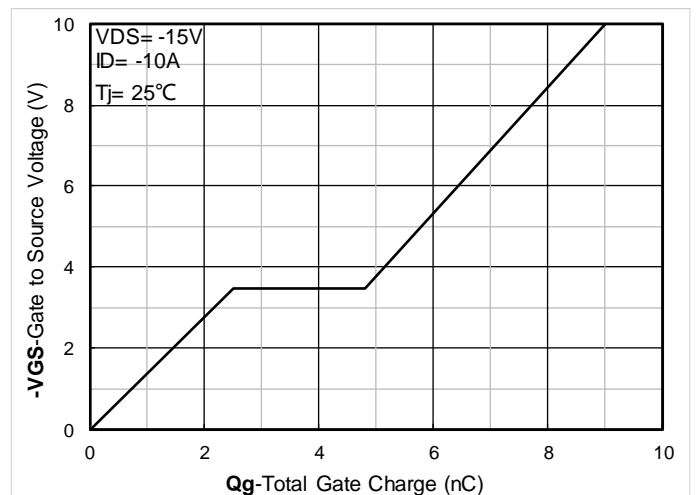


Figure 4. Gate Charge



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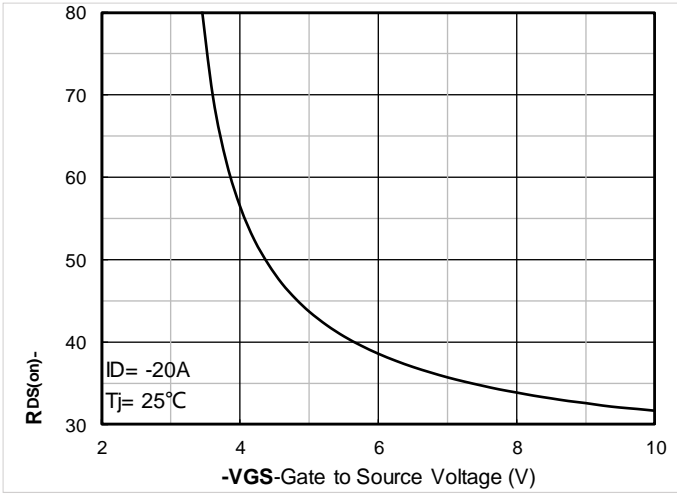


Figure 5. On-Resistance vs Gate to Source Voltage

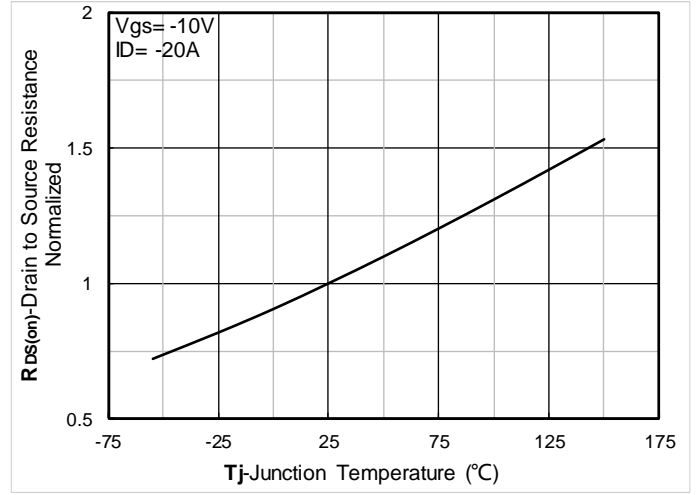


Figure 6. Normalized On-Resistance

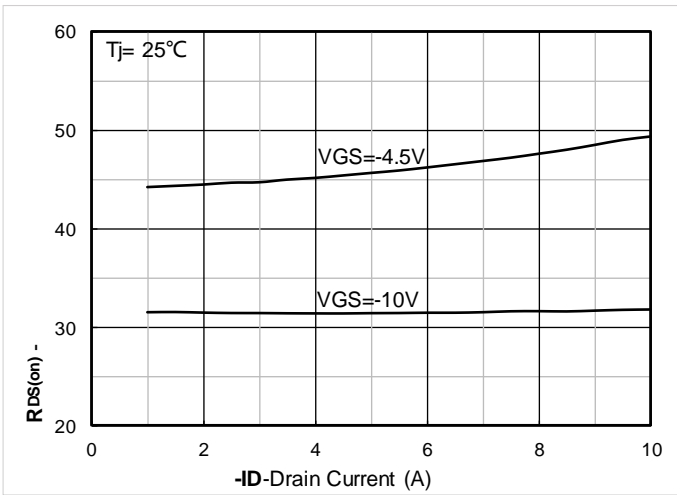


Figure 7. RDS(on) VS Drain Current

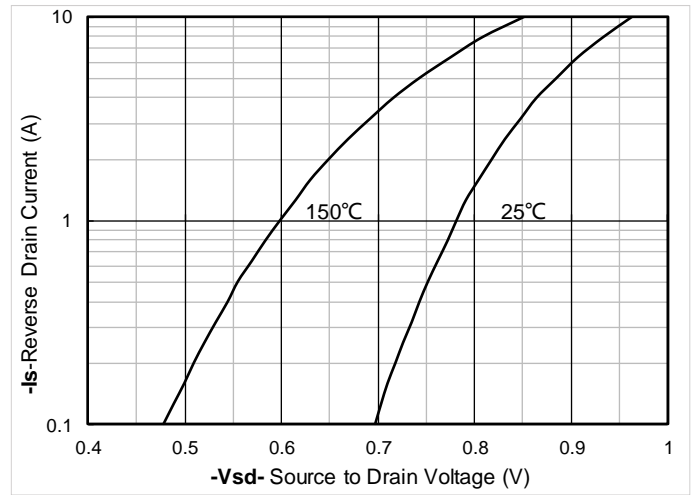


Figure 8. Forward characteristics of reverse diode

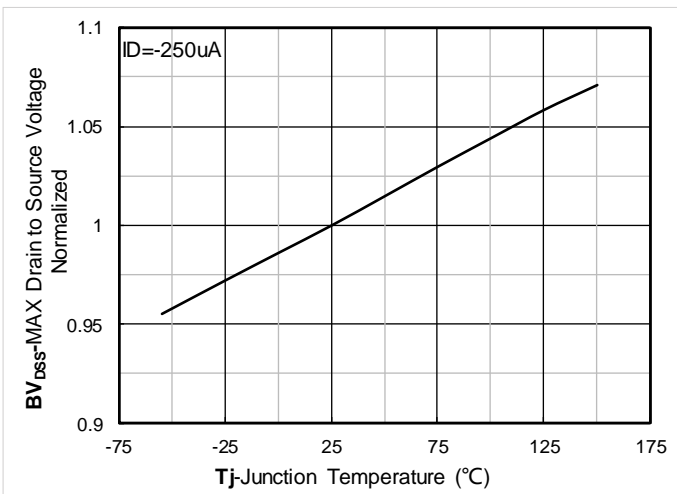


Figure 9. Normalized breakdown voltage

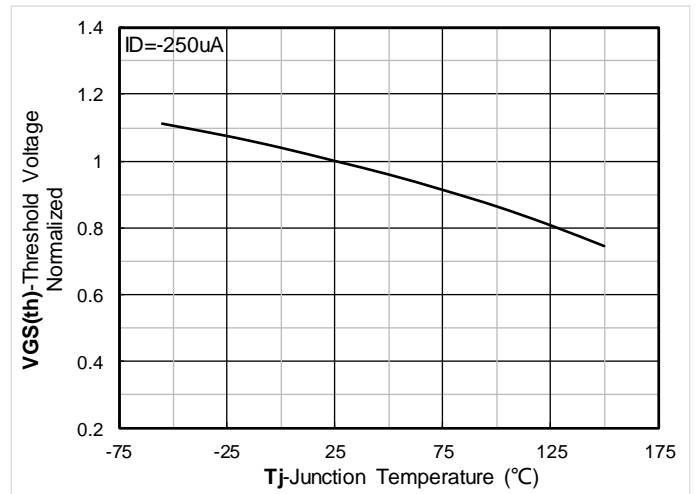


Figure 10. Normalized Threshold voltage

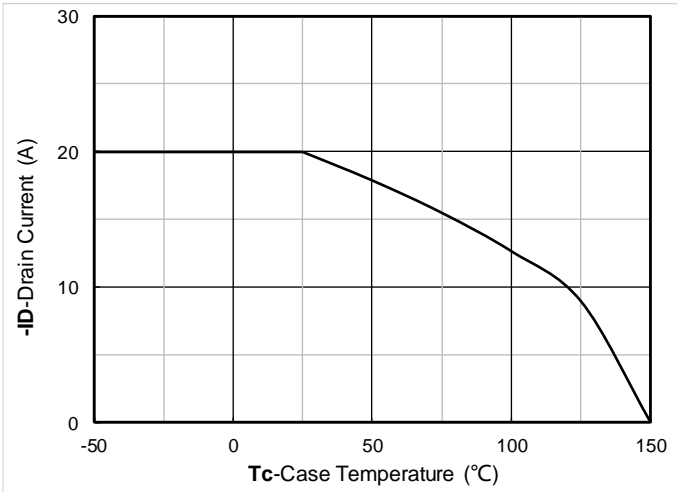


Figure 11. Current dissipation

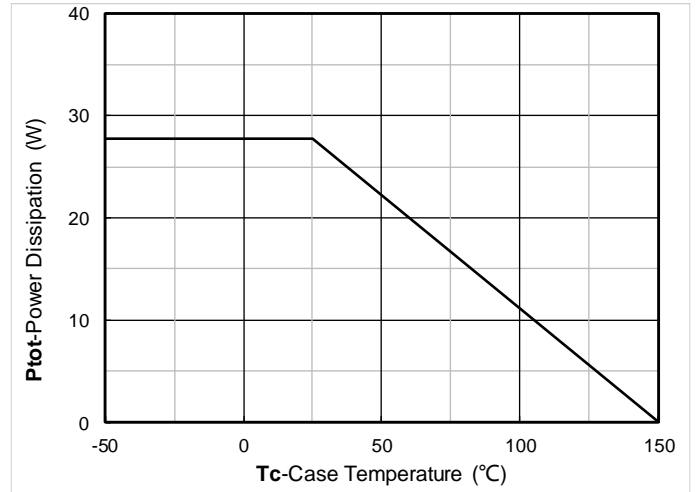


Figure 12. Power dissipation

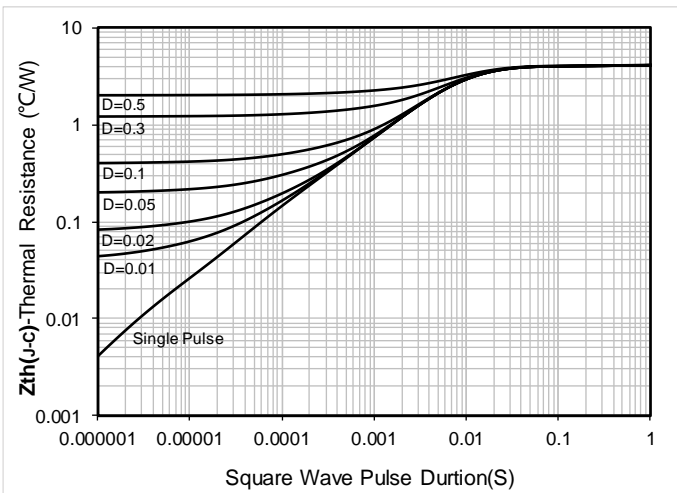


Figure 13. Maximum Transient Thermal Impedance

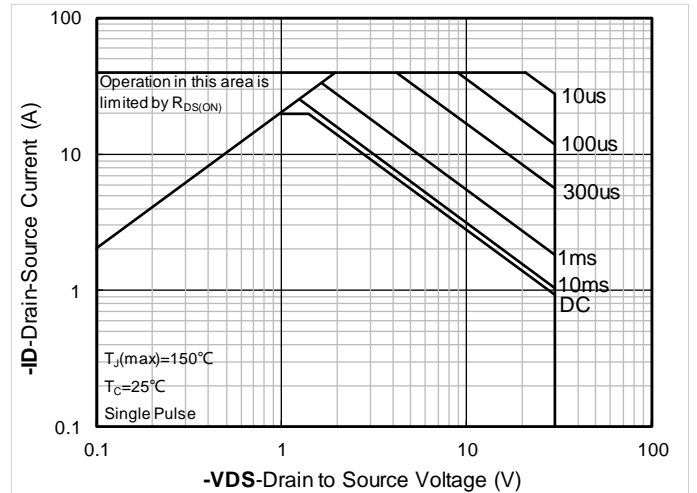
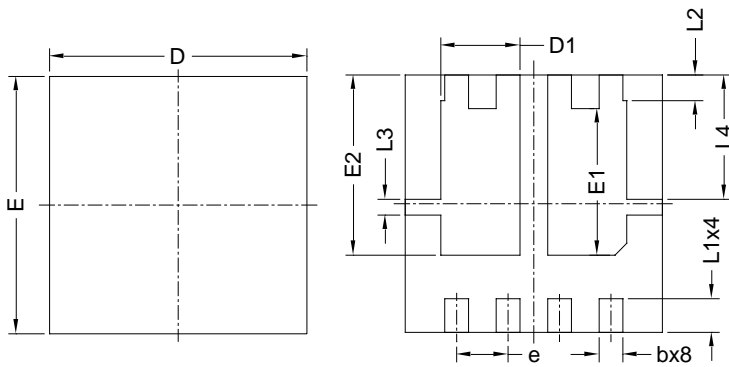


Figure 14. Safe Operation Area



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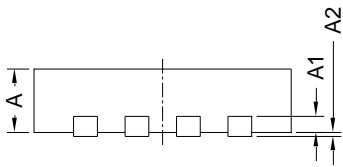
DFN3333-8L-B-0.8MM Package information



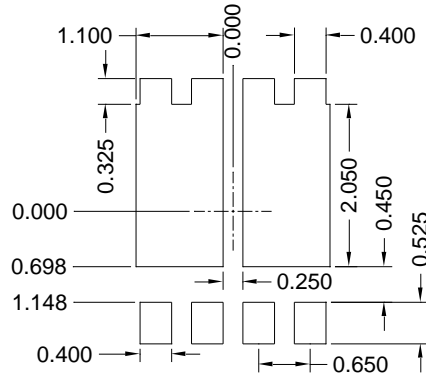
Top View

Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	0.90	1.00	1.10
E1	1.75	1.85	1.95
E2	2.175	2.275	2.375
L1	0.325	0.425	0.525
L2	0.325 BSC		
L3	0.200 BSC		
L4	1.570 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Side View



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



YJQ3611B

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