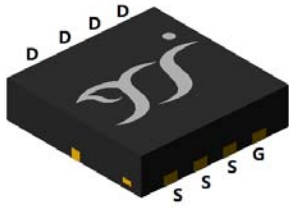
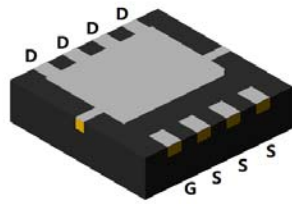


## N-Channel Enhancement Mode Field Effect Transistor

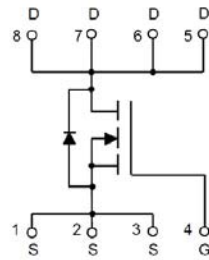


Top View



Bottom View

DFN3333-8L



### Product Summary

- $V_{DS}$  40V
- $I_D$  20A
- $R_{DS(ON)}$ ( at  $V_{GS}=10V$ ) 15.0m $\Omega$
- $R_{DS(ON)}$ ( at  $V_{GS}=4.5V$ ) 20.0m $\Omega$
- 100% EAS Tested

### General Description

- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Part no. with suffix "Q" means AEC-Q101 qualified

### Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- 12V Automotive systems

### ■ Absolute Maximum Ratings ( $T_A=25$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	40	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current	$I_D$	$T_C=25$	20
		$T_C=100$	17
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	80	A
Avalanche energy <sup>B</sup>	EAS	40	mJ
Total Power Dissipation <sup>C</sup>	$P_D$	$T_A=25$	2.2
		$T_C=25$	21
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	5.9
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State	$R_{\theta JA}$	55
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 +150	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ20N04AQ	F1	Q20N04	5000	10000	100000	13" reel



# YJQ20N04AQ

## ■ Electrical Characteristics ( $T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	11	15	m $\Omega$
		$V_{GS}=4.5V, I_D=10A$	-	15	20	
Diode Forward Voltage	$V_{SD}$	$I_S=20A, V_{GS}=0V$	-	0.85	1.2	V
Gate resistance	$R_G$	f=1MHz, Open drain	-	3.5	-	$\Omega$
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V, f=1MHz$	-	1050		pF
Output Capacitance	$C_{oss}$		-	130		
Reverse Transfer Capacitance	$C_{rss}$		-	100		
<b>Switching Parameters</b>						
Total Gate Charge	$Q_g$	$V_{GS}=10V, V_{DS}=20V, I_D=20A$	-	23	-	nC
Gate-Source Charge	$Q_{gs}$		-	3.5	-	
Gate-Drain Charge	$Q_{gd}$		-	7	-	
Reverse Recovery Charge	$Q_{rr}$	$I_F=20A, di/dt=300A/us$	-	11	-	nC
Reverse Recovery Time	$t_{rr}$		-	13	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=20V, I_{DS}=20A$	-	4	-	ns
Turn-on Rise Time	$t_r$		-	57.5	-	
Turn-off Delay Time	$t_{D(off)}$		-	20.2	-	
Turn-off fall Time	$t_f$		-	2.65	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B.  $V_{DD}=40V, V_G=10V, L=1mH, I_{AS}=9A$ .

C.  $P_d$  is based on max. junction temperature, using junction-case thermal resistance.

D. The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in the still air environment with  $T_A=25$ . The maximum allowed junction temperature of 150. The value in any given application depends on the user's specific board design..



# YJQ20N04AQ

## Typical Electrical and Thermal Characteristics Diagrams

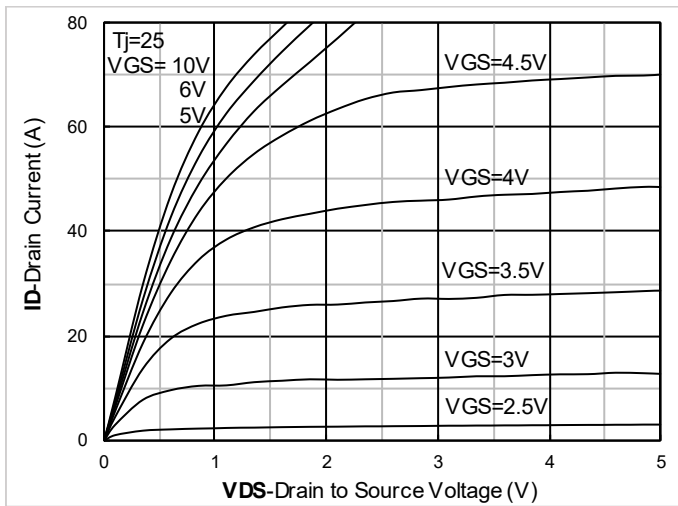


Figure 1. Output Characteristics

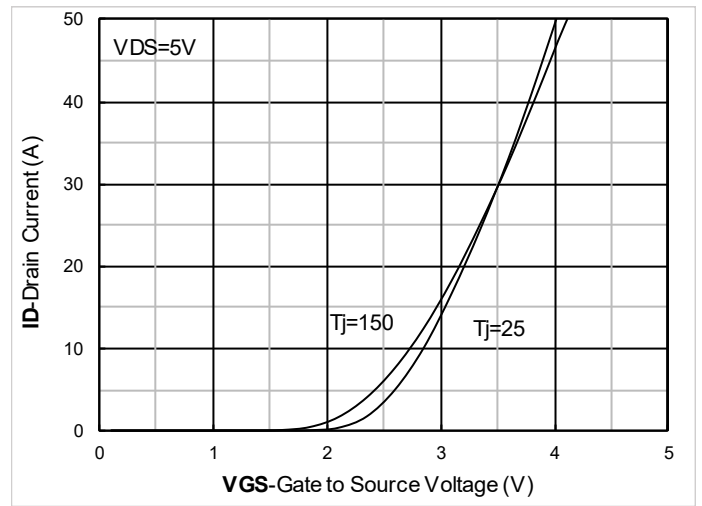


Figure 2. Transfer Characteristics

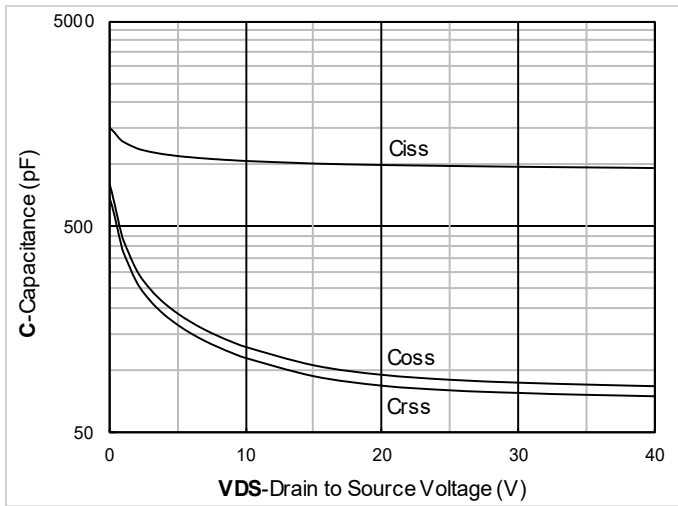


Figure 3. Capacitance Characteristics

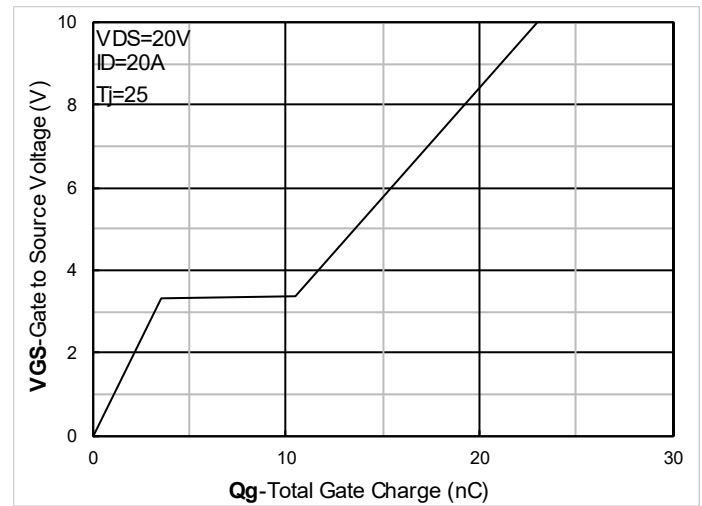


Figure 4. Gate Charge

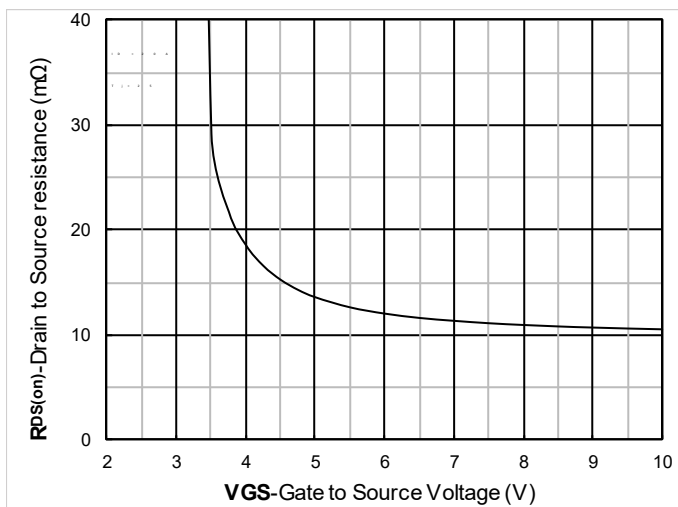


Figure 5. On-Resistance vs Gate to Source Voltage

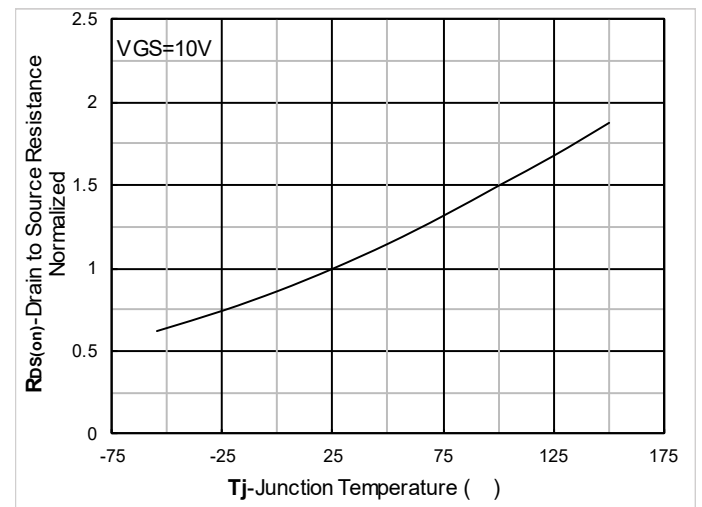


Figure 6. Normalized On-Resistance



# YJQ20N04AQ

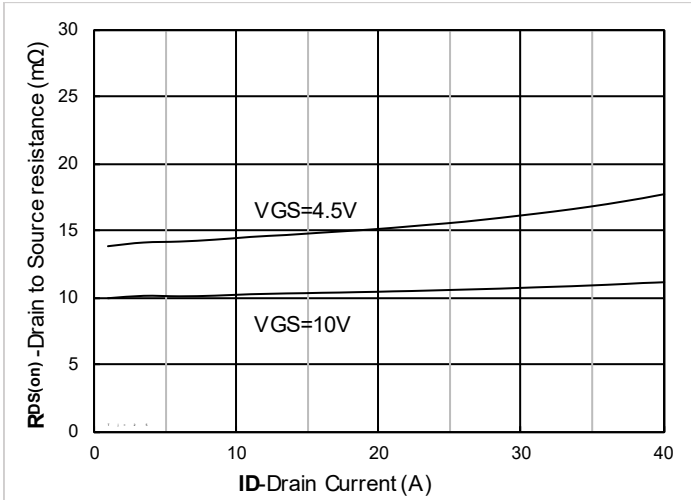


Figure 7. RDS(on) VS Drain Current

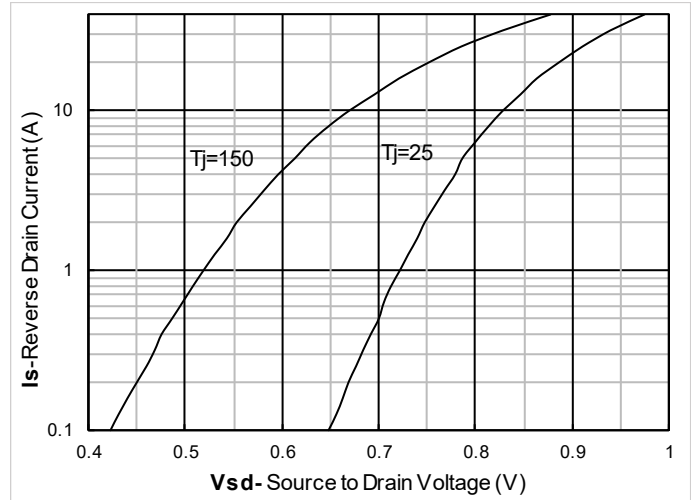


Figure 8. Forward characteristics of reverse diode

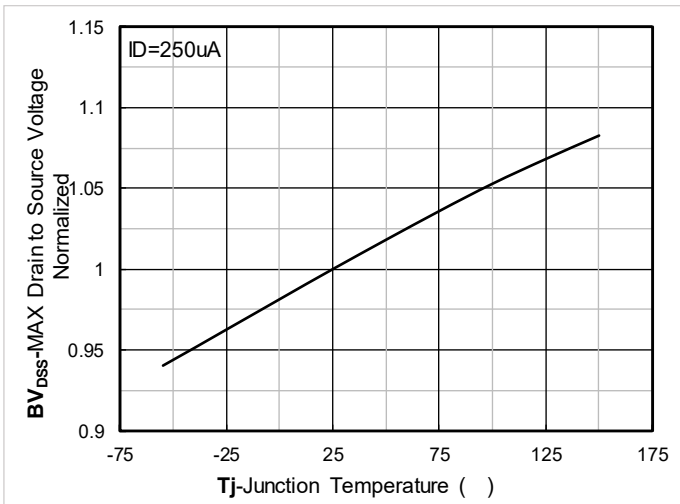


Figure 9. Normalized breakdown voltage

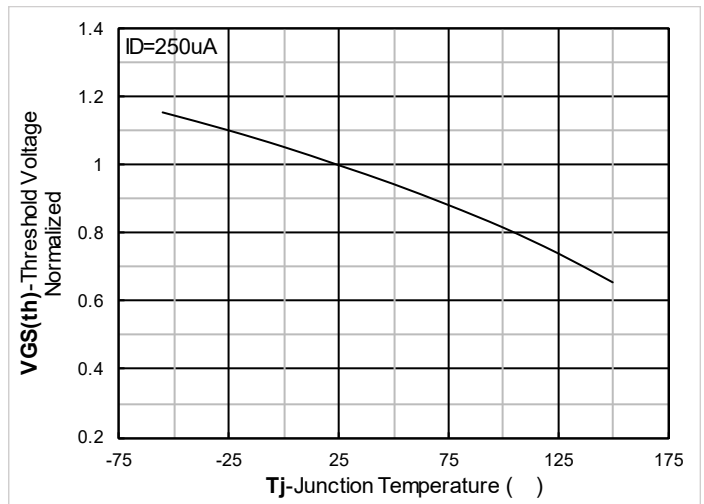


Figure 10. Normalized Threshold voltage

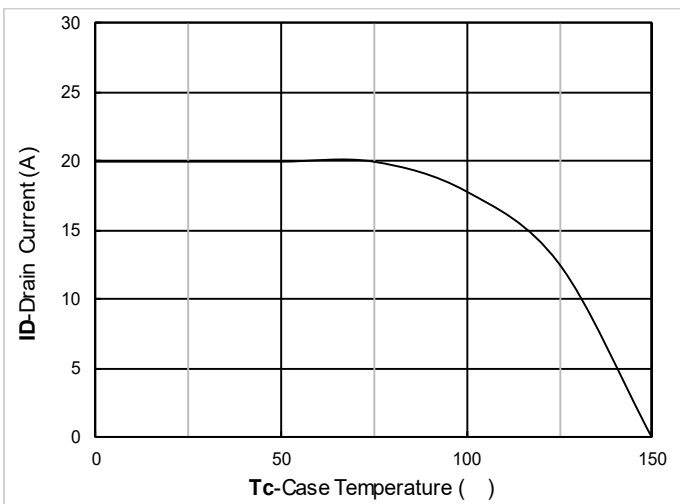


Figure 11. Current dissipation

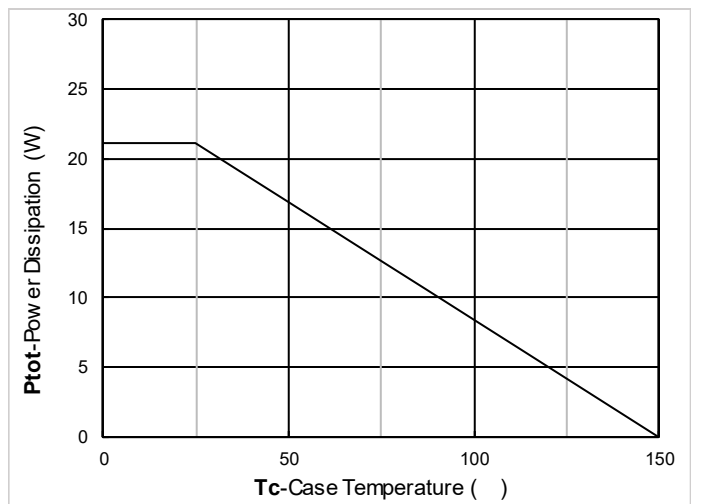


Figure 12. Power dissipation

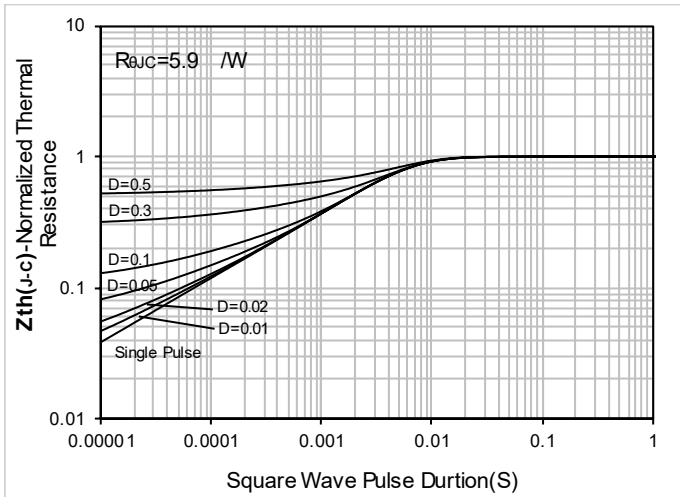


Figure 13. Maximum Transient Thermal Impedance

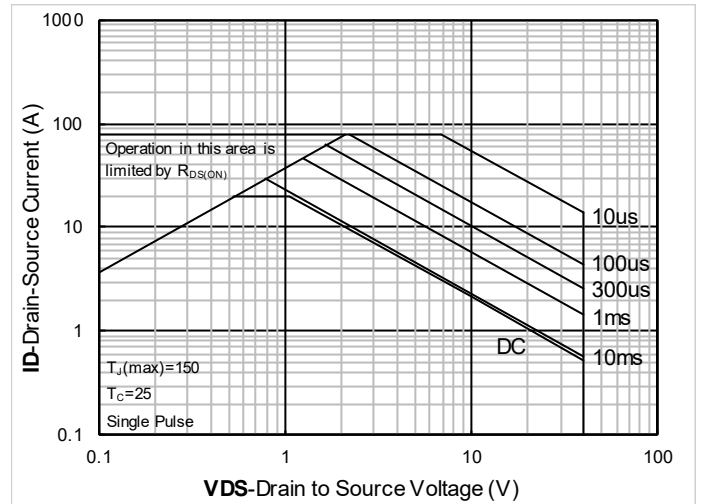
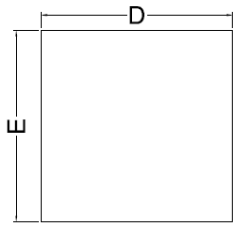


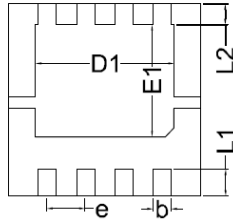
Figure 14. Safe Operation Area



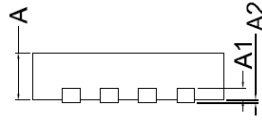
## DFN3333-8L Package information



Top View  
正面视图

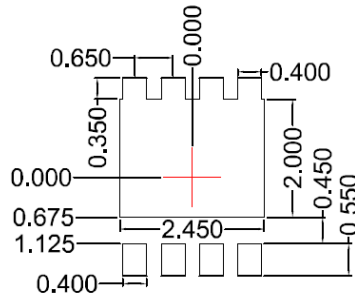


Bottom View  
背面视图



Side View  
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout  
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10\text{mm}$ .
3. The pad layout is for reference purposes only.



## YJQ20N04AQ

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