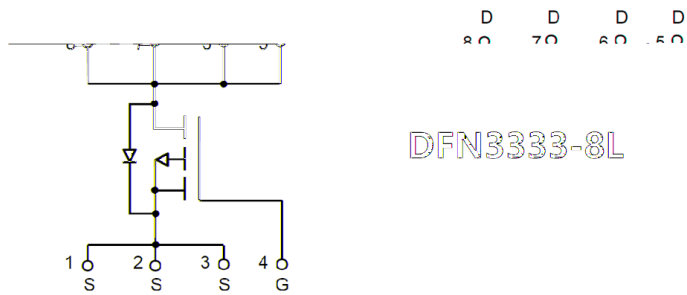
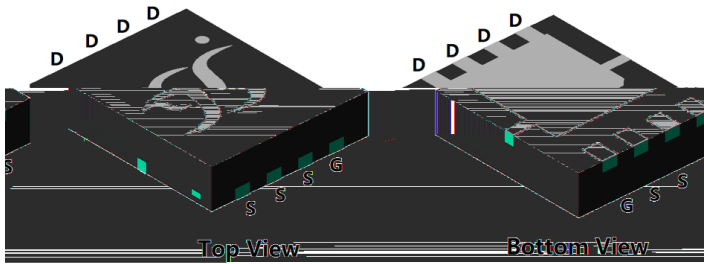


P-Channel Enhancement Mode Field Effect Transistor



Product Summary

V_{DS}	-100V
I_D	-15A
$R_{DS(ON)}$ (at $V_{GS}=-10V$)	< 110 mohm
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	< 120 mohm
100% EAS Tested	

General Description

Split gate trench MOSFET technology
 Excellent package for heat dissipation
 High density cell design for low $R_{DS(ON)}$
 Moisture Sensitivity Level 3
 Epoxy Meets UL 94 V-0 Flammability Rating
 Halogen Free

Applications

DC-DC Converters
 Power management functions

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	-4.5	A
	$T_A=100^\circ\text{C}$		-2.8	
	$T_C=25^\circ\text{C}$		-15	
	$T_C=100^\circ\text{C}$		-9.5	
Pulsed Drain Current ^A		I_{DM}	-45	A
Avalanche energy ^B		EAS	64	mJ
Total Power Dissipation ^C	$T_A=25^\circ\text{C}$	P_D	3	W
	$T_A=100^\circ\text{C}$		1.2	
	$T_C=25^\circ\text{C}$		43	
	$T_C=100^\circ\text{C}$		17.2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	$t \leq 10\text{S}$	R	20	25	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Ambient ^D	Steady-State		40	50	
Thermal Resistance Junction-to-Case	Steady-State		2.4	2.9	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ15GP10A	F1	Q15GP10A	5000	10000	100000	13 reel



YJQ15GP10A

Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250	-100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-100V, V _{GS} =0V	T _J =25°C		-1	
			T _J =55°C		-5	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250	-1.0	-1.8	-2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -10V, I _D =-10A		83	110	m
		V _{GS} = -4.5V, I _D =-5A		95	120	
Diode Forward Voltage	V _{SD}	I _S =-15A, V _{GS} =0V			-1.3	V
Maximum Body-Diode Continuous Current	I _S				-15	A
Gate resistance	R _g	f=1MHz		10		
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-50V, V _{GS} =0V, f=1MHz		1051		pF
Output Capacitance	C _{oss}			119		
Reverse Transfer Capacitance	C _{rss}			25		
Switching Parameters						
Total Gate Charge	Q _{g(-10V)}	V _{GS} =-10V, V _{DS} =-50V, I _D =-5A		20.1		nC
Total Gate Charge	Q _{g(-4.5V)}			9.7		
Gate-Source Charge	Q _{gs}			3.98		
Gate-Drain Charge	Q _{gd}			4.38		
Reverse Recovery Charge	Q _{rr}	I _F =-5A, di/dt=100A/us		140		nC
Reverse Recovery Time	t _{rr}			80		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DD} =-50V, I _{DS} =-5A R _{GEN} =6		10		ns
Turn-on Rise Time	t _r			30		
Turn-off Delay Time	t _{D(off)}			77		
Turn-off fall Time	t _f			81		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T_J=25°C, V_{DD}=-50V, V_G=-10V, R_G, I_{AS}=-16A.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. -4 board with 2oz. Copper, in a still air environment with T_A=25° C. The allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.



YJQ15GP10A

Typical Performance Characteristics

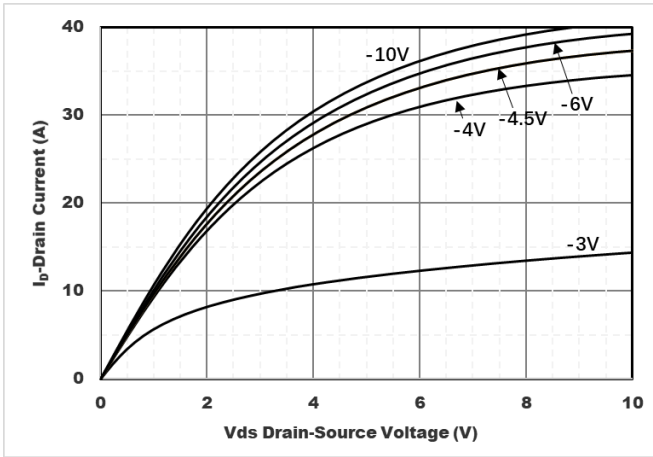


Figure1. Output Characteristics

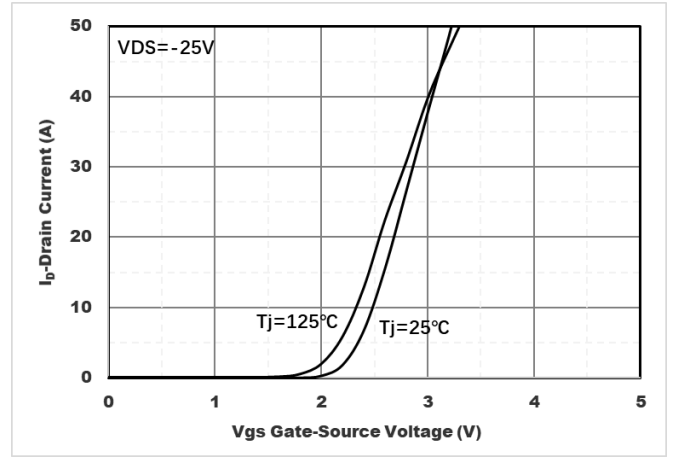


Figure2. Transfer Characteristics

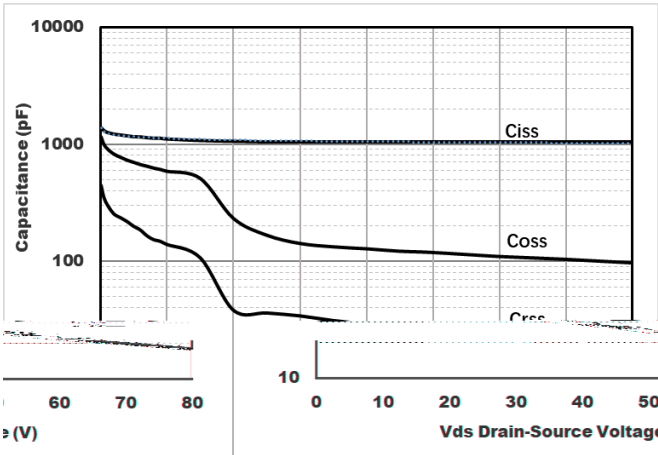


Figure3. Capacitance Characteristics

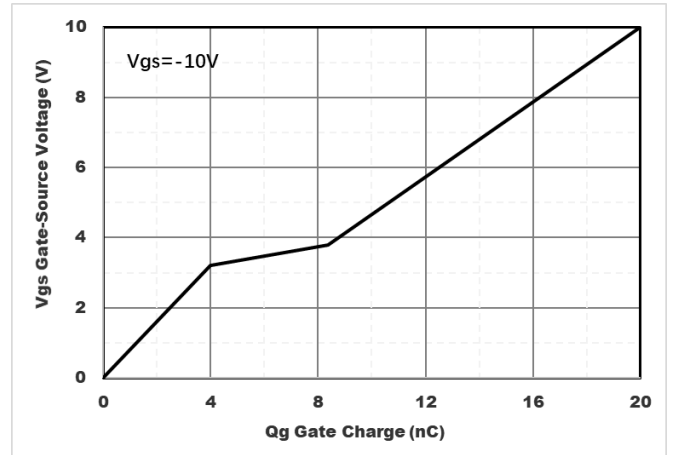


Figure4. Gate Charge

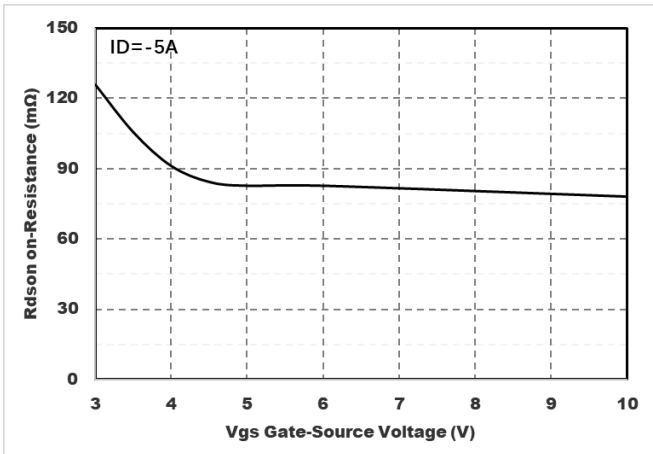


Figure5. : On-Resistance vs. Gate to Source Voltage

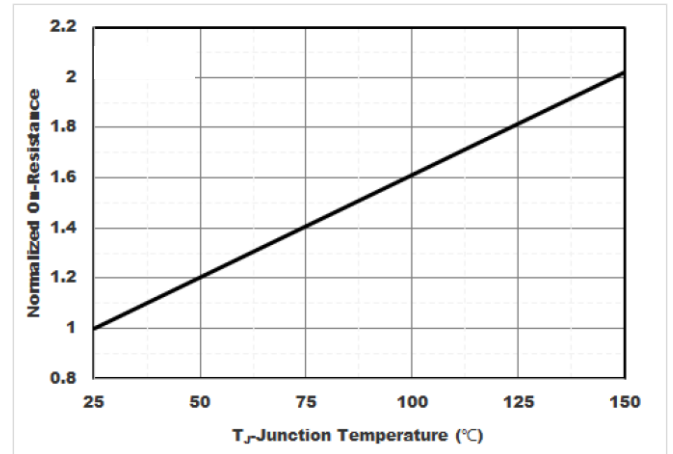


Figure6. Normalized On-Resistance



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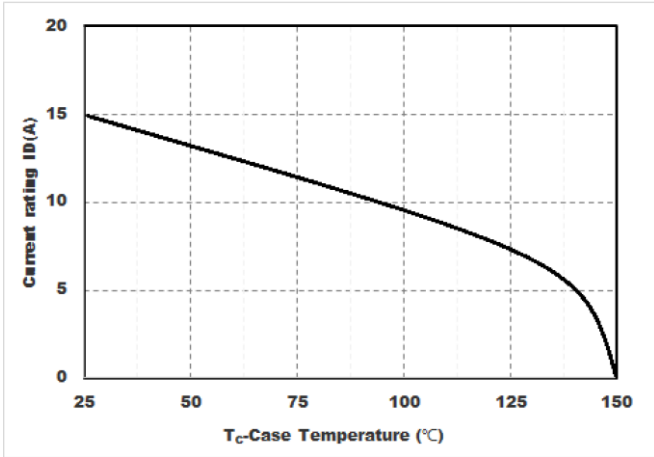


Figure7. Drain current

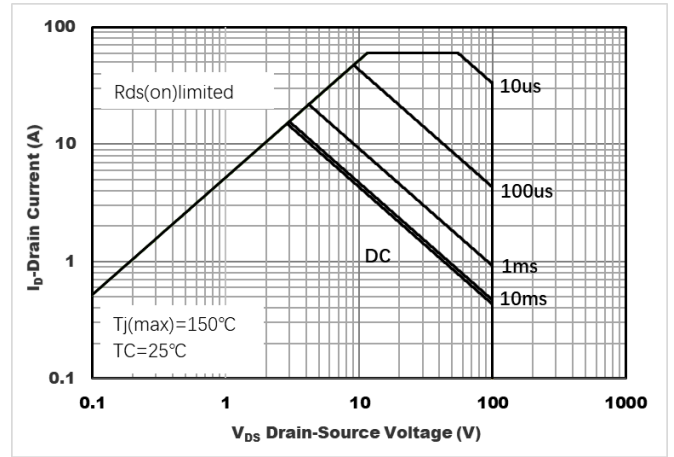


Figure8.Safe Operation Area

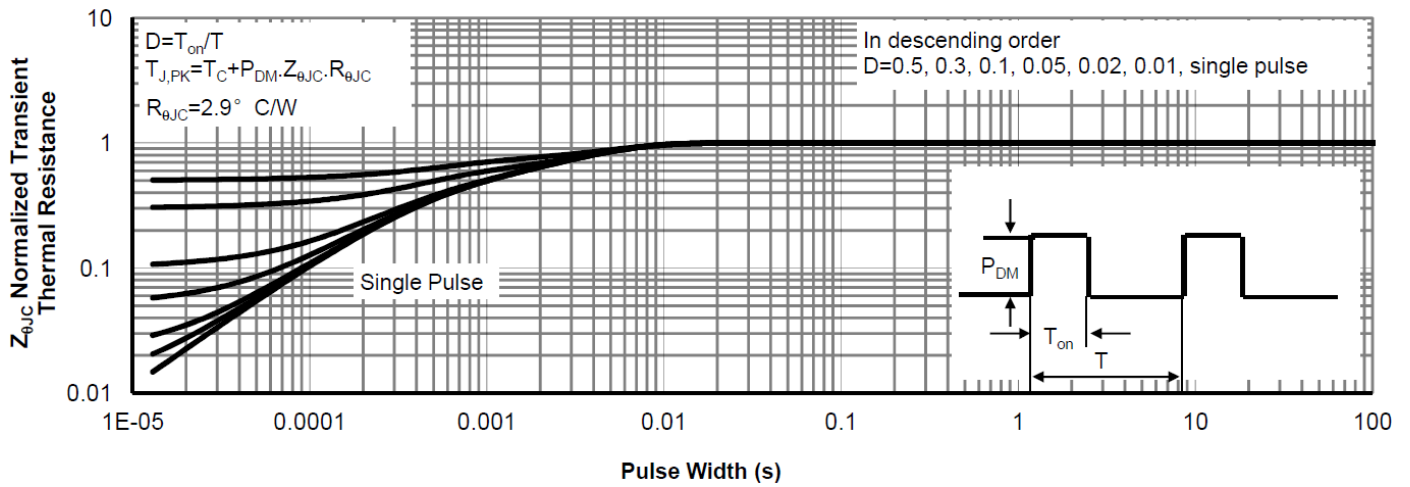


Figure9.Normalized Maximum Transient thermal impedance

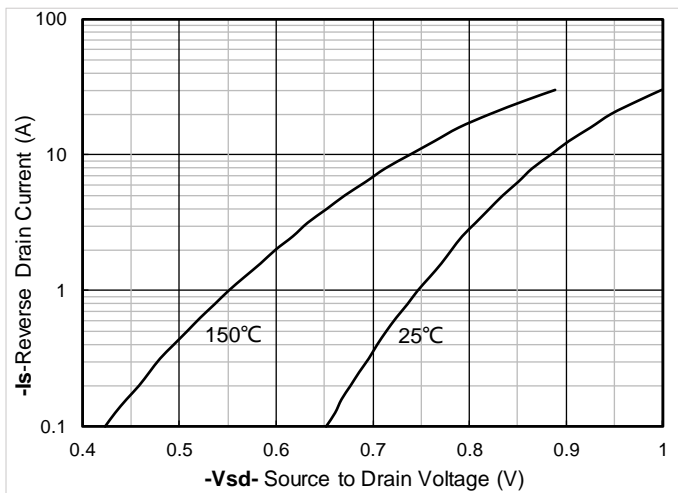
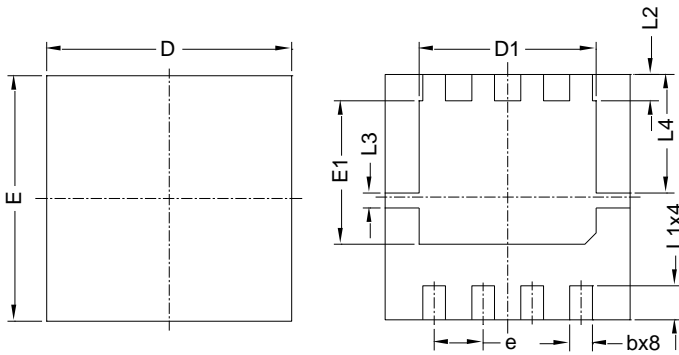


Figure 10. Forward characteristics of reverse diode



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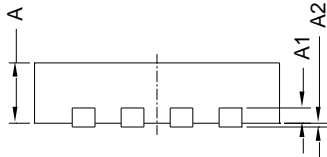
DFN3333-8L-A-0.8MM Package Information



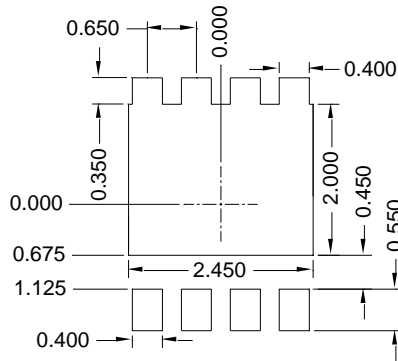
Top View
正面视图

Bottom View
背面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
L3	0.20 BSC		
L4	1.57 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Side View
侧面视图



Suggested Solder Pad Layout
Top View

Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.10\text{mm}$.
 3. The pad layout is for reference purposes only.



YJQ15GP10A

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