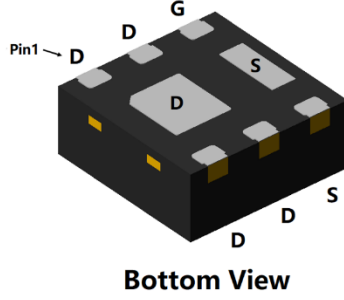
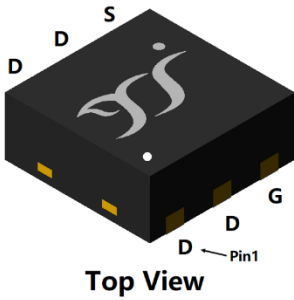
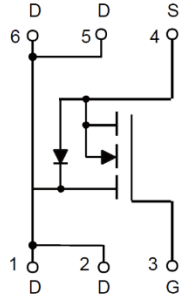


## N-Channel Enhancement Mode Field Effect Transistor



**DFN2020-6L**



### Product Summary

$V_{DS}$	30V
$I_D$	10A
$R_{DS(ON)}$ ( at $V_{GS}=4.5V$ )	28m
$R_{DS(ON)}$ ( at $V_{GS}=2.5V$ )	35m
$R_{DS(ON)}$ ( at $V_{GS}=1.8V$ )	45m

### General Description

Split gate trench MOSFET technology  
Excellent package for heat dissipation  
High density cell design for low  $R_{DS(ON)}$

UL 94 V-0 Flammability Rating

### Applications

Power switching application  
Uninterruptible power supply  
DC-DC convertor

### Absolute Maximum Ratings ( $T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	30	V
Gate-source Voltage		$V_{GS}$	$\pm 12$	V
Drain Current	$T_A=25^\circ C$	$I_D$	5	A
	$T_A=100^\circ C$		3	
	$T_C=25^\circ C$		10	
	$T_C=100^\circ C$		6	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	40	A
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ C$	$P_D$	1.5	W
	$T_A=100^\circ C$		0.6	
	$T_C=25^\circ C$		16	
	$T_C=100^\circ C$		6.5	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 +150	$^\circ C$

### Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State	R	65	80	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	R	6	7.5	

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ10N03A	F1	Q10N03	3000	30000	120000	



# YJQ10N03A

## Electrical Characteristics ( $T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D$	30	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=30V, V_{GS}=0V$	-	-	1	
		$V_{DS}=30V, V_{GS}=0V, T_J=150^\circ C$	-	-	100	
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D$	0.45	0.7	1	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=10A$	-	20	28	
		$V_{GS}=2.5V, I_D=8A$	-	25	35	
		$V_{GS}=1.8V, I_D=6A$	-	32	45	
Diode Forward Voltage	$V_{SD}$	$I_S=10A, V_{GS}=0V$	-	0.9	1.2	V
Gate resistance	$R_G$	$f=1MHz, \text{Open drain}$	-	3	-	
Maximum Body-Diode Continuous Current	$I_S$		-	-	10	A
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	-	520	-	pF
Output Capacitance	$C_{oss}$		-	60	-	
Reverse Transfer Capacitance	$C_{rss}$		-	50	-	
<b>Switching Parameters</b>						
Total Gate Charge	$Q_g$	$V_{GS}=10V, V_{DS}=15V, I_D=10A$	-	16.5	-	nC
Gate-Source Charge	$Q_{gs}$		-	2	-	
Gate-Drain Charge	$Q_{gd}$		-	2	-	
Reverse Recovery Charge	$Q_{rr}$	$I_F=10A, di/dt=100A/us$	-	1.6	-	nC
Reverse Recovery Time	$t_{rr}$		-	6	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=15V, I_D=10A$ $R_{GEN}=3$	-	6	-	ns
Turn-on Rise Time	$t_r$		-	50	-	
Turn-off Delay Time	$t_{D(off)}$		-	20	-	
Turn-off fall Time	$t_f$		-	90	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B.  $P_d$  is based on max. junction temperature, using junction-case thermal resistance.

C. The value of  $R_{\theta}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in the still air environment with  $T_A=25^\circ C$ . The maximum allowed junction temperature of  $150^\circ C$ . The value in any given application depends on the user's specific board design.



## Typical Electrical and Thermal Characteristics Diagrams

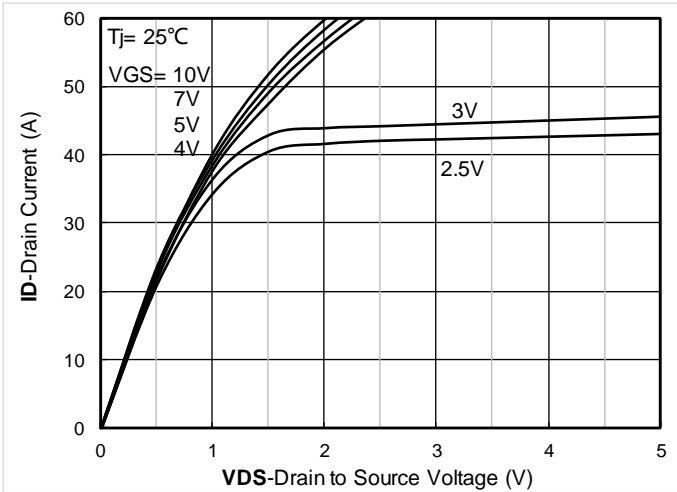


Figure 1. Output Characteristics

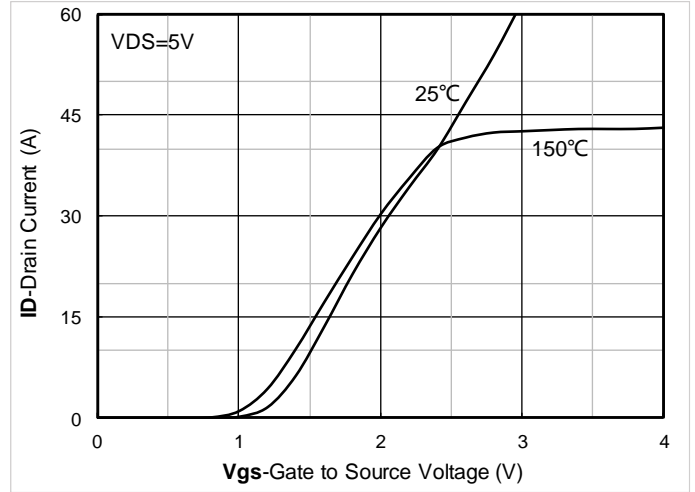


Figure 2. Transfer Characteristics

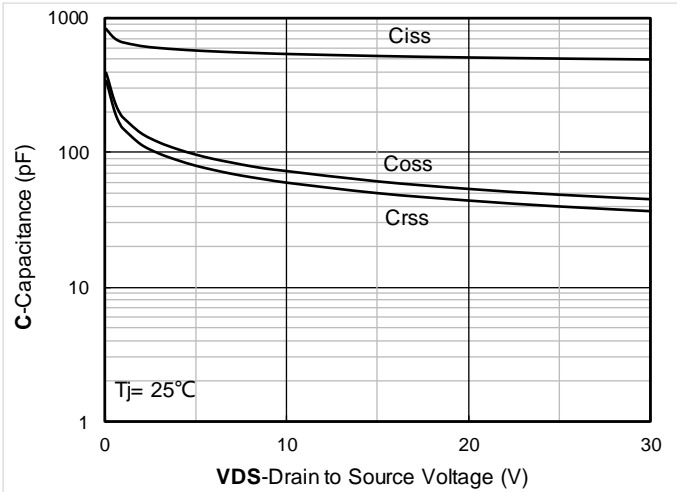


Figure 3. Capacitance Characteristics

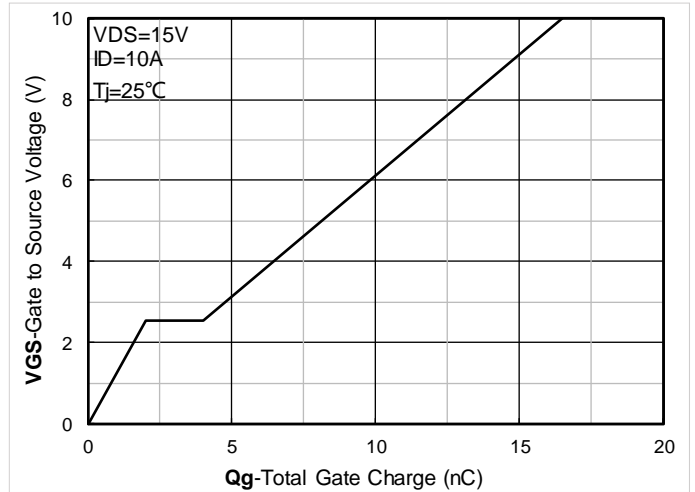


Figure 4. Gate Charge

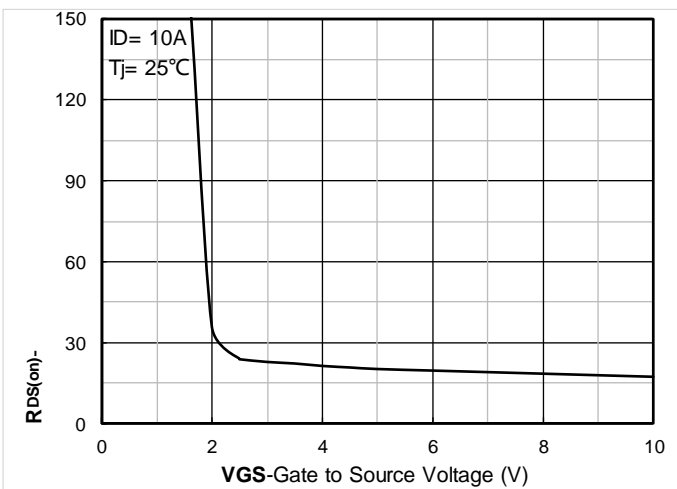


Figure 5. On-Resistance vs Gate to Source Voltage

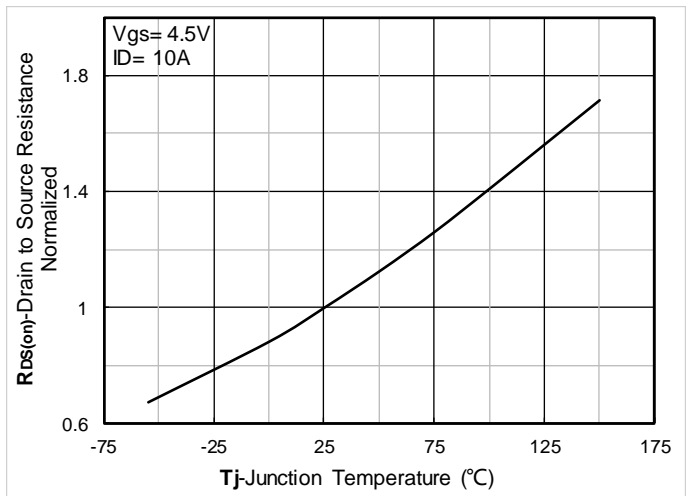


Figure 6. Normalized On-Resistance



# YJQ10N03A

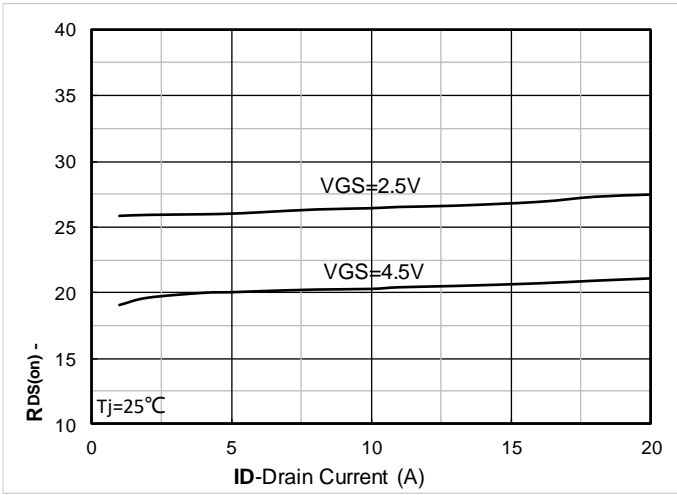


Figure 7. RDS(on) VS Drain Current

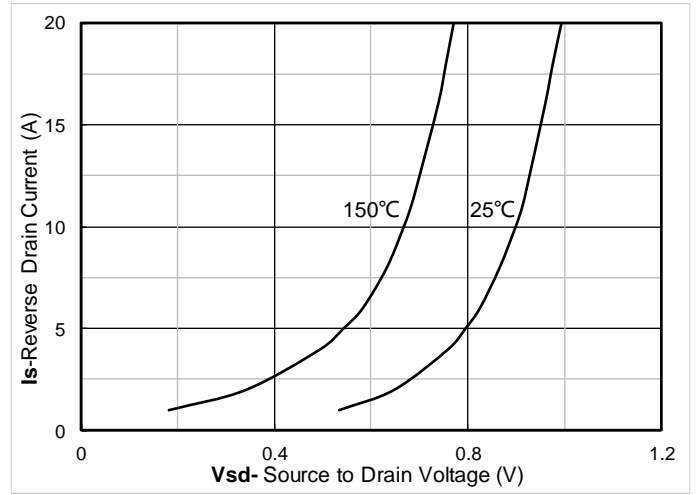


Figure 8. Forward characteristics of reverse diode

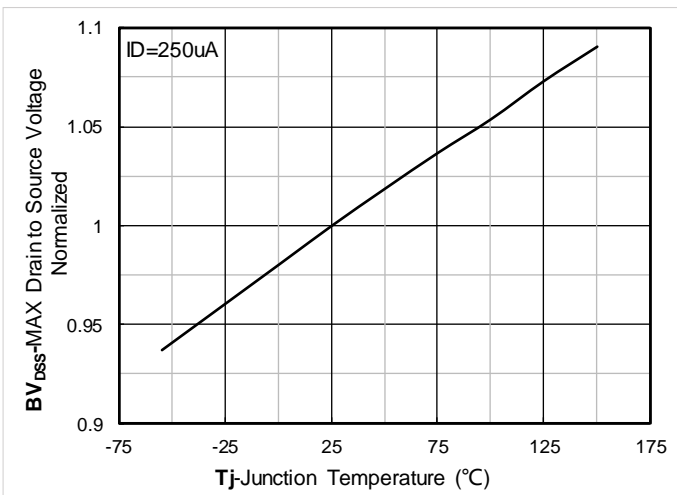


Figure 9. Normalized breakdown voltage

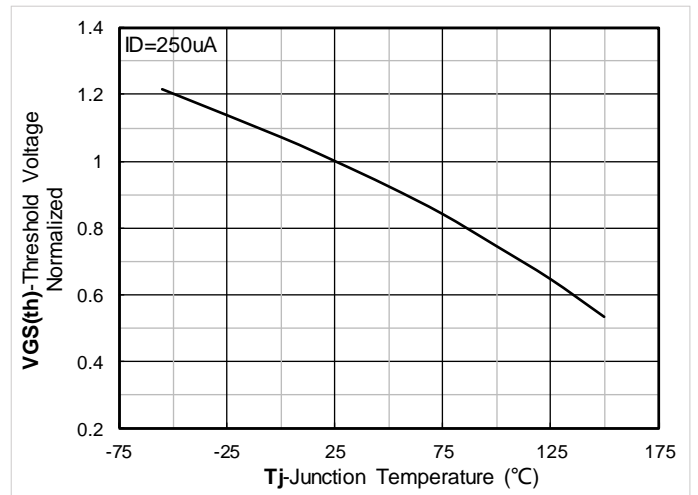


Figure 10. Normalized Threshold voltage

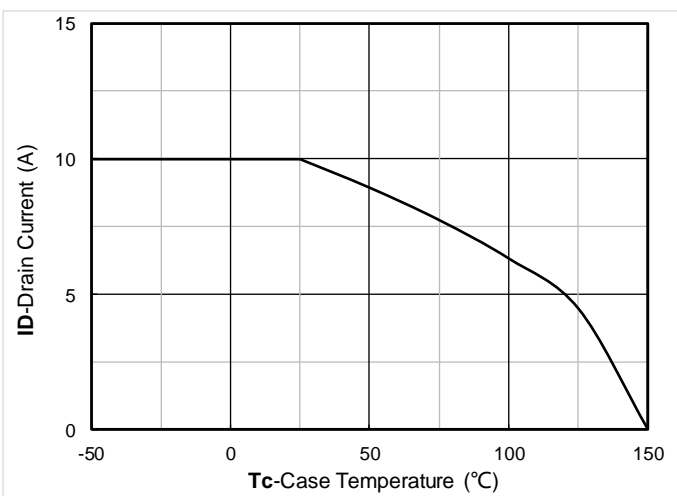


Figure 11. Current dissipation

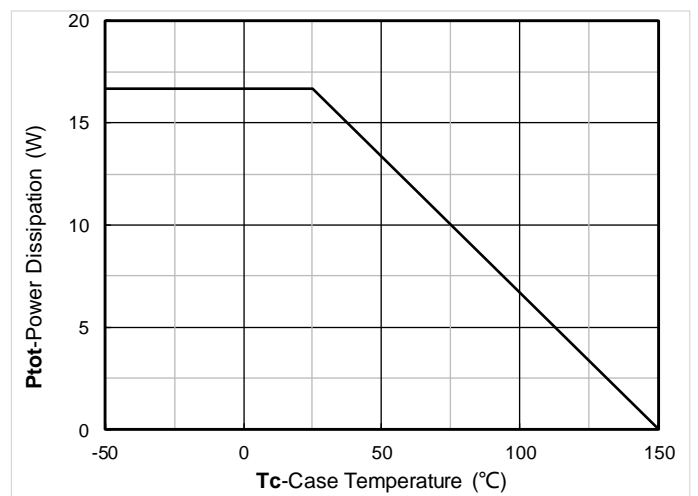


Figure 12. Power dissipation

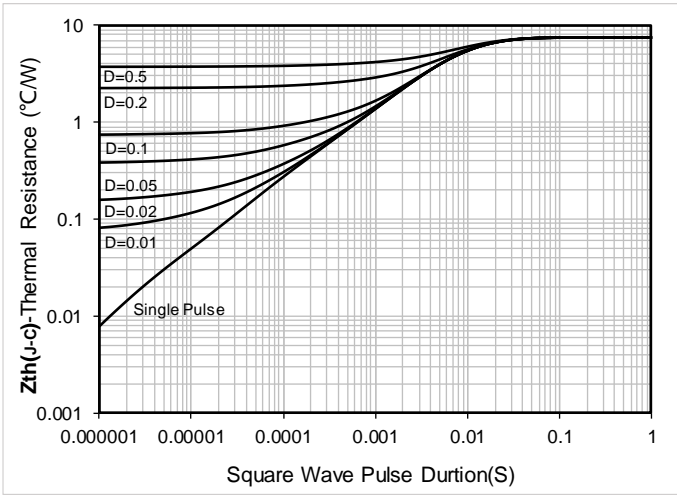


Figure 13. Maximum Transient Thermal Impedance

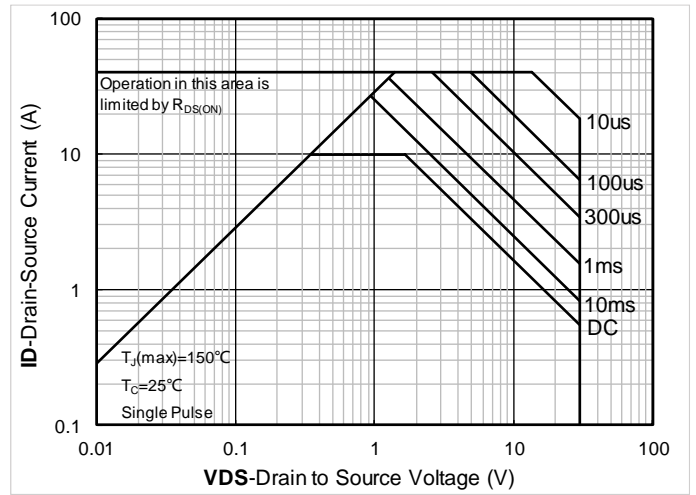


Figure 14. Safe Operation Area

## Test Circuits & Waveforms

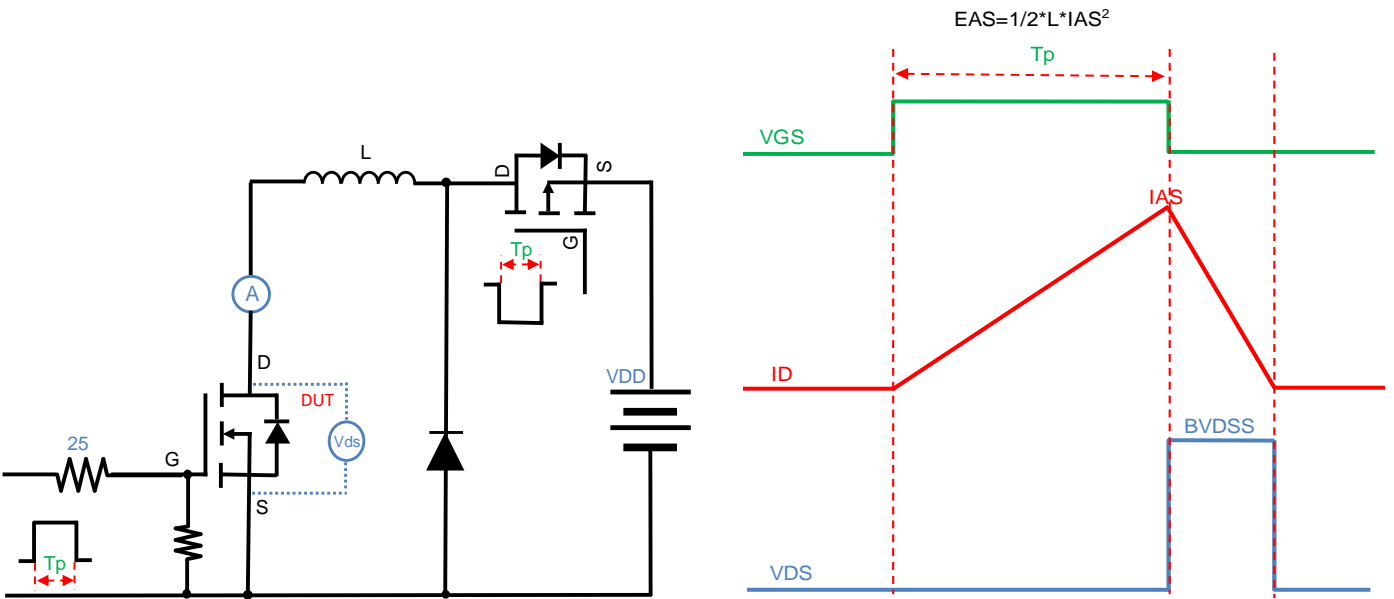


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



Figure B. Gate Charge Test Circuit & Waveform



Figure C. Resistive Switching Test Circuit & Waveform

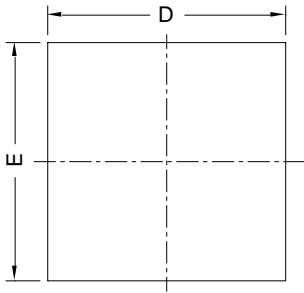


Figure D. Diode Recovery Test Circuit & Waveform

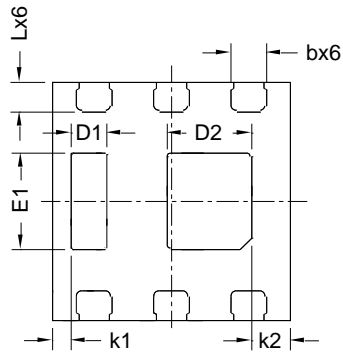


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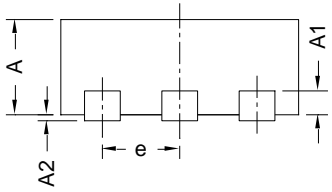
## DFN2020-6L-E-0.8mm Package information



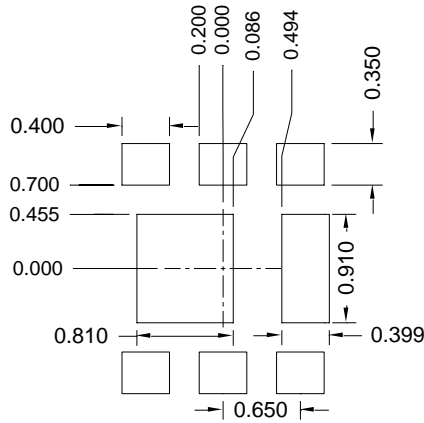
Top View



Bottom View



Side View



Suggested Solder Pad Layout  
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	1.90	2.00	2.10
E	1.90	2.00	2.10
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	0.20	0.30	0.40
D2	0.61	0.71	0.81
E1	0.71	0.81	0.91
L	0.15	0.25	0.35
b	0.20	0.30	0.40
e	0.65 BSC		
k1	0.156 BSC		
k2	0.326 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.



## YJQ10N03A

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