



N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- V_{DS} 100V
- I_D 180A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<4.3m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC



YJN180G10HJ

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
		V _{DS} =100V, V _{GS} =0V, T _J =150°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	2	3	4	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =90A	-	3.3	4.3	mΩ
		V _{GS} =10V, I _D =20A	-	3.3	4.3	
Diode Forward Voltage	V _{SD}	I _S =90A, V _{GS} =0V	-	1	1.2	V
Gate resistance	R _G	f=1MHz, Open drain	-	1.3	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	180	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	9100	-	pF
Output Capacitance	C _{oss}		-	1200	-	
Reverse Transfer Capacitance	C _{rss}		-	400	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =90A	-	138	-	nC
Gate-Source Charge	Q _{gs}		-	47	-	
Gate-Drain Charge	Q _{gd}		-	32	-	
Reverse Recovery Charge	Q _{rr}	I _F =90A, di/dt=100A/us	-	226	-	nC
Reverse Recovery Time	t _{rr}		-	82	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =90A R _{GEN} =2.2Ω	-	29	-	ns
Turn-on Rise Time	t _r		-	60	-	
Turn-off Delay Time	t _{D(off)}		-	45	-	
Turn-off fall Time	t _f		-	17	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T_J=25°C, V_{DD}=100V, V_G=10V, R_G=25Ω, L=5mH, I_{AS}=24.5A.

C. P_q is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in the still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



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Typical Electrical and Thermal Characteristics Diagrams

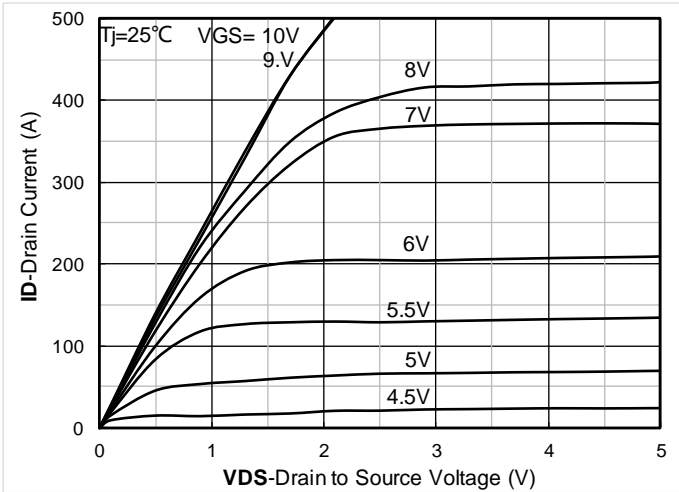


Figure 1. Output Characteristics

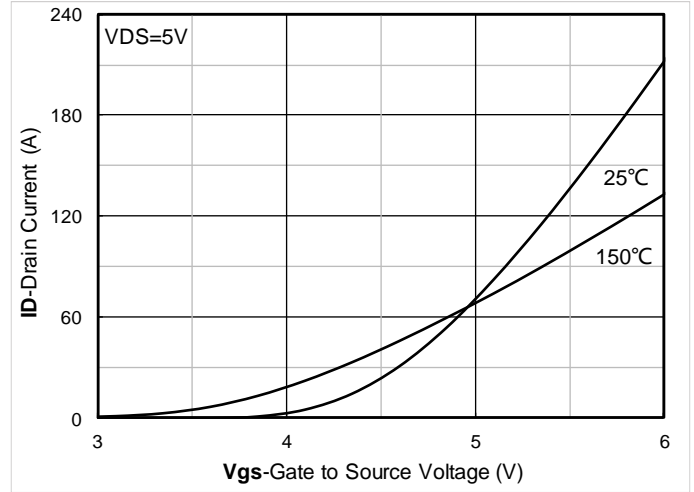


Figure 2. Transfer Characteristics

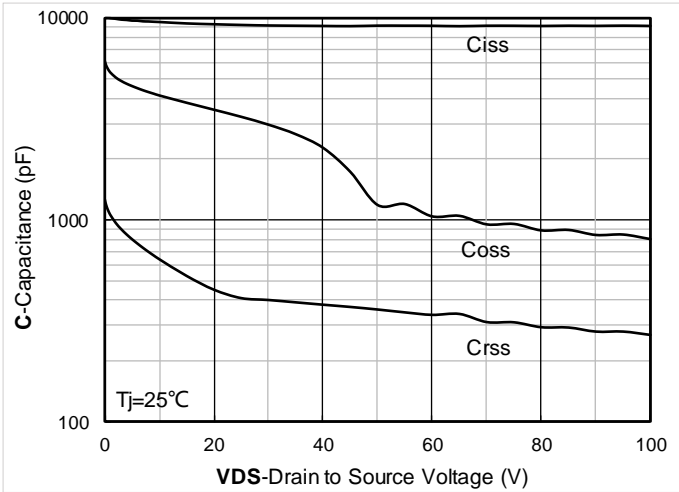


Figure 3. Capacitance Characteristics

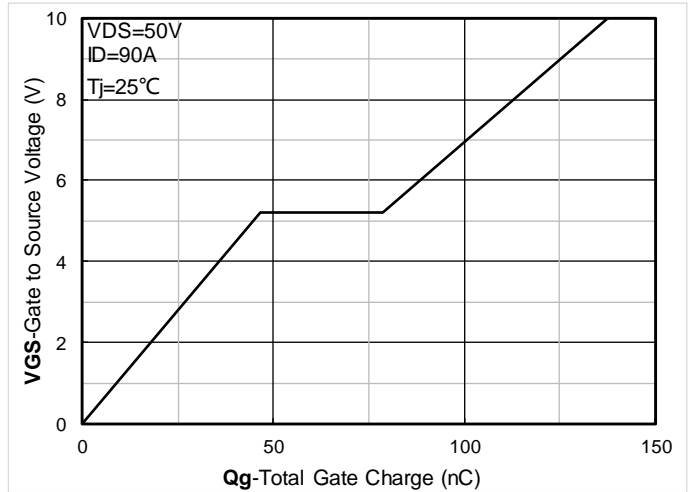


Figure 4. Gate Charge

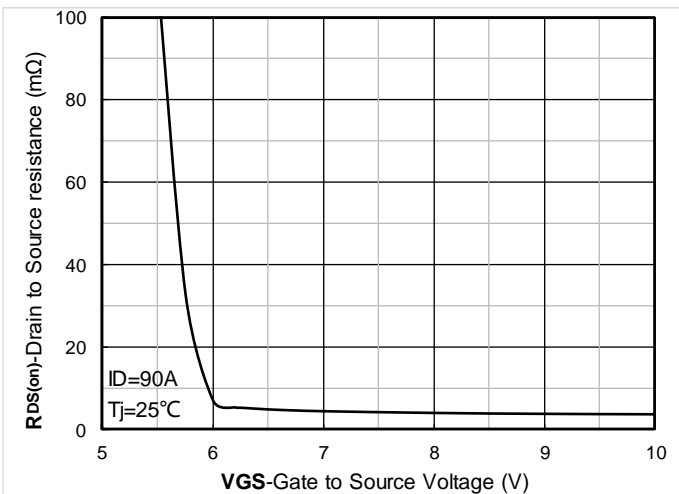


Figure 5. On-Resistance vs Gate to Source Voltage

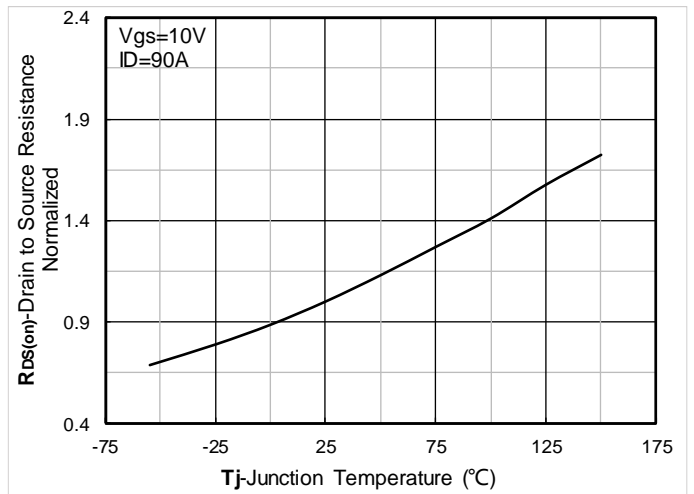


Figure 6. Normalized On-Resistance



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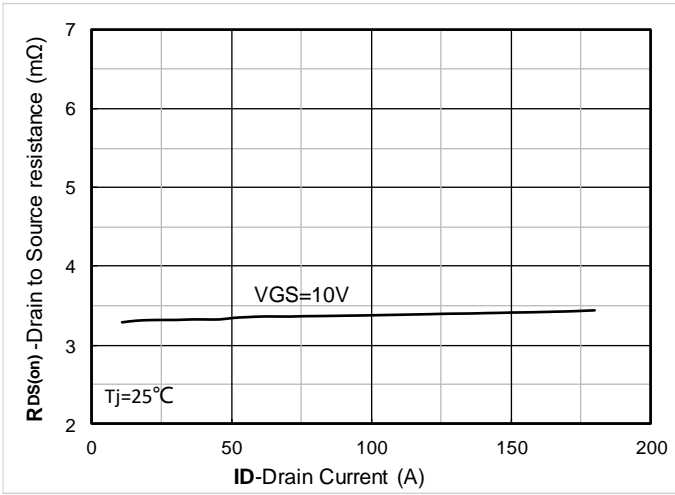


Figure 7. RDS(on) VS Drain Current

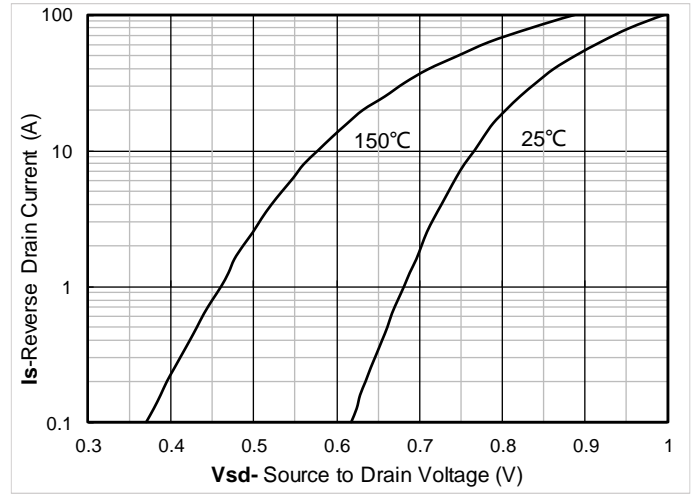


Figure 8. Forward characteristics of reverse diode

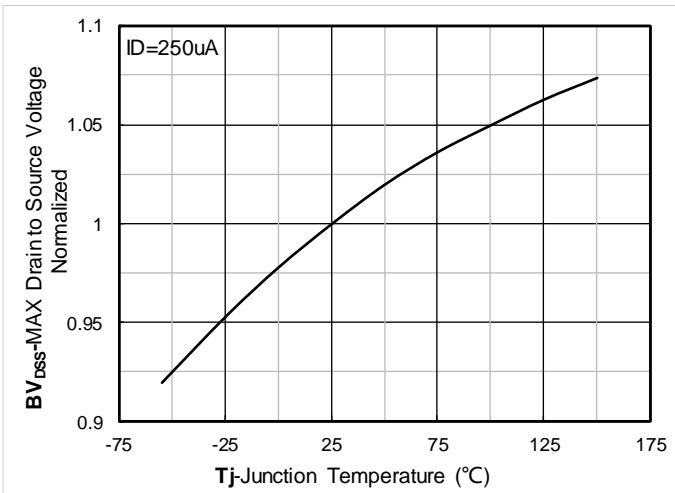


Figure 9. Normalized breakdown voltage

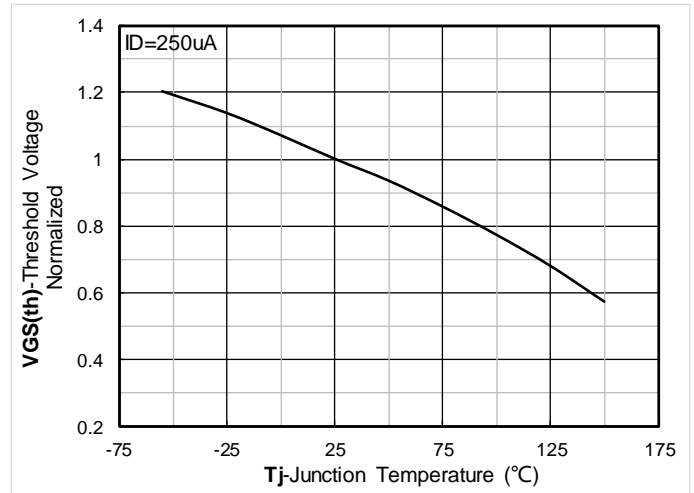


Figure 10. Normalized Threshold voltage

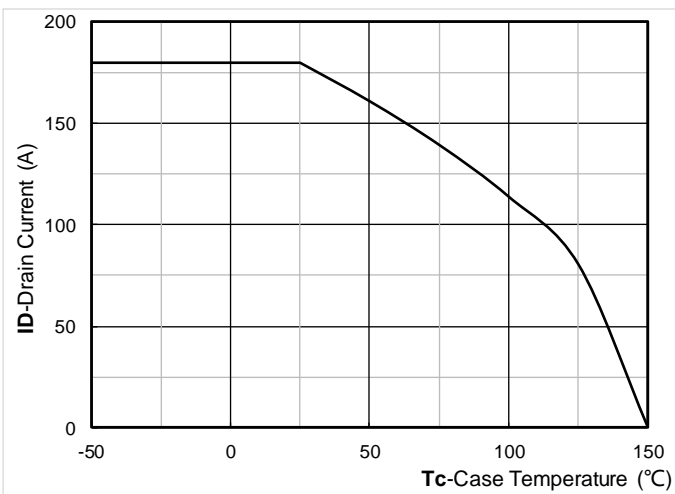


Figure 11. Current dissipation

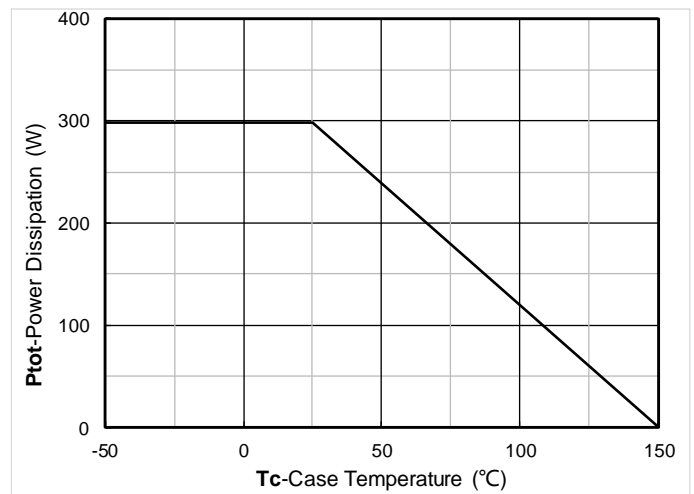


Figure 12. Power dissipation

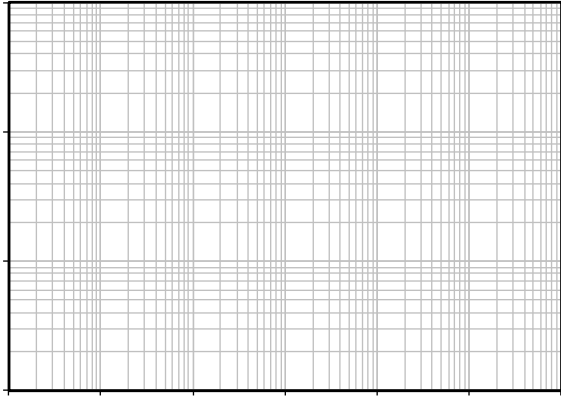


Figure 13. Maximum Transient Thermal Impedance

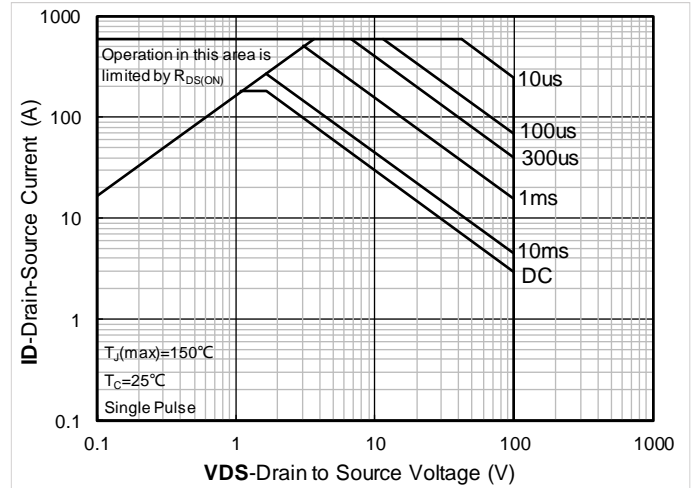


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

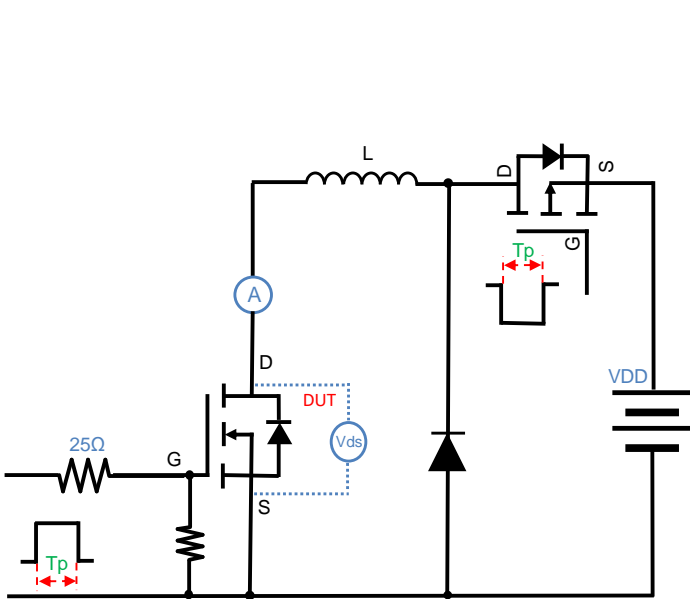
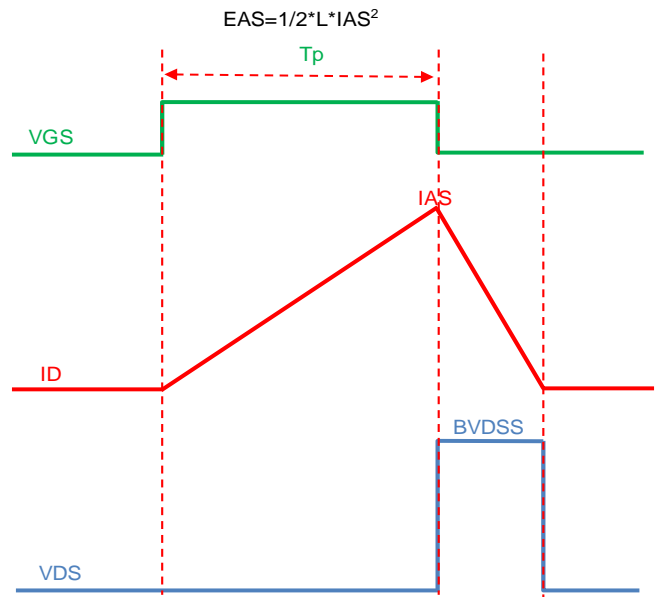


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



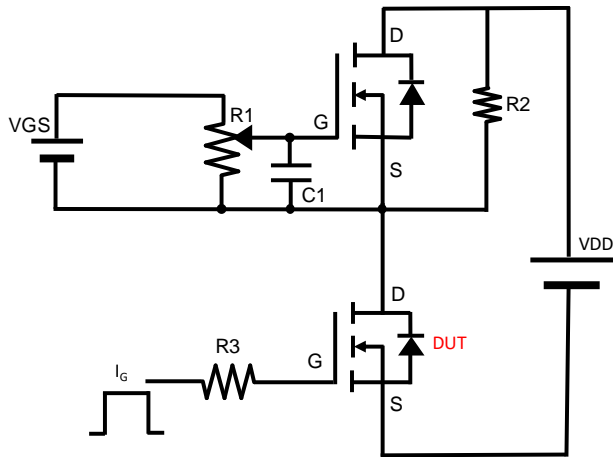


Figure B. Gate Charge Test Circuit & Waveform



Figure C. Resistive Switching Test Circuit & Waveform

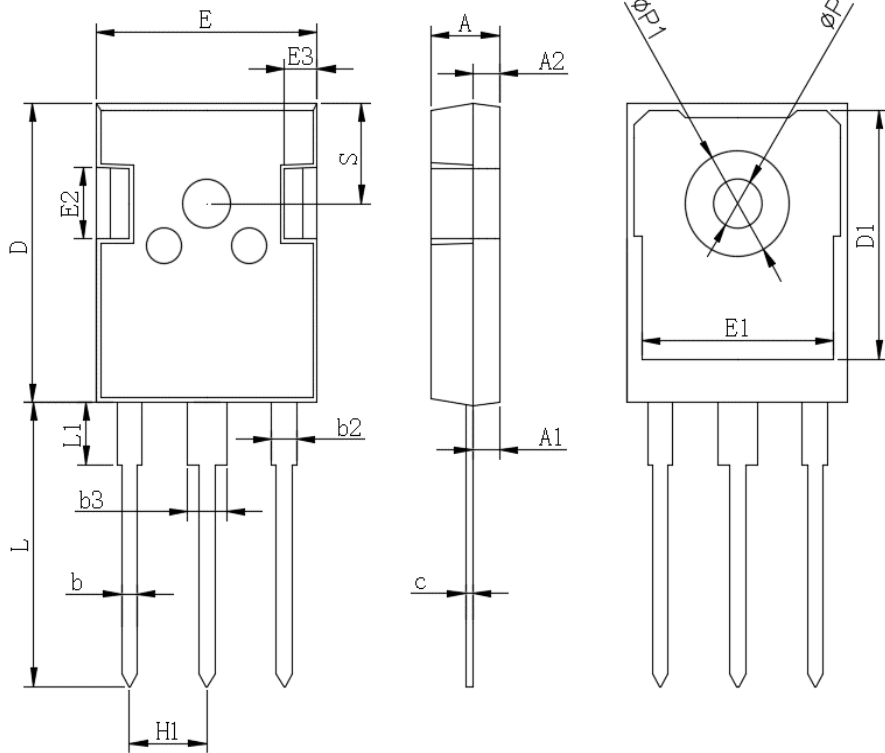


Figure D. Diode Recovery Test Circuit & Waveform



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■ TO-247AB Package information



TO-247AB		
Dim	Min	Max
A	4.80	5.20
A1	2.21	2.61
A2	1.85	2.15
b	1.0	1.4
b2	1.91	2.21
c	0.5	0.7
D	20.70	21.30
D1	16.25	16.85
E	15.50	16.10
E1	13.0	13.6
E2	4.80	5.20
E3	2.30	2.70
L	19.62	20.22
L1	-	4.30
ϕP	3.40	3.80
$\phi P1$	-	7.30
S	6.15TYP	
H1	5.44TYP	
b3	2.80	3.20



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