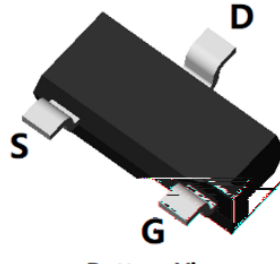
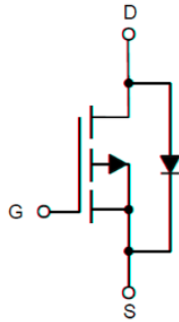


Top View



Bottom View

SOT-23



V_{DS}	-30V
I_D	-4.1A
$R_{DS(ON)}$ (at $V_{GS}=-10V$)	49mohm
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	65mohm

Trench Power LV MOSFET technology
High density cell design for Low $R_{DS(ON)}$
High Speed switching
Part no. with suffix "Q" means AEC-Q101 qualified

Battery protection
Load switch
Power management

($T_A=25$ unless otherwise noted)

Drain-source Voltage		V_{DS}	-30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25$	I_D	-4.1	A
	$T_A=70$		-3.2	
Pulsed Drain Current ^A		I_{DM}	-15	A
Total Power Dissipation	$T_A=25$	P_D	1.2	W
	$T_A=70$		0.8	
Thermal Resistance Junction-to-Ambient ^B		R_{JA}	105	/ W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	

(Example)

YJL3407AQ	F2	3407.	3000	30000	120000	7" reel
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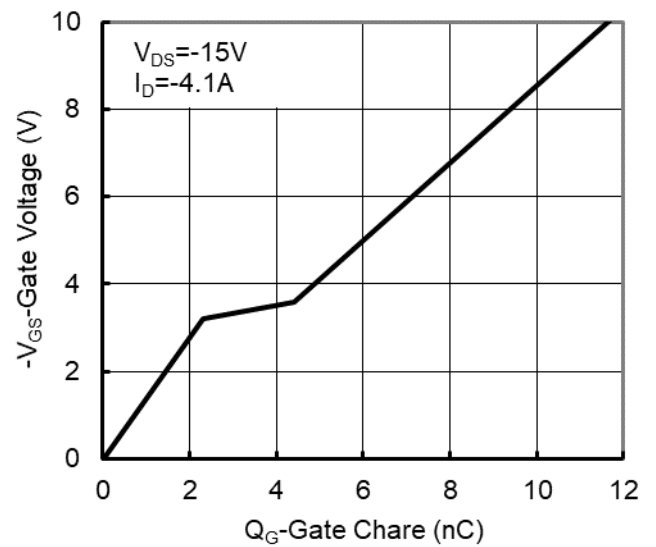
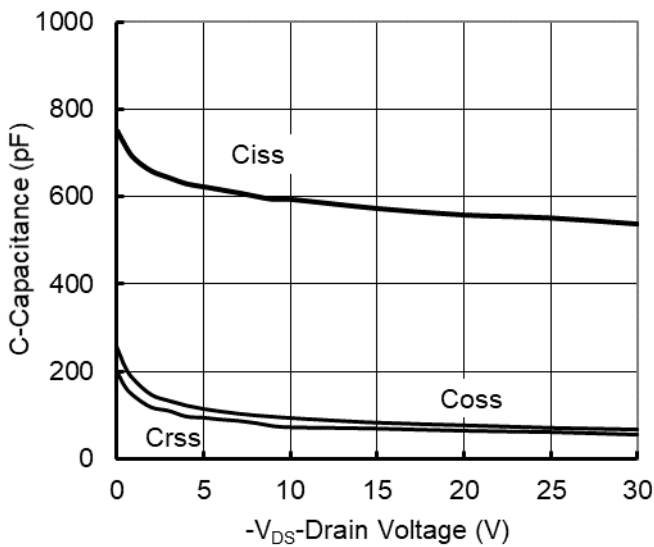
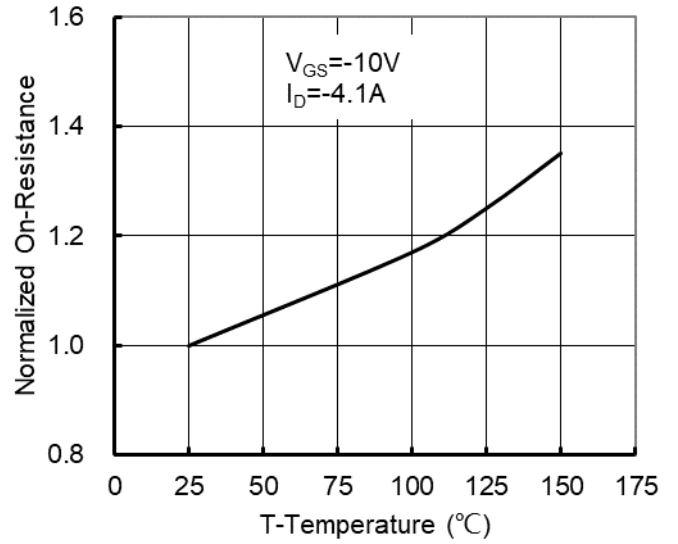
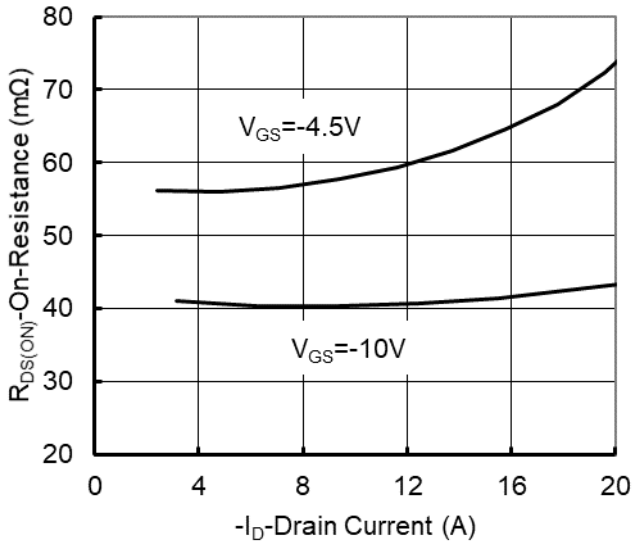
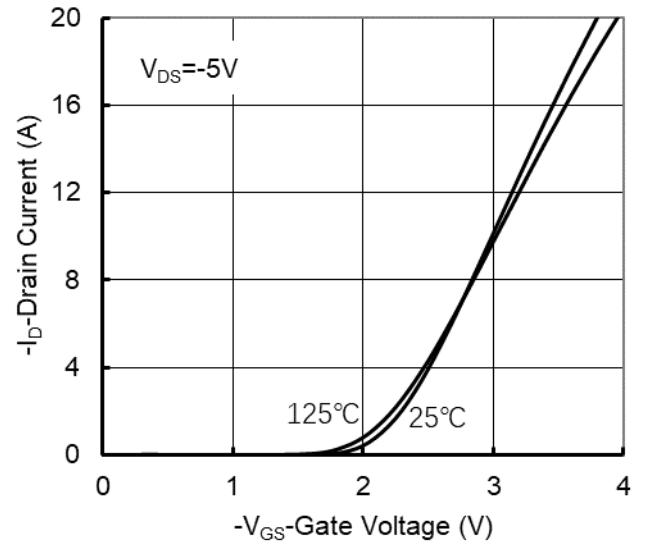
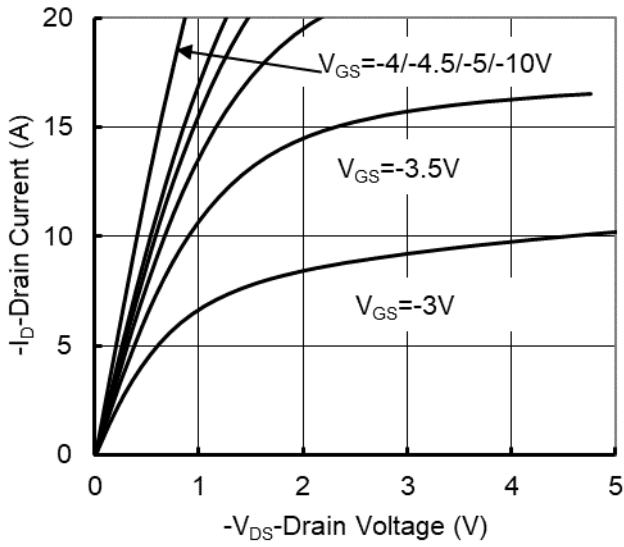


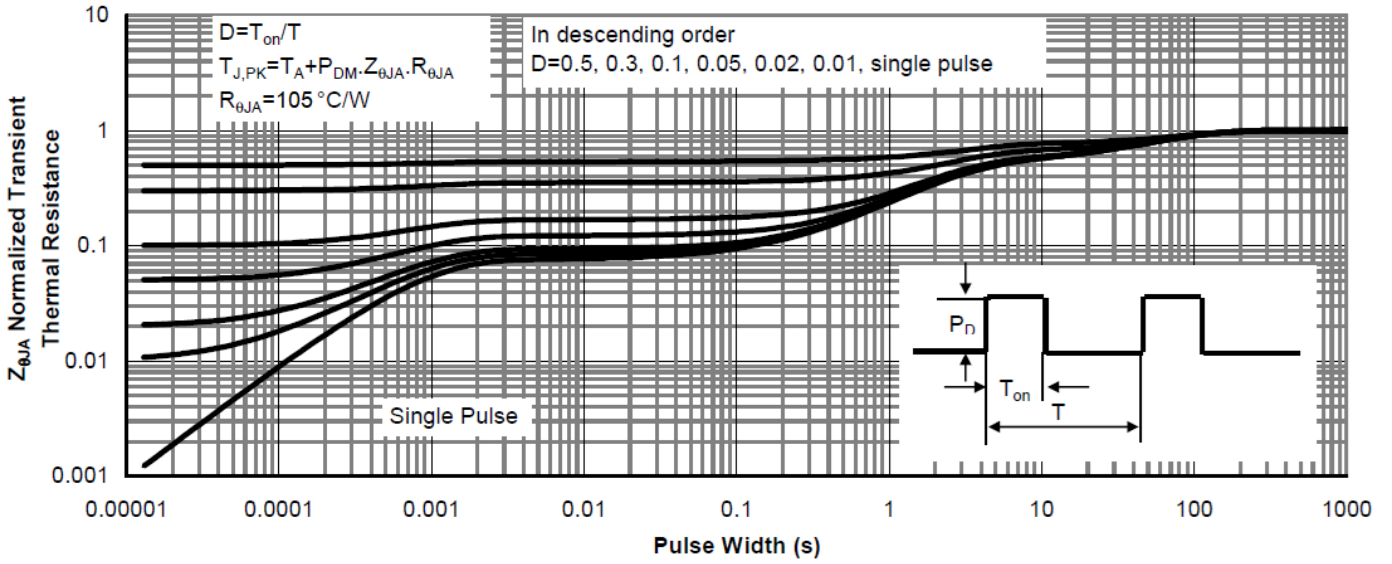
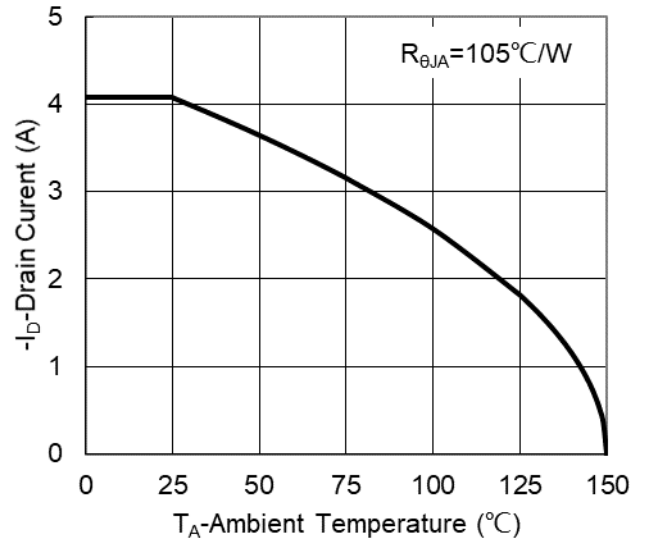
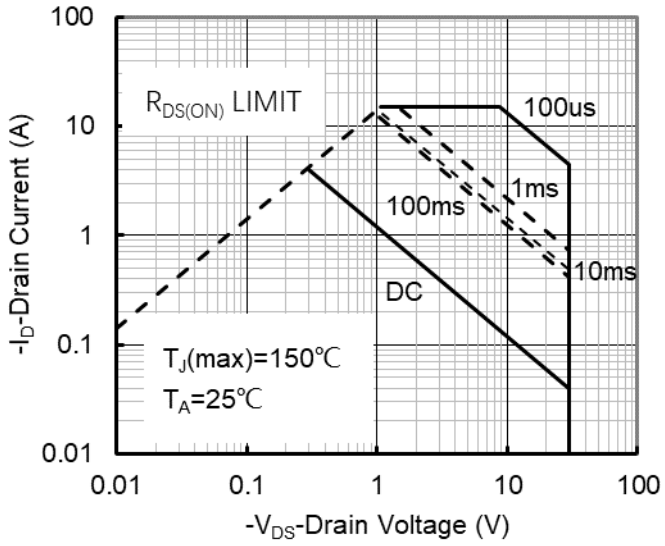
($T_J=25$ unless otherwise noted)

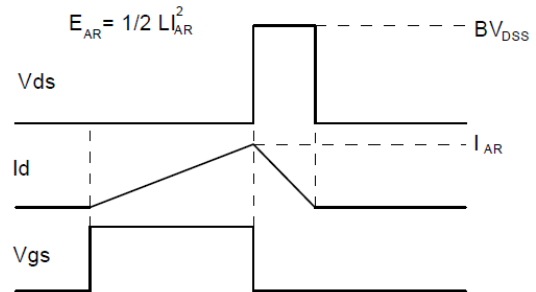
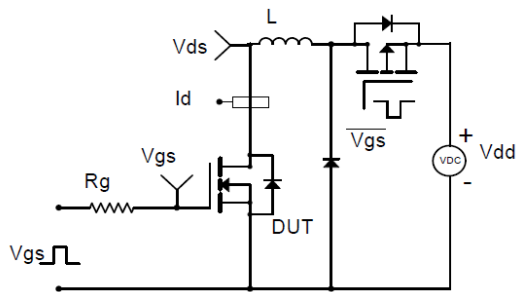
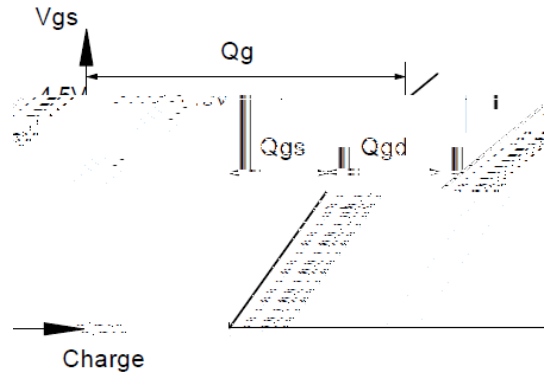
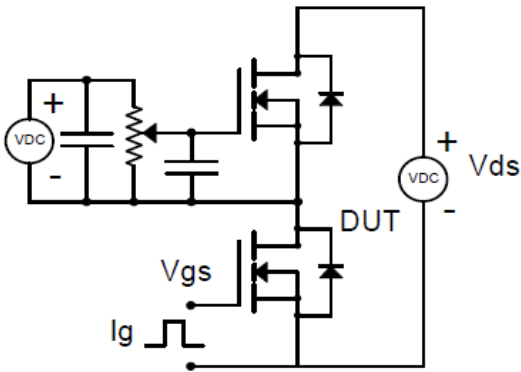
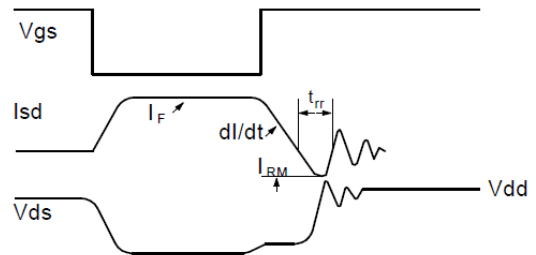
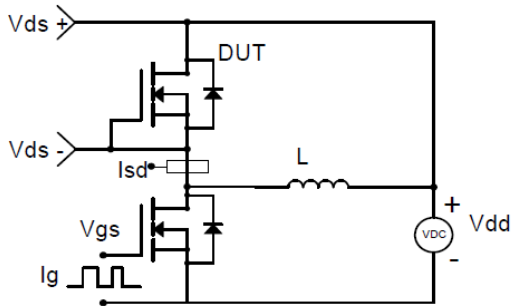
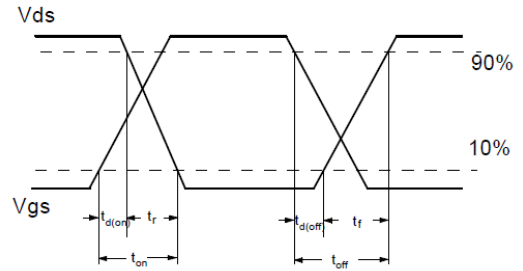
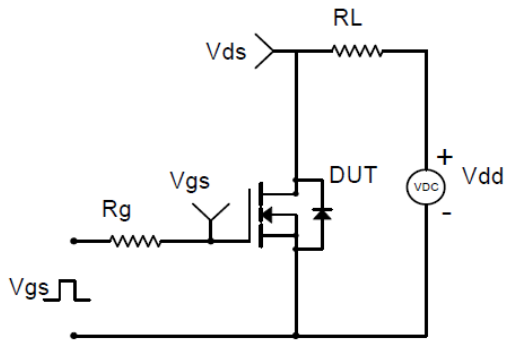
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V, T_J=25$			-1	μA
		$V_{DS}=-30V, V_{GS}=0V, T_J=150$			-5	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 10V, V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.5	-2.4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-4.1A$		36	49	m
		$V_{GS}=-4.5V, I_D=-3.5A$		52	65	
Diode Forward Voltage	V_{SD}	$I_S=-4.1A, V_{GS}=0V$			-1.2	V
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$		572		pF
Output Capacitance	C_{oss}			82		
Reverse Transfer Capacitance	C_{rss}			70		
Total Gate Charge	Q_g	$V_{GS}=-10V, V_{DS}=-15V, I_D=-4.1A$		11.65		nC
Gate-Source Charge	Q_{gs}			2.32		
Gate-Drain Charge	Q_{gd}			2.08		
Reverse Recovery Charge	Q_{rr}	$I_F=-10A, di/dt=100A/\mu s$		0.643		ns
Reverse Recovery Time	t_{rr}			15.7		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=-10V, V_{DS}=-15V, R_L=15$ $R_{GEN}=2.5$		3.8		ns
Turn-on Rise Time	t_r			17.6		
Turn-off Delay Time	$t_{D(off)}$			17.8		
Turn-off fall Time	t_f			21.8		

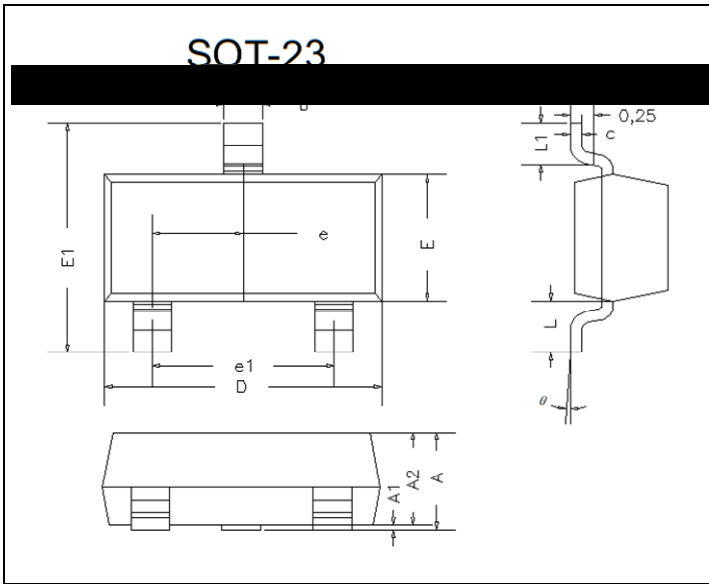
A. Pulse Test: Pulse Width 300us, Duty cycle 2%.

B. R_{JA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{JC} is guaranteed by design, while R_{JA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² FR-4 board with 2oz copper.

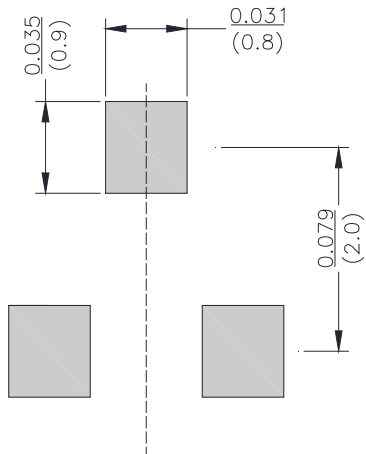








DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	0.035	0.045	0.90	1.15	
A1	0.000	0.004	0.00	0.10	
A2	0.035	0.041	0.90	1.05	
b	0.012	0.020	0.30	0.50	
c	0.004	0.008	0.10	0.20	
D	0.110	0.118	2.80	3.00	
E	0.047	0.055	1.20	1.40	
E1	0.089	0.100	2.25	2.55	
e	0.370TYP		0.95TYP		
e1	0.071	0.079	1.80	2.00	
L	0.220REF		0.55REF		
L1	0.012	0.020	0.30	0.50	
	0°	8°	0°	8°	





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