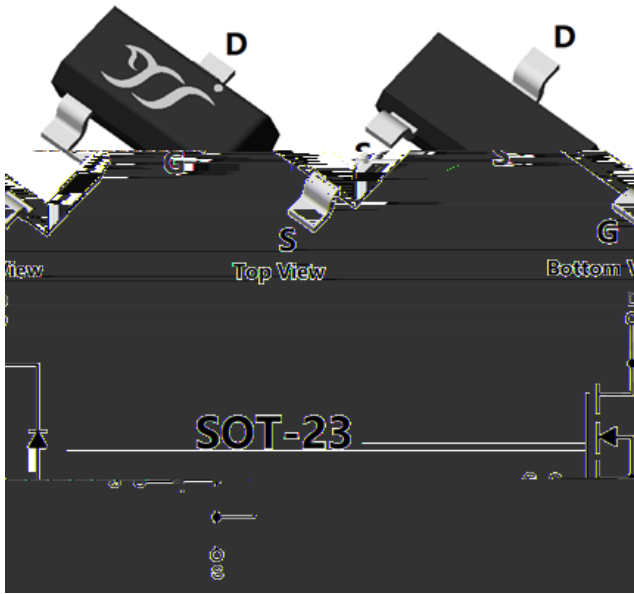


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 30V
- I_D 5.6A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<24m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $<43m\Omega$

General Description

- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	5.6	A
	$T_A=100^\circ C$		3.5	
Pulsed Drain Current ^A		I_{DM}	40	A
Total Power Dissipation ^B	$T_A=25^\circ C$	P_D	1	W
	$T_A=100^\circ C$		0.4	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^C	Steady-State	$R_{\theta JA}$	100	120	$^\circ C/W$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL3404B	F2	3404.	3000	30000	120000	7" reel



Typical Electrical and Thermal Characteristics Diagrams

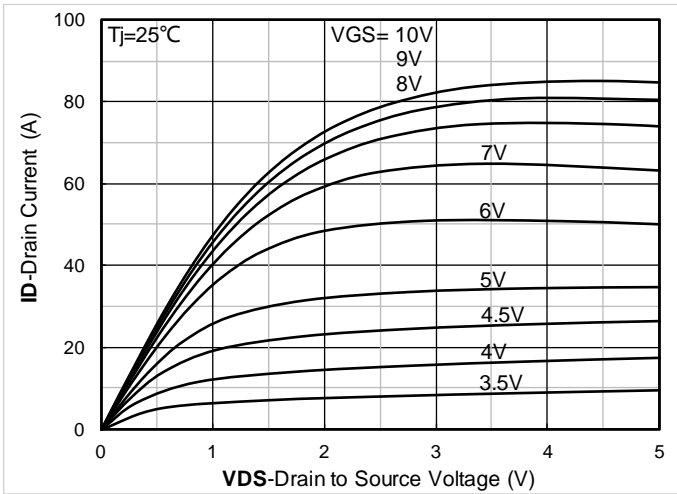


Figure 1. Output Characteristics

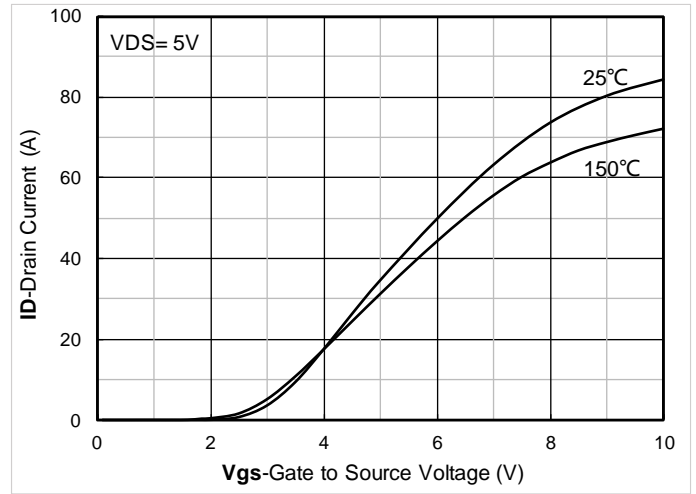


Figure 2. Transfer Characteristics

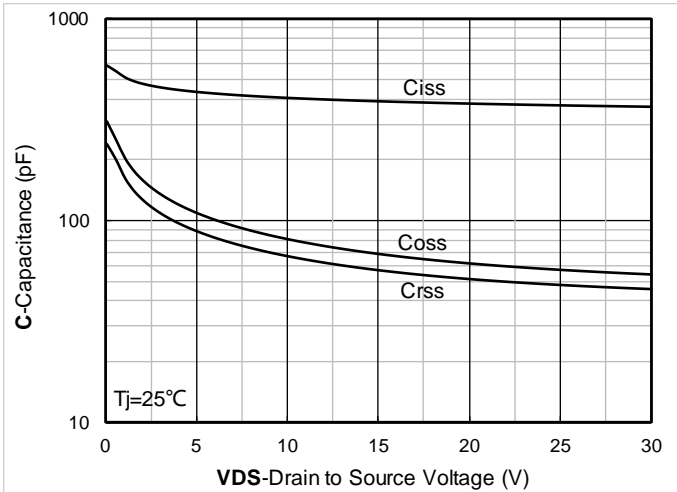


Figure 3. Capacitance Characteristics

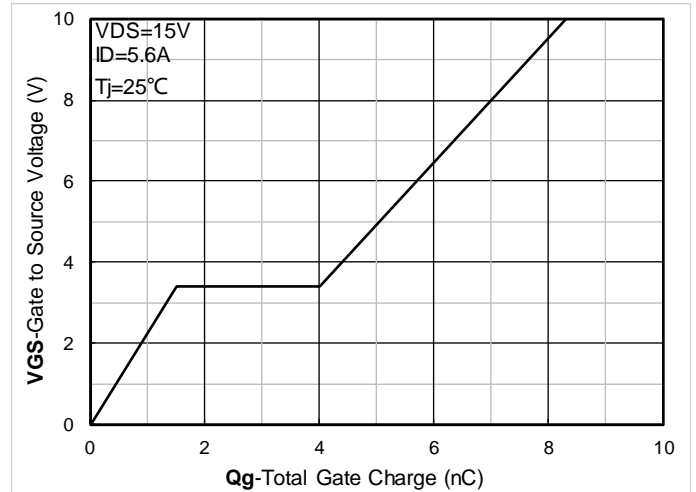


Figure 4. Gate Charge

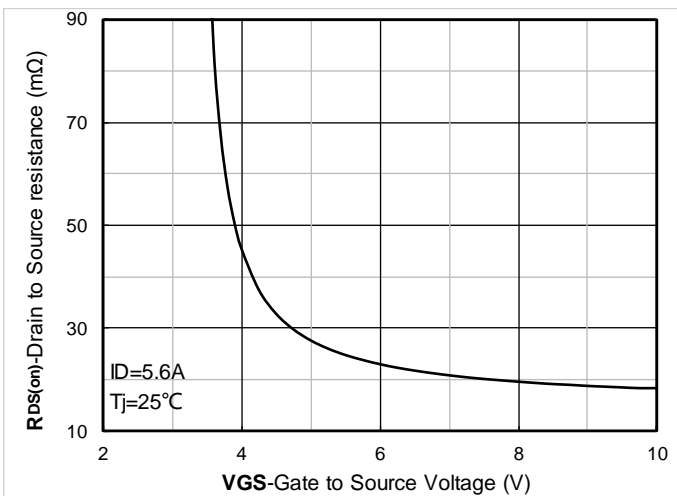


Figure 5. On-Resistance vs Gate to Source Voltage

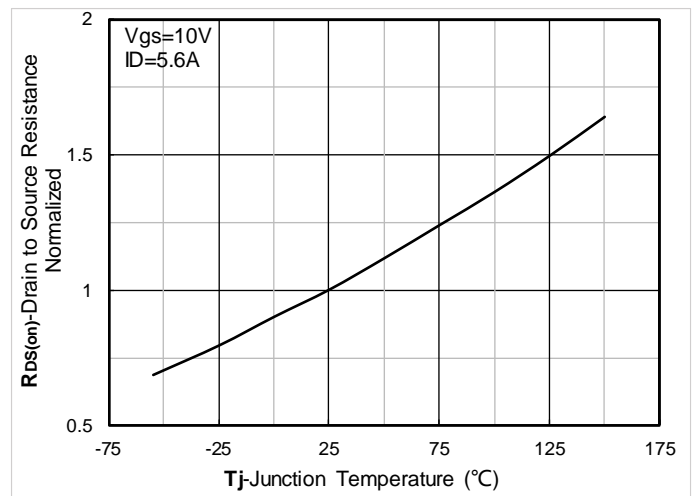


Figure 6. Normalized On-Resistance

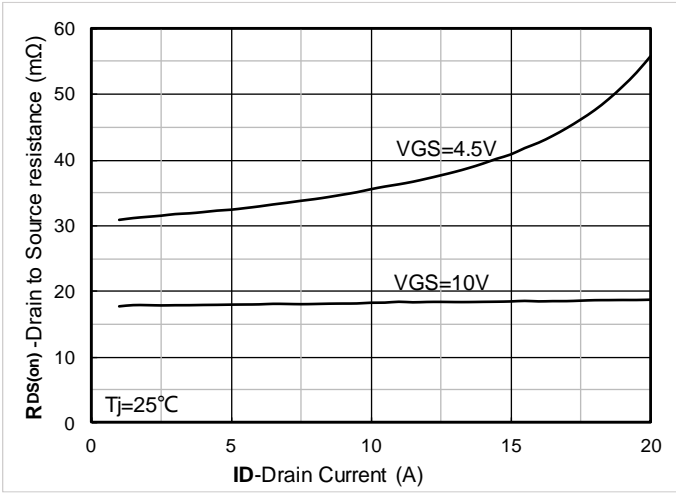


Figure 7. $R_{DS(on)}$ VS Drain Current

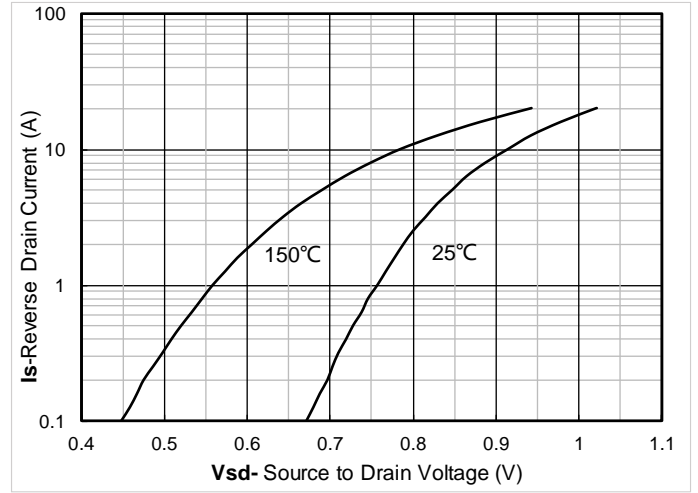


Figure 8. Forward characteristics of reverse diode

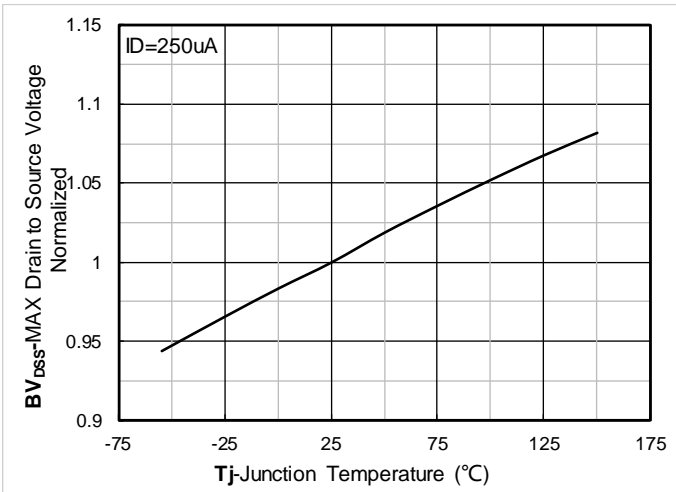


Figure 9. Normalized breakdown voltage

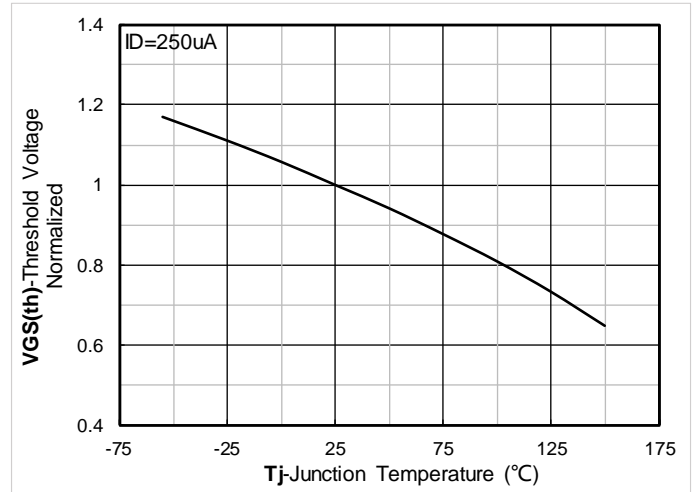


Figure 10. Normalized Threshold voltage

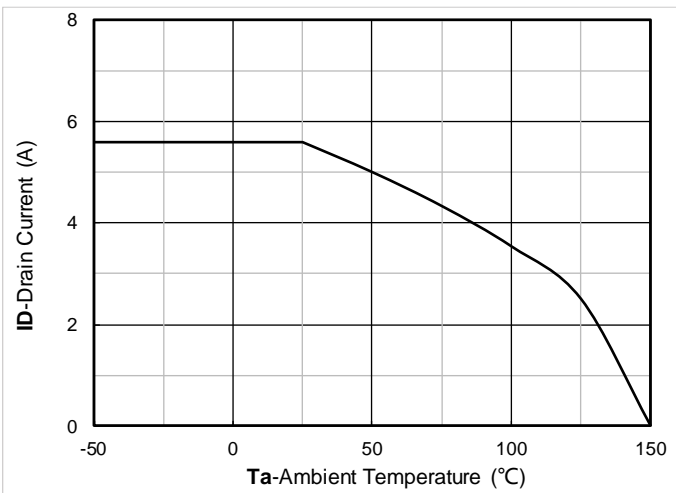


Figure 11. Current dissipation

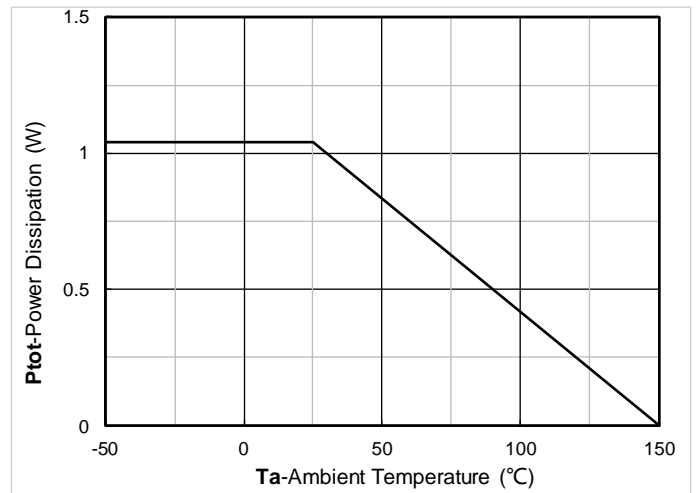


Figure 12. Power dissipation

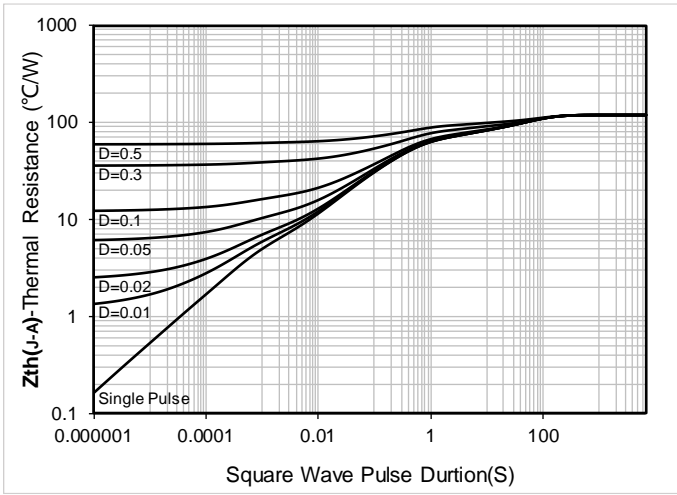


Figure 13. Maximum Transient Thermal Impedance

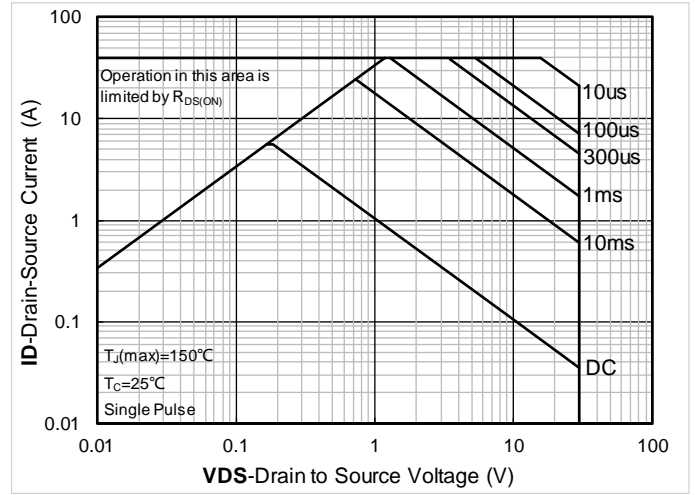


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

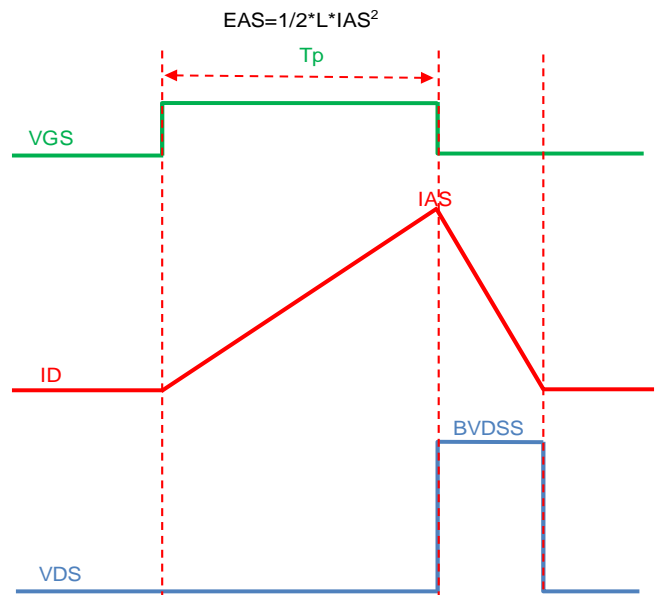
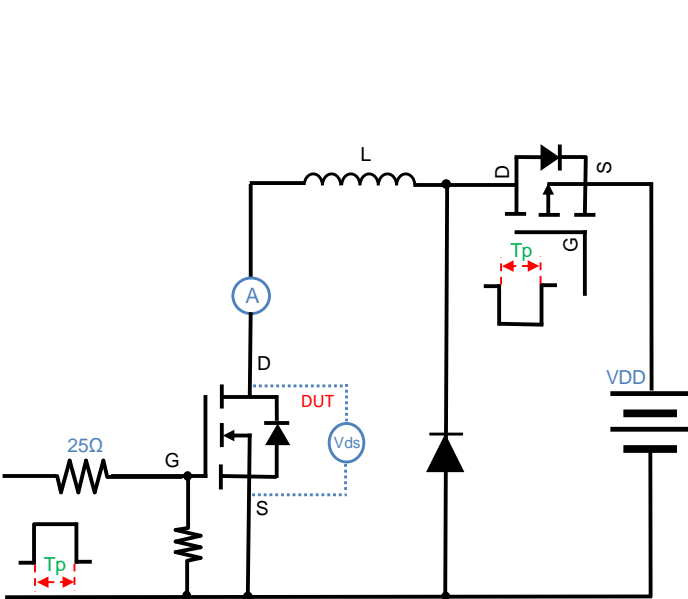


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

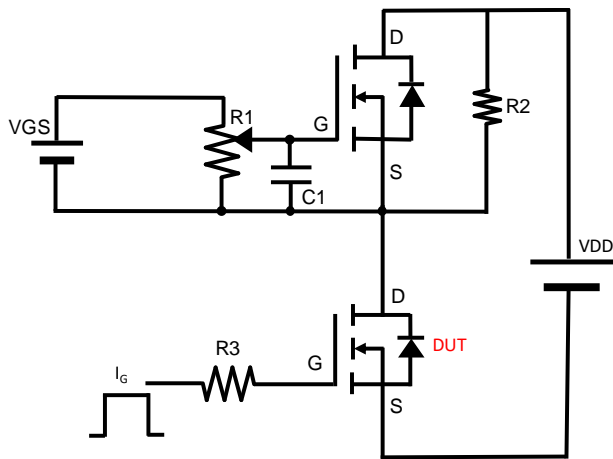


Figure B. Gate Charge Test Circuit & Waveform

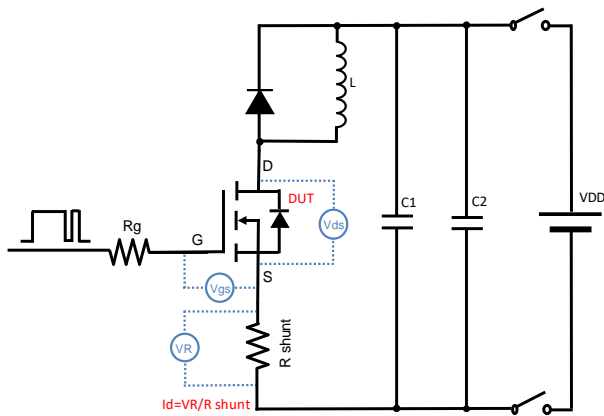


Figure C. Resistive Switching Test Circuit & Waveform

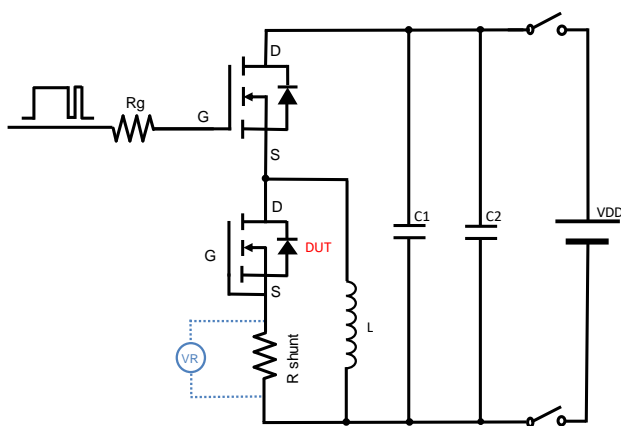
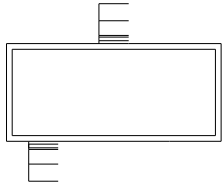


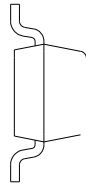
Figure D. Diode Recovery Test Circuit & Waveform



■ SOT-23 Package information



TOP VIEW



SIDE VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT



YJL3404B

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