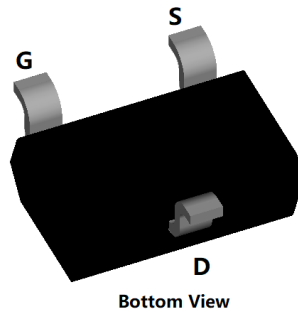
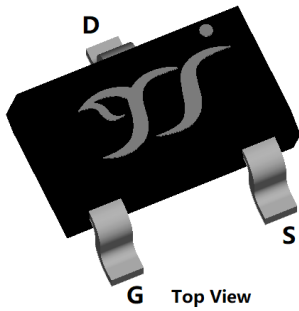
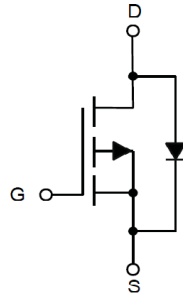


## P-Channel Enhancement Mode Field Effect Transistor



**SOT-23-3L**



### Product Summary

- $V_{DS}$  -30V
- $I_D$  -4.4A
- $R_{DS(ON)}$ ( at  $V_{GS}=-10V$ ) <55mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=-4.5V$ ) <66mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=-2.5V$ ) <94mohm
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Trench Power LV MOSFET technology
- High density cell design for Low  $R_{DS(ON)}$
- High Speed switching

### Applications

- Battery protection
- Power management
- Load switch

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	-30	V
Gate-source Voltage	$V_{GS}$	$\pm 12$	V
Drain Current	$I_D$	$T_A=25^\circ\text{C}$	-4.4
		$T_A=70^\circ\text{C}$	-3.5
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	-27	A
Total Power Dissipation	$P_D$	$T_A=25^\circ\text{C}$	1.5
		$T_A=70^\circ\text{C}$	0.98
Thermal Resistance Junction-to-Ambient <sup>B</sup>	$R_{\theta JA}$	82	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL3401AL	F1	R1 <sub>A</sub>	3000	30000	120000	7" reel



# YJL3401AL

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V			-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.6	-0.9	-1.4	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-4.4A		40	55	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3A		47	66	
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-2A		60	94	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-4.4A, V <sub>GS</sub> =0V			-1.2	V
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHZ		1040		pF
Output Capacitance	C <sub>oss</sub>			80		
Reverse Transfer Capacitance	C <sub>rss</sub>			68		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-4.4A		22		nC
Gate-Source Charge	Q <sub>gs</sub>			3.28		
Gate-Drain Charge	Q <sub>gd</sub>			2.11		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =4.4A R <sub>GEN</sub> =3Ω		4.4		nC
Turn-on Rise Time	t <sub>r</sub>			26		
Turn-off Delay Time	t <sub>D(off)</sub>			49.2		
Turn-off fall Time	t <sub>f</sub>			42.8		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



### Typical Performance Characteristics

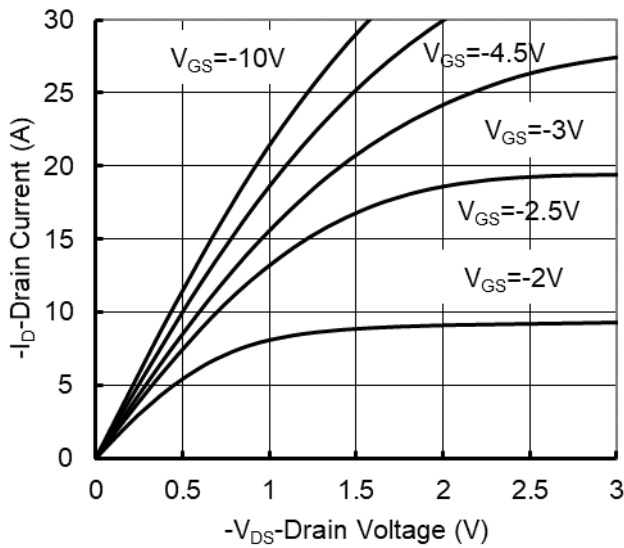


Figure1. Output Characteristics

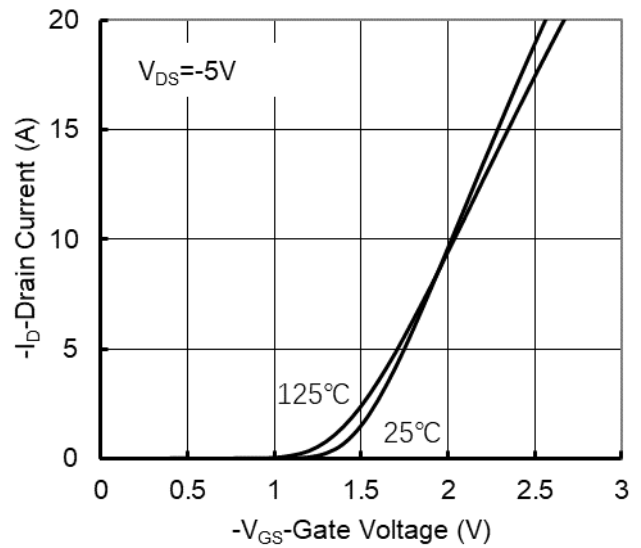


Figure2. Transfer Characteristics

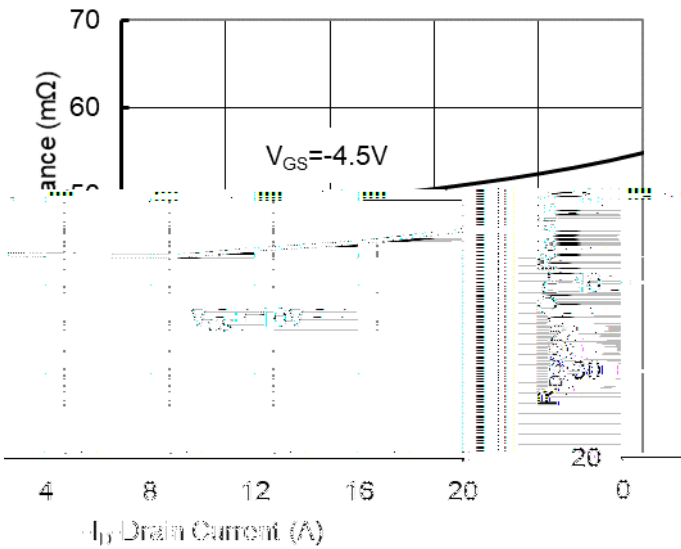


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

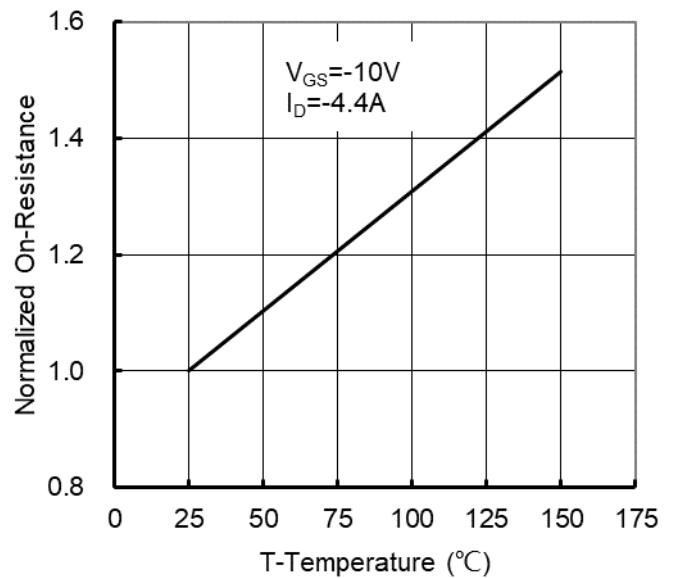


Figure 4: On-Resistance vs. Junction Temperature

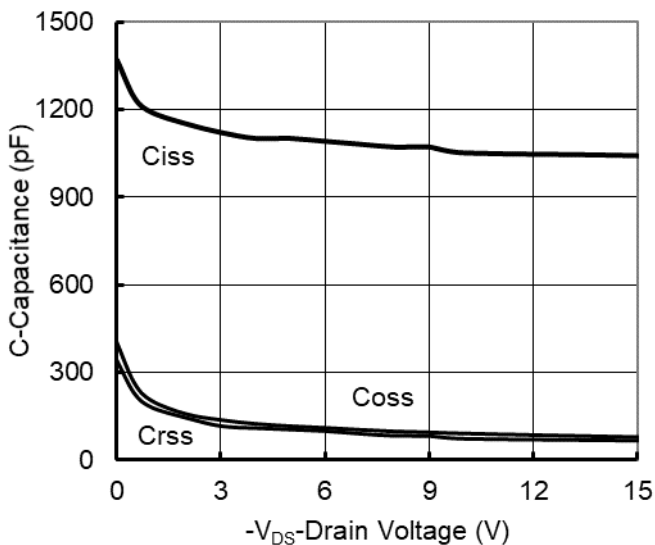


Figure5. Capacitance Characteristics

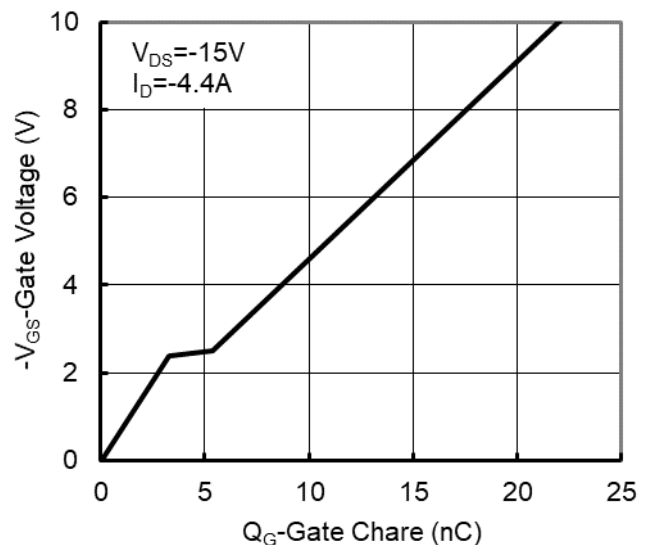


Figure6. Gate Charge

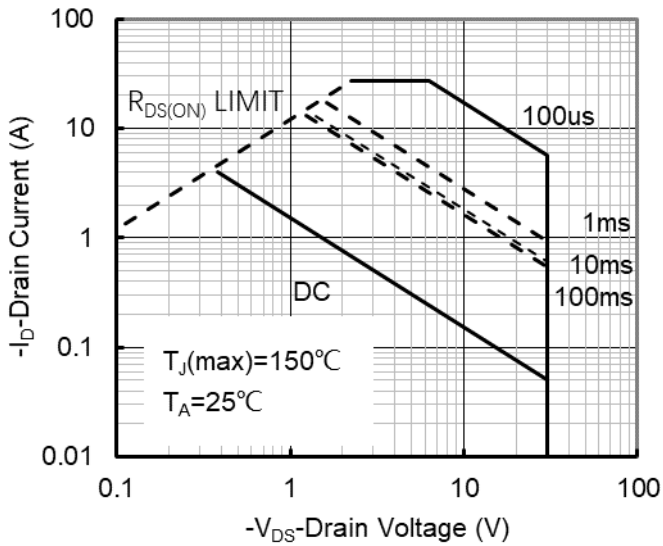


Figure7. Safe Operation Area

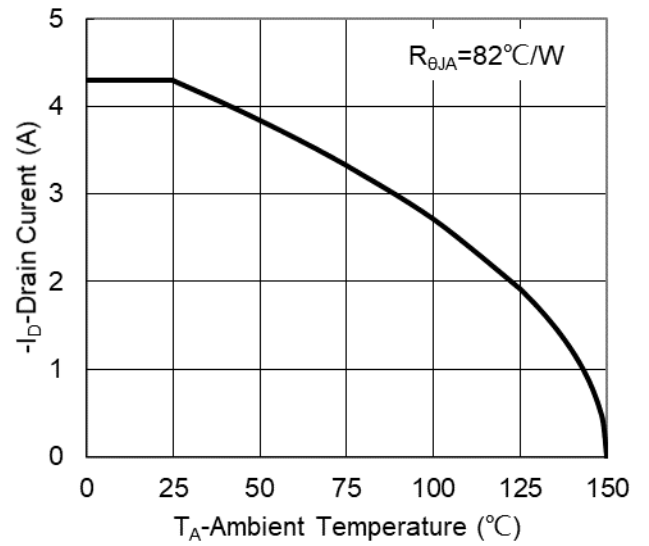


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

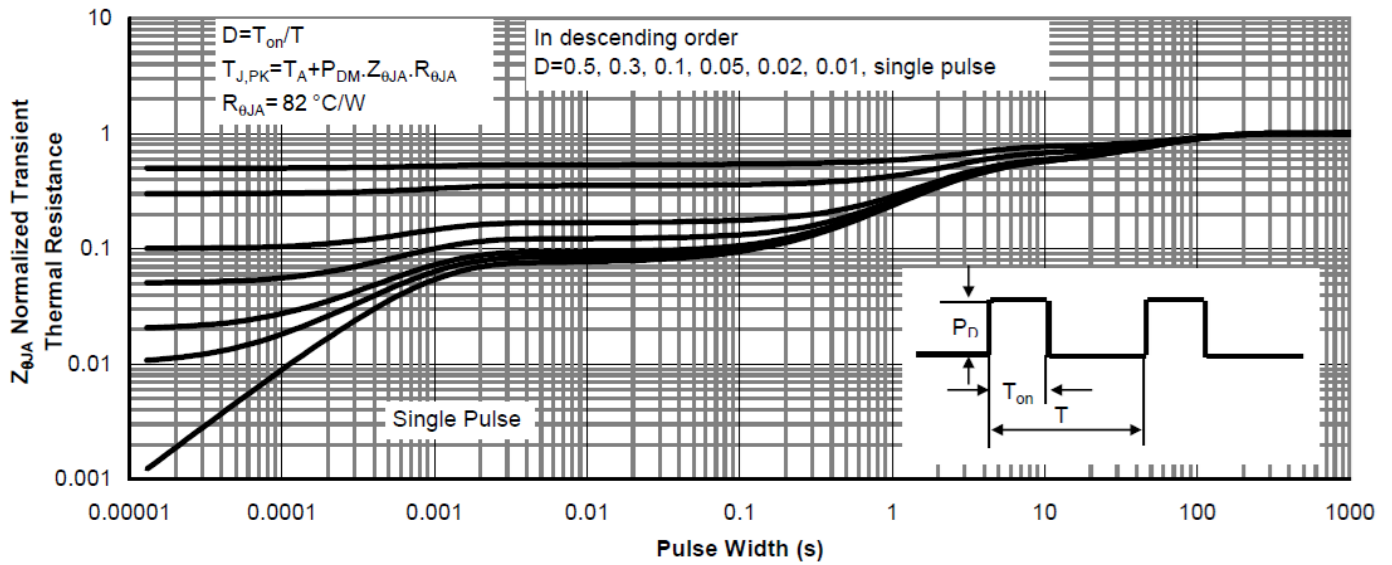
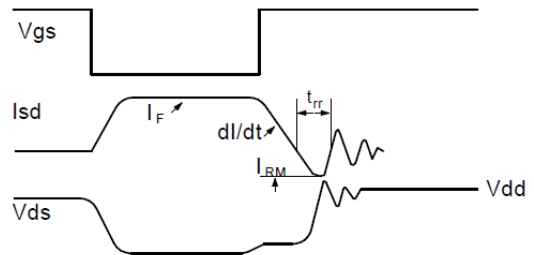
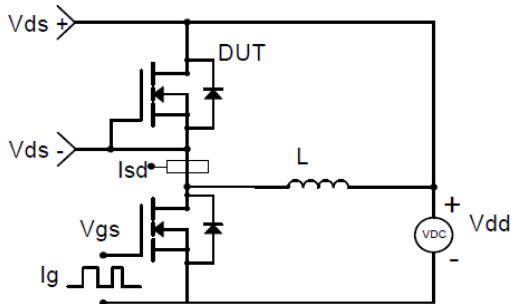


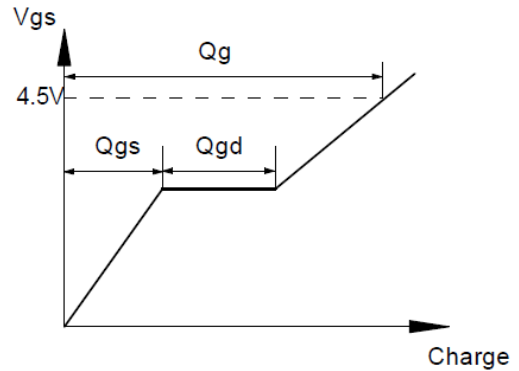
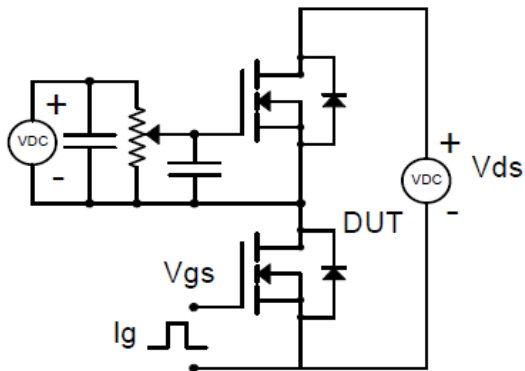
Figure9. Normalized Maximum Transient Thermal Impedance



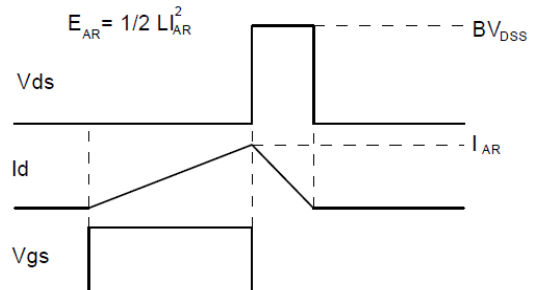
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

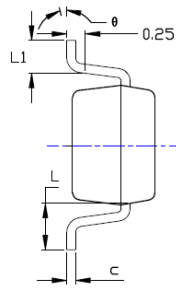
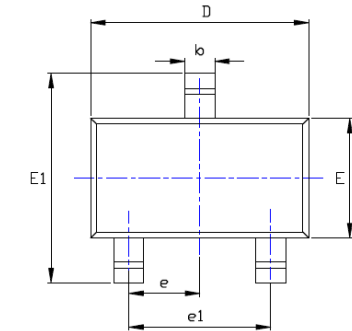


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



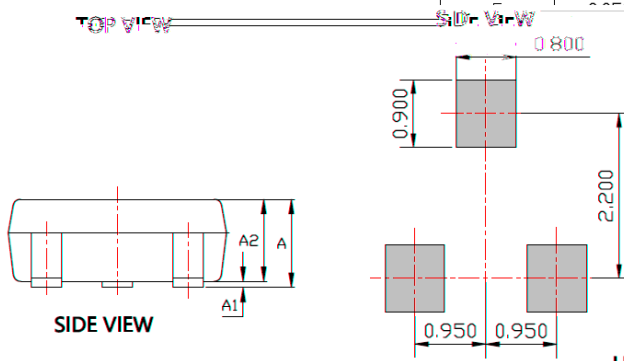
# YJL3401AL

## ■ SOT-23-3L Package Information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.041	0.049	1.050	1.250
A1	0.000	0.008	0.000	0.200
A2	0.041	0.045	1.050	1.150
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.111	0.119	2.820	3.020

0.116	2.650	2.950
0.079	1.800	2.000
0.024	0.300	0.600
8°	0°	8°



L1	0.104
e	0.037TYP
e1	0.071
L	0.024REF
L1	0.012
∅	0°

EXCLUDE MOLD FLASH AND  
LESS OTHERWISE SPECIFIED.  
OR REFERENCE PURPOSES

**NOTE:**  
1. PACKAGE BODY SIZES  
GATE BURRS.  
2. TOLERANCE 0.1mm UN  
3. THE PAD LAYOUT IS FC  
ONLY.

UNIT: mm

SUGGESTED SOLDER PAD LAYOUT



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