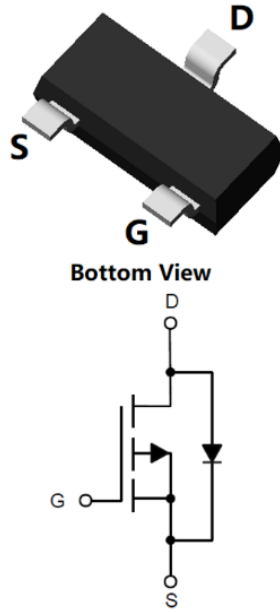
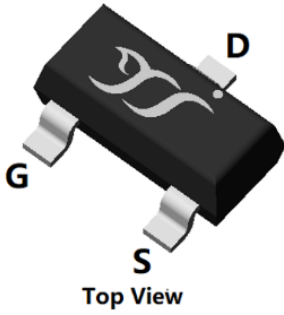


P-Channel Enhancement Mode Field Effect Transistor



SOT-23

Product Summary

- V_{DS} -20V
- I_D -5.4A
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <39mohm
- $R_{DS(ON)}$ (at $V_{GS}=-2.5V$) <49mohm
- $R_{DS(ON)}$ (at $V_{GS}=-1.8V$) <63mohm
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- High Power and Current handling capability
- Low Gate Charge

Applications

- Battery protection
- Power management
- Load switch

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	± 10	V
Drain Current	$T_A=25^\circ C$	I_D	-5.4	A
	$T_A=70^\circ C$		-4.4	
Pulsed Drain Current ^A		I_{DM}	-22	A
Total Power Dissipation	$T_A=25^\circ C$	P_D	1.2	W
	$T_A=70^\circ C$		0.8	W
Thermal Resistance Junction-to-Ambient ^B		$R_{\theta JA}$	104	$^\circ C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL2305B	F2	S5B.	3000	30000	120000	7" reel



YJL2305B

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±10V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-0.4	-0.62	-1.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-4.5V, I _D =-5.4A		27	39	mΩ
		V _{GS} =-2.5V, I _D =-4A		36	49	
		V _{GS} =-1.8V, I _D =-3A		48	63	
Diode Forward Voltage	V _{SD}	I _S =-5.4A, V _{GS} =0V			-1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, f=1MHZ		1010		pF
Output Capacitance	C _{oss}			130		
Reverse Transfer Capacitance	C _{rss}			109		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-4.5V, V _{DS} =-10V, I _D =-4A		10.98		nC
Gate-Source Charge	Q _{gs}			2.17		
Gate-Drain Charge	Q _{gd}			2.54		
Reverse Recovery Charge	Q _{rr}	I _F =-4A, di/dt=100A/us		4.38		ns
Reverse Recovery Time	t _{rr}			24.8		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-4.5V, V _{DS} =-10V, R _L =2.5Ω R _{GEN} =3Ω		8.4		ns
Turn-on Rise Time	t _r			36.2		
Turn-off Delay Time	t _{D(off)}			76.8		
Turn-off fall Time	t _f			56.2		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



Typical Performance Characteristics

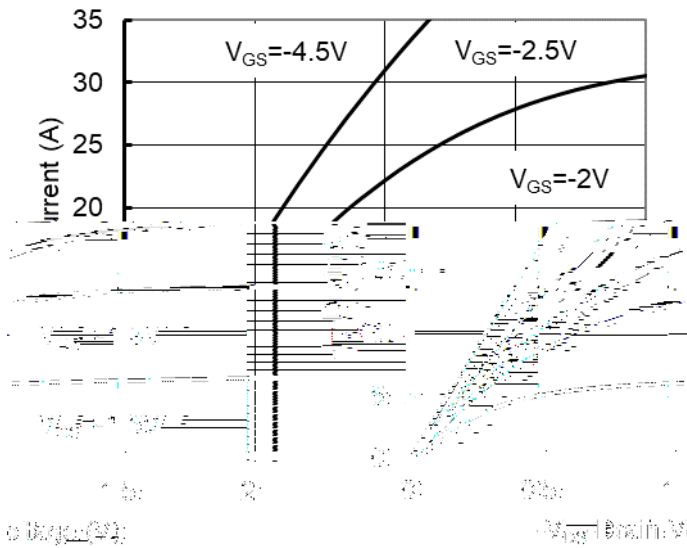


Figure1. Output Characteristics

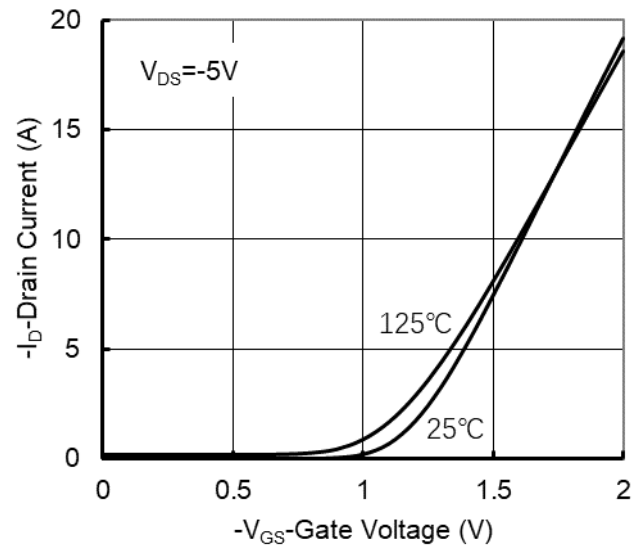


Figure2. Transfer Characteristics

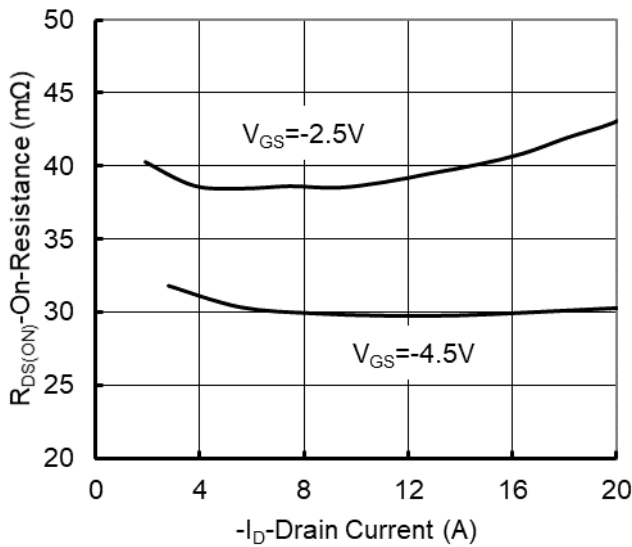


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

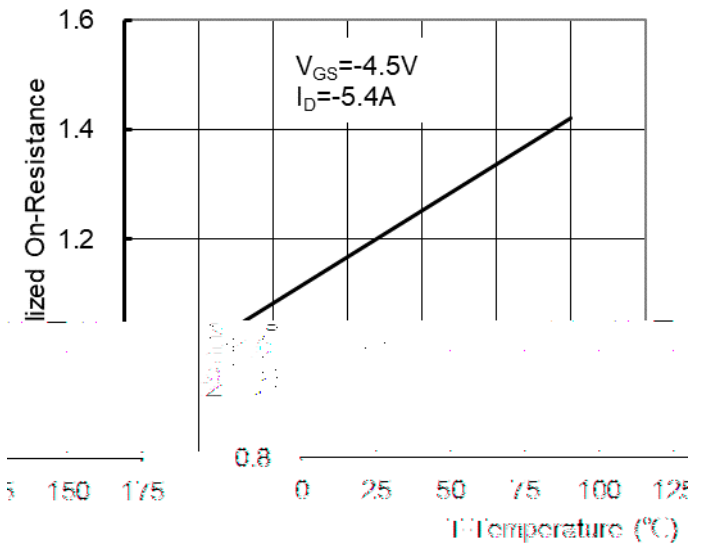


Figure 4: On-Resistance vs. Junction Temperature

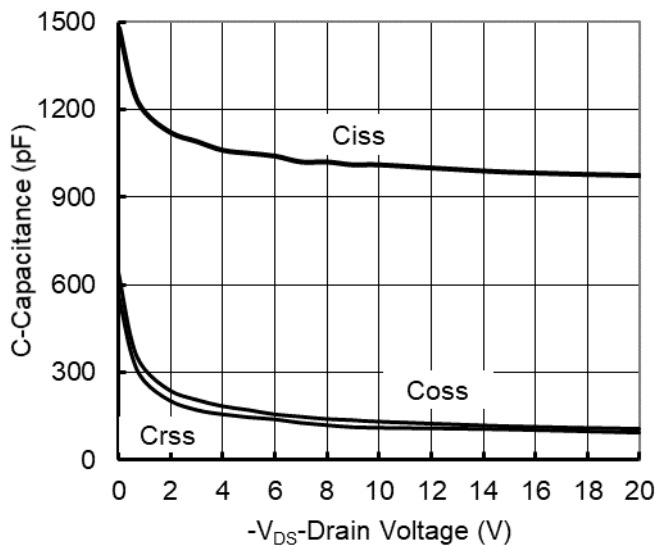


Figure5. Capacitance Characteristics

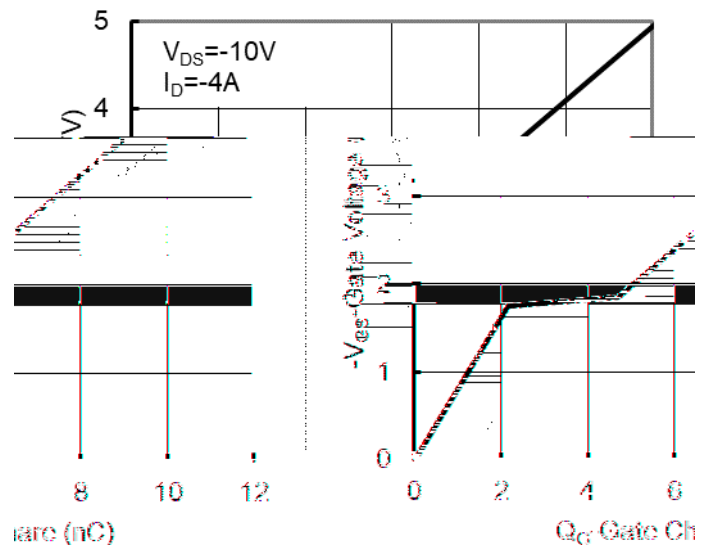


Figure6. Gate Charge



YJL2305B

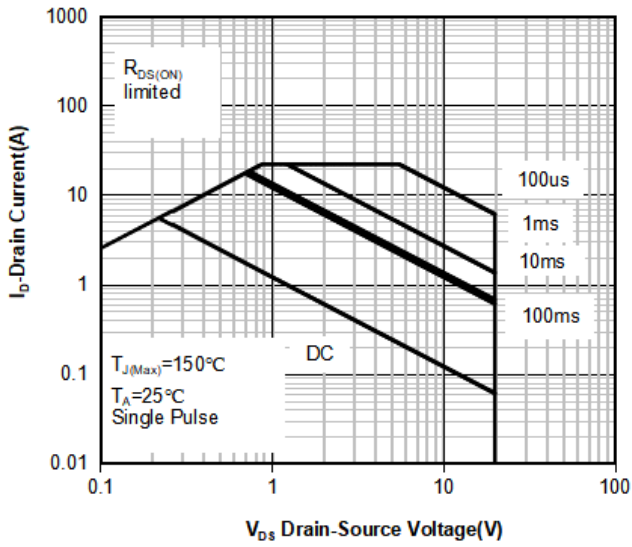


Figure7. Safe Operation Area

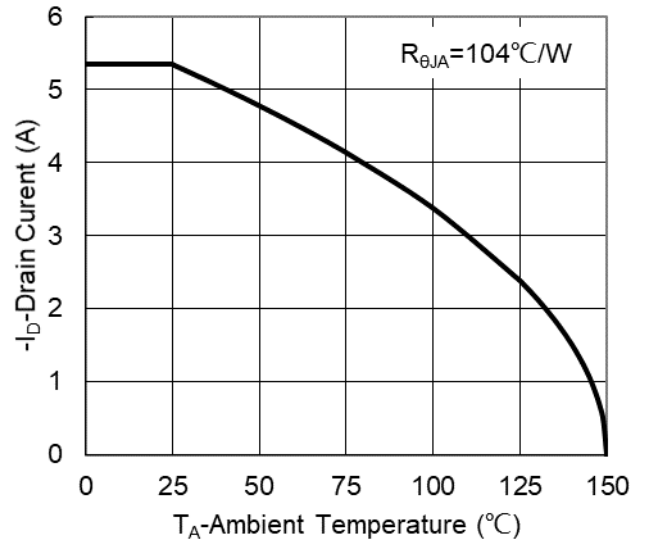


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

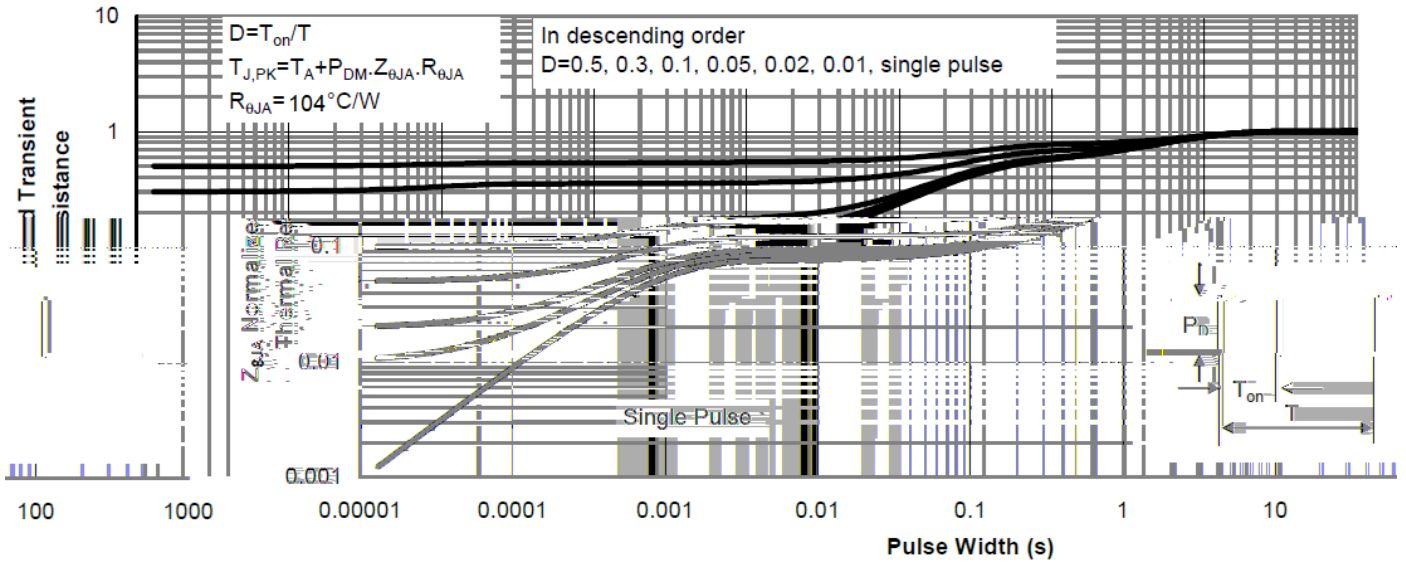
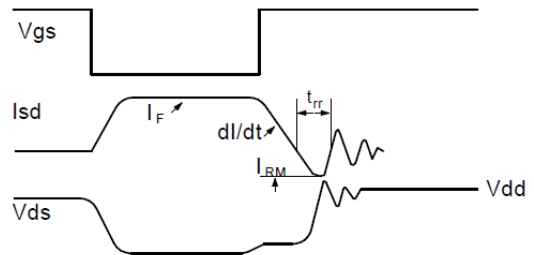
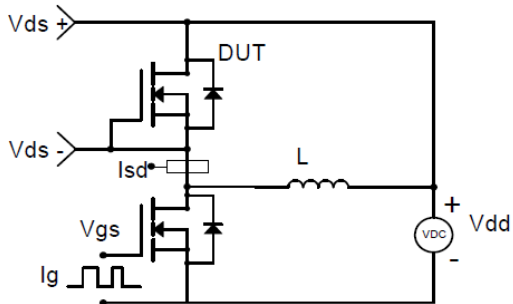


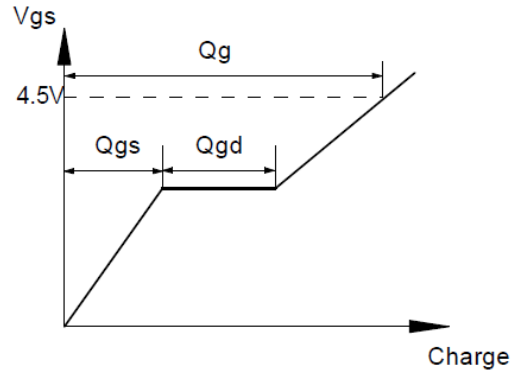
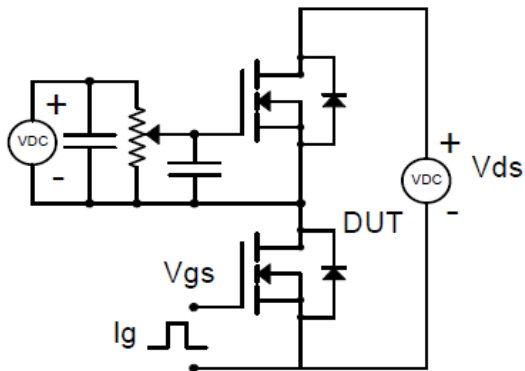
Figure9. Normalized Maximum Transient Thermal Impedance



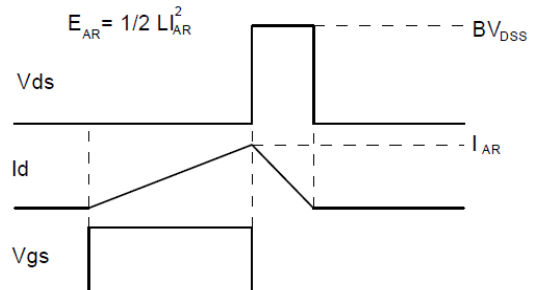
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



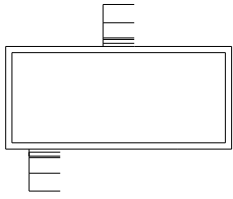
Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



■ SOT-23 Package Information



TOP VIEW



SIDE VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT



YJL2305B

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