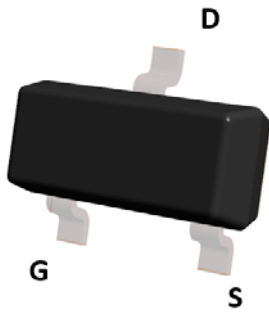
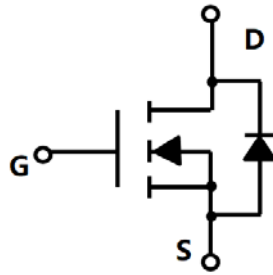
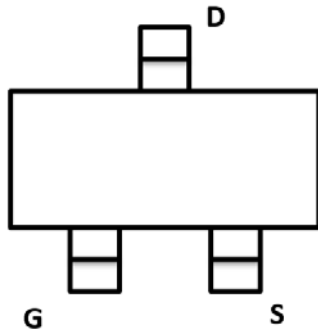


## N-Channel Enhancement Mode Field Effect Transistor



Top View

**SOT-23**



### Product Summary

$V_{DS}$	20V
$I_D$	4.3A
$R_{DS(ON)}$ ( at $V_{GS}= 4.5V$ )	27mohm
$R_{DS(ON)}$ ( at $V_{GS}= 2.5V$ )	37mohm

### General Description

Trench Power LV MOSFET technology  
High Density Cell Design for Low  $R_{DS(ON)}$   
High Speed switching  
Part no. with suffix "Q" means AEC-Q101 qualified

### Applications

Battery protection  
Load switch  
Power management

### Absolute Maximum Ratings ( $T_A=25$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-source Voltage	$V_{DS}$	20	V	
Gate-source Voltage	$V_{GS}$	$\pm 10$	V	
Drain Current	$I_D$	$T_A=25$	4.3	A
		$T_A=70$	3.4	
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	17.2	A	
Total Power Dissipation @ $T_A=25$ Steady State	$P_D$	1	W	
Thermal Resistance Junction-to-Ambient <sup>B</sup>	$R_{JA}$	125	/W	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 +150		

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL2302AQ	F2	.2302.	3000	30000	120000	7" reel



# YJL2302AQ

## Electrical Characteristics (T<sub>J</sub>=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> = 250μA	20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	0.55	0.85	1.25	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 4.3A		21	27	m
		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 3.0A		28	37	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 4.3A, V <sub>GS</sub> =0V		0.8	1.2	V
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1MHZ		602		pF
Output Capacitance	C <sub>oss</sub>			79		
Reverse Transfer Capacitance	C <sub>rss</sub>			62		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 4.5V, V <sub>DS</sub> = 10V, I <sub>D</sub> = 4.3A		6.5		nC
Gate-Source Charge	Q <sub>gs</sub>			1.6		
Gate-Drain Charge	Q <sub>gd</sub>			1.5		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 15A, di/dt=100A/us		0.6		
Reverse Recovery Time	t <sub>rr</sub>			9.9		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> = 4.5V, V <sub>DS</sub> = 10V, I <sub>D</sub> = 6.7A R <sub>GEN</sub> = 3		8		ns
Turn-on Rise Time	t <sub>r</sub>			58		
Turn-off Delay Time	t <sub>D(off)</sub>			20		
Turn-off fall Time	t <sub>f</sub>			68		

A. Pulse Test: Pulse Width 300us, Duty cycle 2%.

B. R<sub>JA</sub> is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. R<sub>JL</sub> is guaranteed by design, while R<sub>JA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



## ■ Typical Performance Characteristics

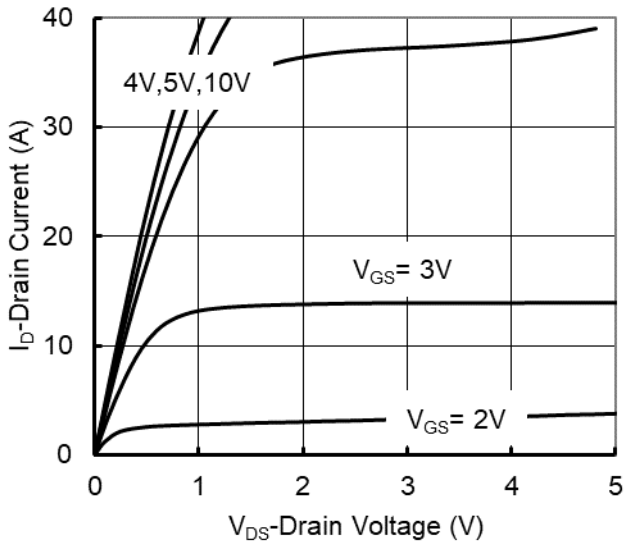


Figure1. Output Characteristics

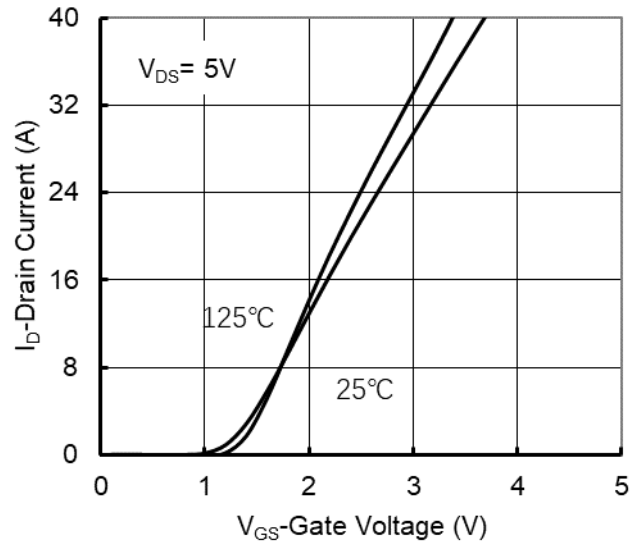


Figure2. Transfer Characteristics

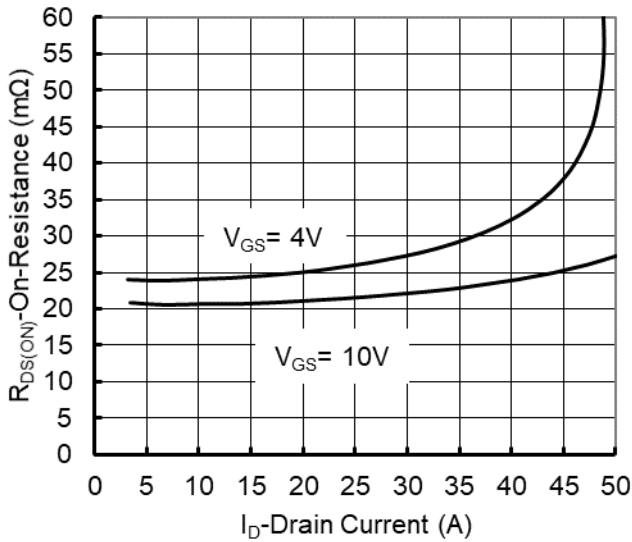


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

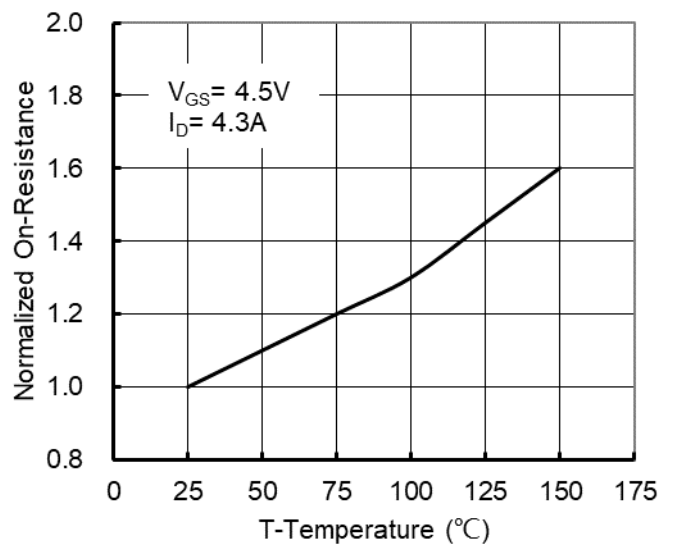


Figure 4: On-Resistance vs. Junction Temperature

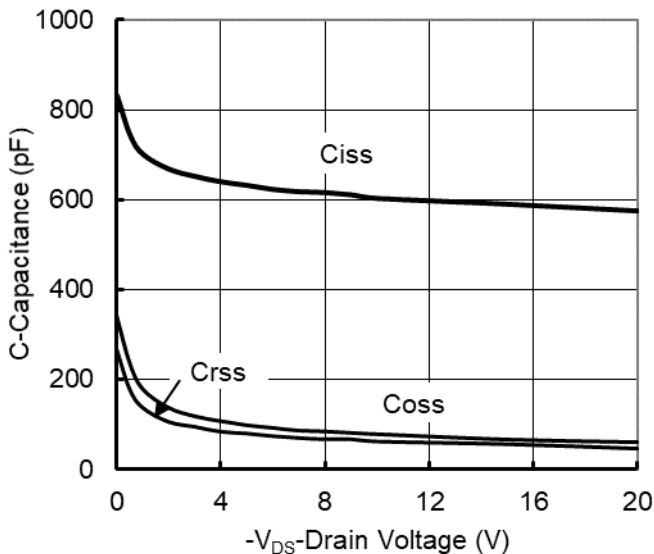


Figure5. Capacitance Characteristics

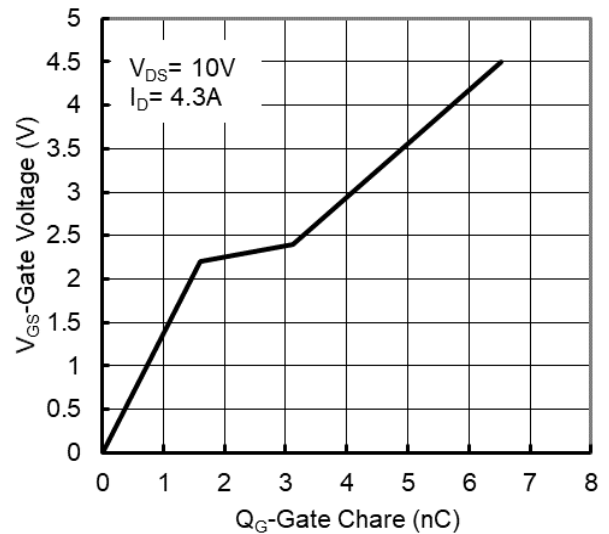


Figure6. Gate Charge



# YJL2302AQ

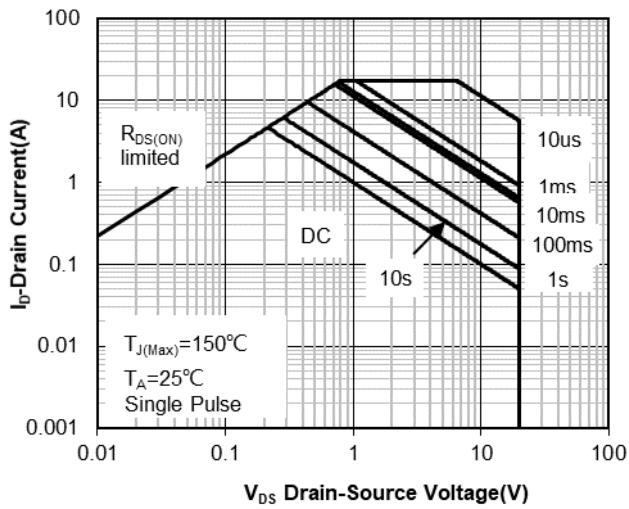


Figure7. Safe Operation Area

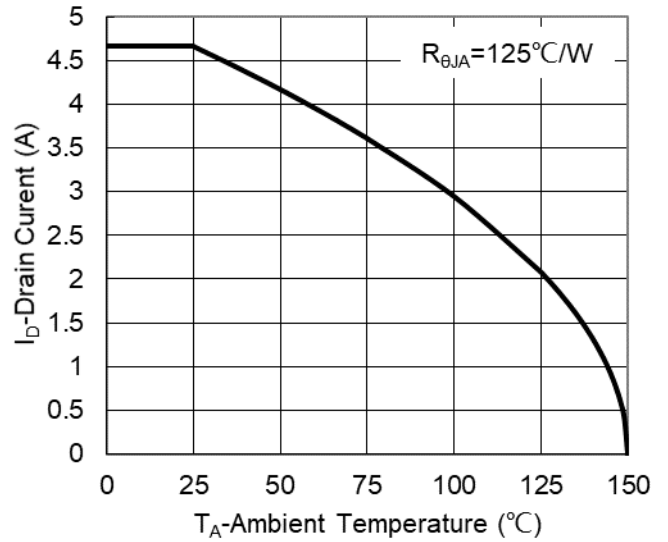


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

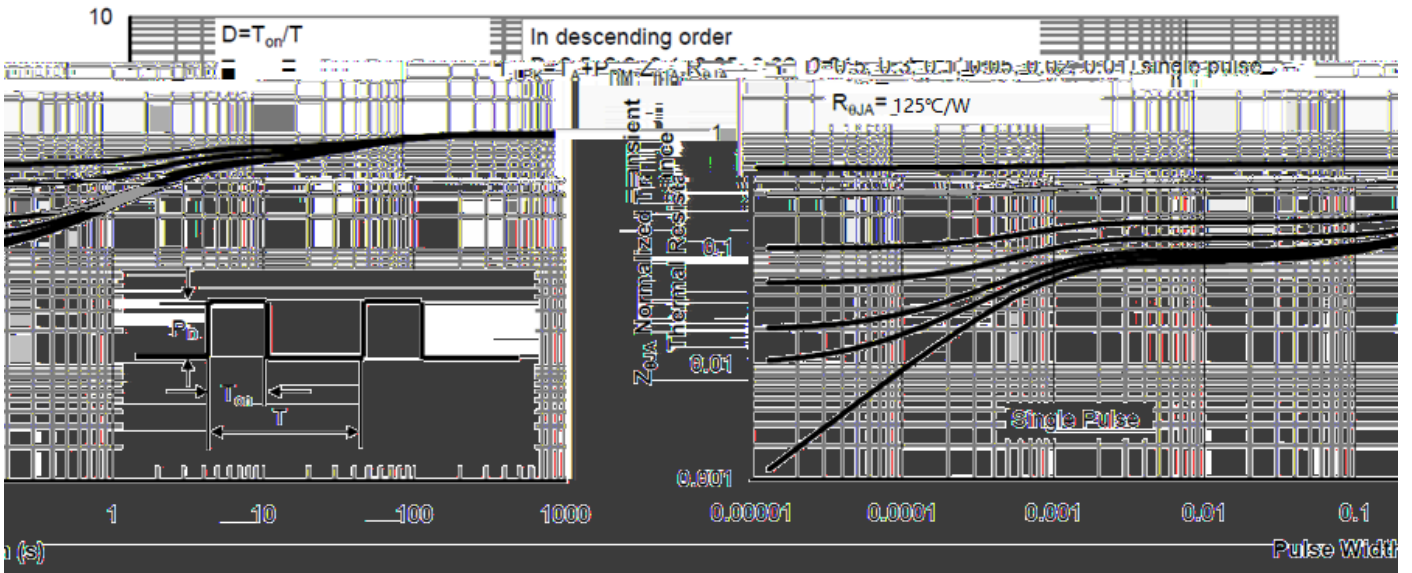
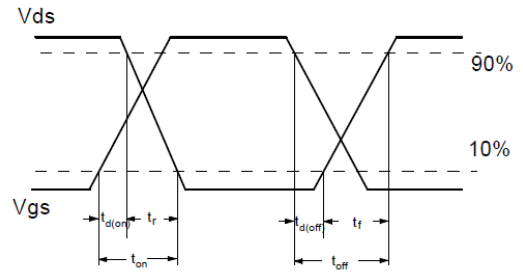
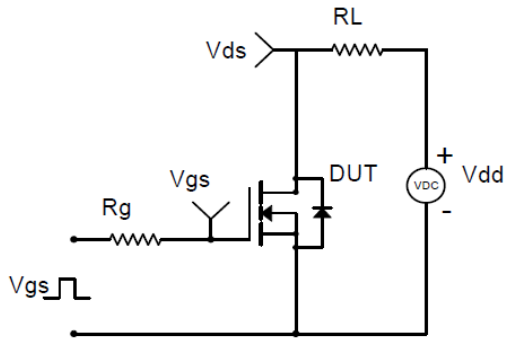
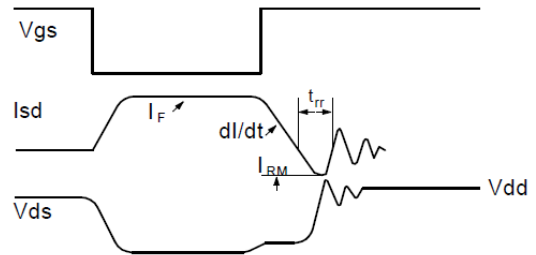
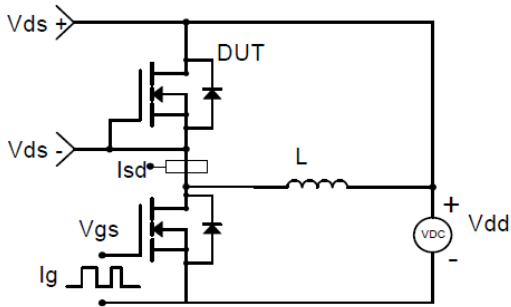


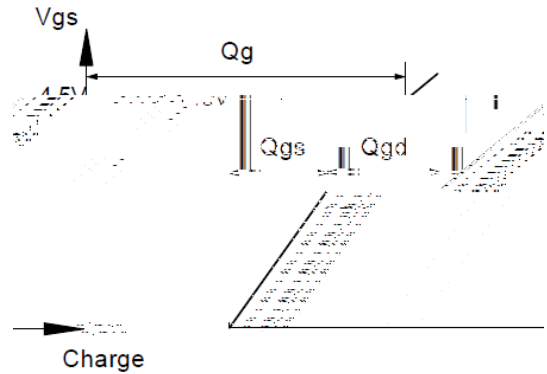
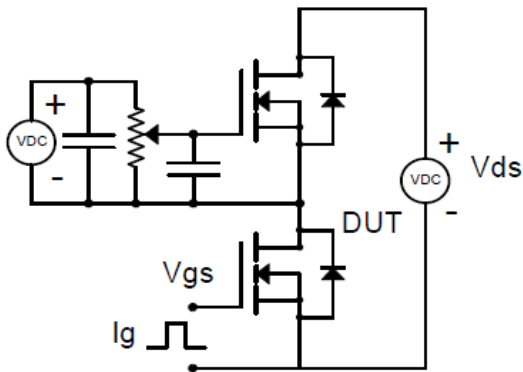
Figure9. Normalized Maximum Transient Thermal Impedance



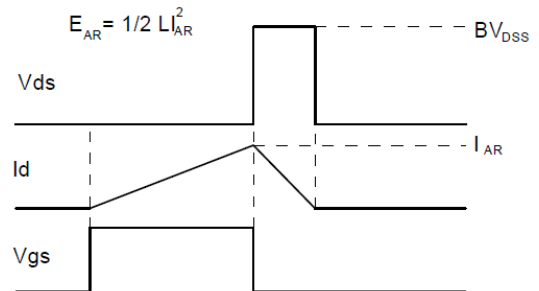
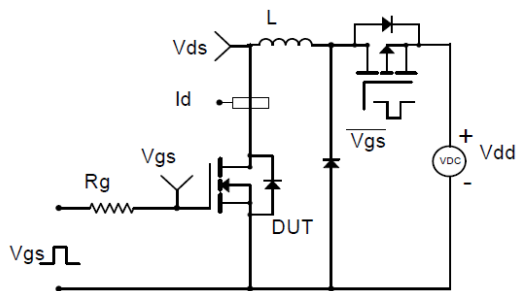
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

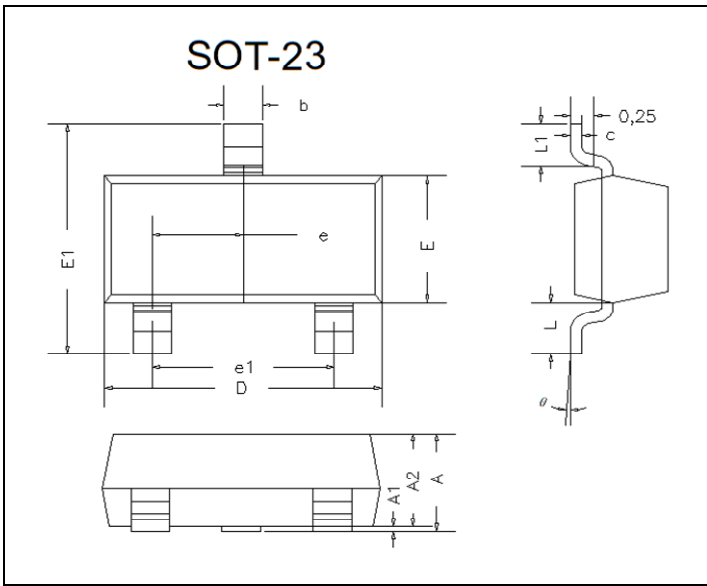


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



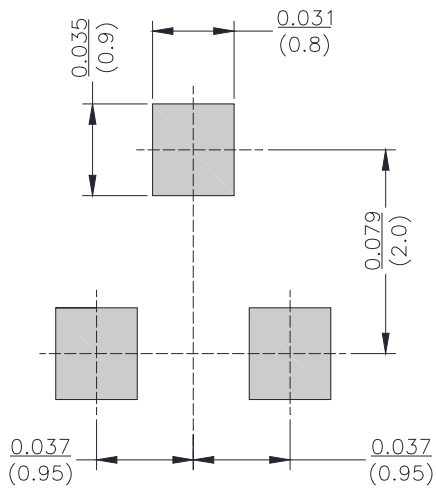
# YJL2302AQ

## SOT-23 Package information



DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	0.035	0.045	0.90	1.15	
A1	0.000	0.004	0.00	0.10	
A2	0.035	0.041	0.90	1.05	
b	0.012	0.020	0.30	0.50	
c	0.004	0.008	0.10	0.20	
D	0.110	0.118	2.80	3.00	
E	0.047	0.055	1.20	1.40	
E1	0.089	0.100	2.25	2.55	
e	0.370TYP		0.95TYP		
e1	0.071	0.079	1.80	2.00	
L	0.220REF		0.55REF		
L1	0.012	0.020	0.30	0.50	
	0°	8°	0°	8°	

## SOT-23 Suggested Pad Layout





## Disclaimer

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