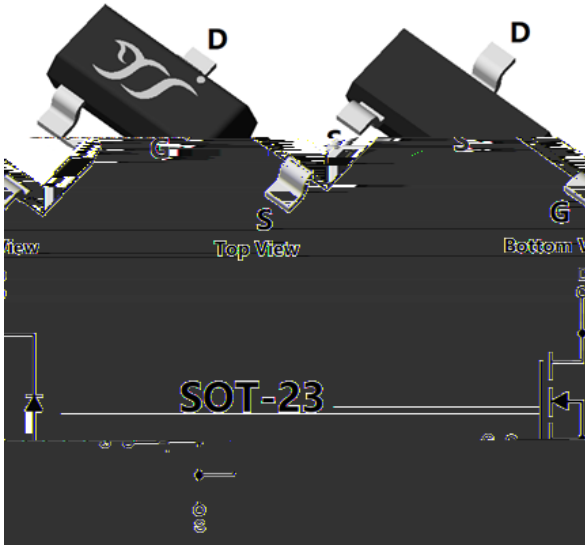


## N-Channel Enhancement Mode Field Effect Transistor



### Product Summary

$V_{DS}$	100V
$I_D$	3A
$R_{DS(ON)}$ ( at $V_{GS}=10V$ )	<140 mohm
$R_{DS(ON)}$ ( at $V_{GS}=4.5V$ )	<300 mohm

### General Description

Split Gate Trench MOSFET technology  
 Excellent package for heat dissipation  
 High density cell design for low  $R_{DS(ON)}$   
 Moisture Sensitivity Level 1  
 Epoxy Meets UL 94 V-0 Flammability Rating  
 Halogen Free

### Applications

DC-DC Converters  
 Power management functions

### Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	100	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current	$I_D$	$T_A=25^\circ\text{C}$	3
		$T_A=70^\circ\text{C}$	2.4
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	12	A
Avalanche energy <sup>B</sup>	$E_{AS}$	8	mJ
Total Power Dissipation <sup>C</sup>	$P_D$	$T_A=25^\circ\text{C}$	1.2
		$T_A=70^\circ\text{C}$	0.8
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### Thermal resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	R	82	104	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Ambient <sup>D E</sup>		Steady-State	111	
Thermal Resistance Junction-to-Case	$R_{L}$	43	52	

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL03G10A	F2	1003.	3000	30000	120000	7



# YJL03G10A

## Electrical Characteristics (T<sub>j</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250	100			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V			1	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250	1.0	1.8	3.0	V
Static Drain-Source On-Resistance	R <sub>D(S)ON</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =3A		110	140	m
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =2A		160	300	m
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =3A, V <sub>GS</sub> =0V			1.3	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				3	A
Gate resistance	R <sub>G</sub>	f= 1 MHz, Open drain		8		
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, f=100KHZ		206		pF
Output Capacitance	C <sub>oss</sub>			28.9		
Reverse Transfer Capacitance	C <sub>rss</sub>			1.4		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =3A		4.3		nC
Gate-Source Charge	Q <sub>gs</sub>			1.5		
Gate-Drain Charge	Q <sub>gd</sub>			1.1		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =3A, di/dt=100A/us		39.4		ns
Reverse Recovery Time	t <sub>rr</sub>			32.1		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =50V, I <sub>D</sub> =3A R <sub>GEN</sub> =2		14.7		ns
Turn-on Rise Time	t <sub>r</sub>			3.5		
Turn-off Delay Time	t <sub>D(off)</sub>			20.9		
Turn-off fall Time	t <sub>f</sub>			2.7		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V<sub>DD</sub>=50V, R<sub>G</sub> 0.5mH.

C. Pd is based on max. junction temperature, using ≤10us junction-to-ambient thermal resistance.

D. The value of R is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25°C. The value in any given application depends on the user's specific board design.

E. The R is the sum of the thermal impedance from junction to lead R<sub>L</sub> and lead to ambient



## ■ Typical Performance Characteristics

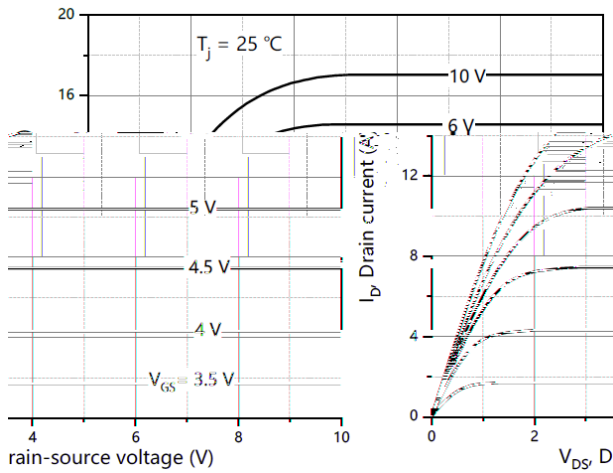


Figure1. Output Characteristics

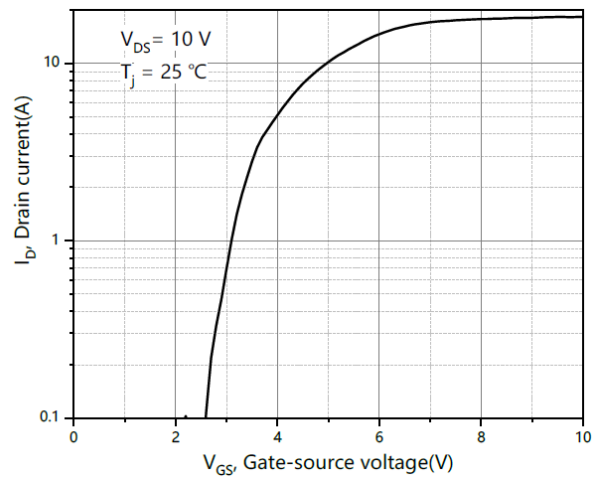


Figure2. Transfer Characteristics

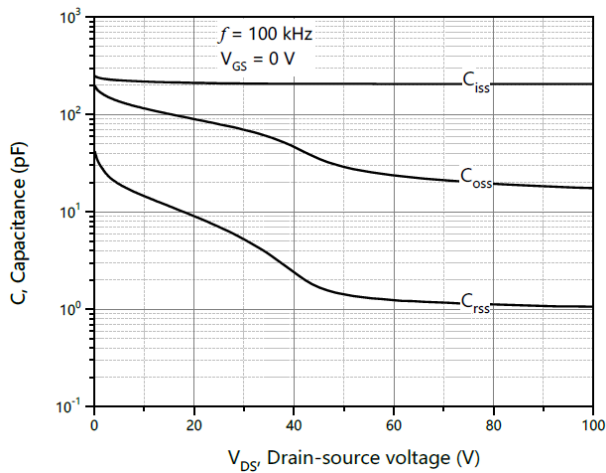


Figure3. Capacitance Characteristics

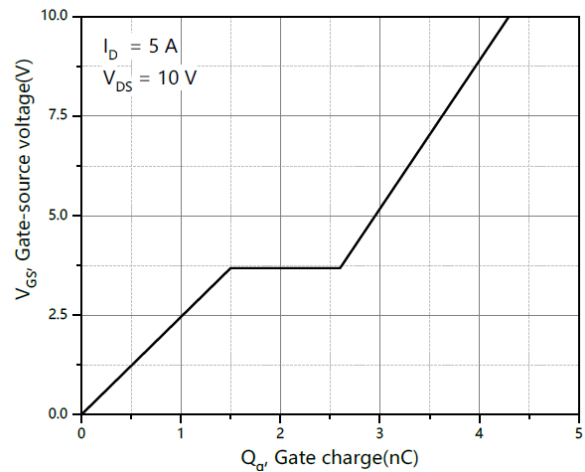


Figure4. Gate Charge

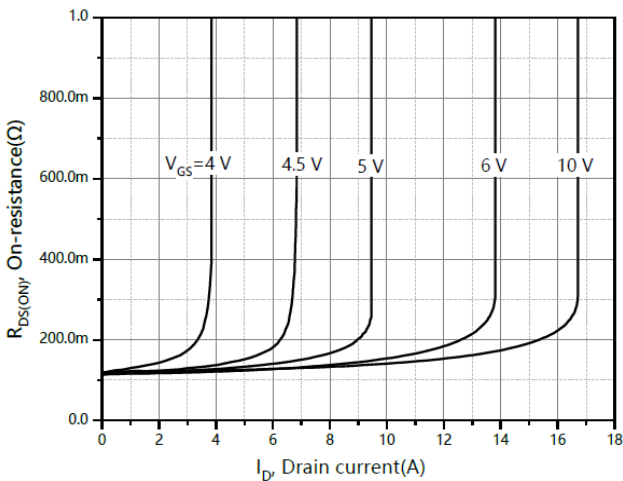


Figure5. : On-Resistance vs. Drain Current and Gate Voltage

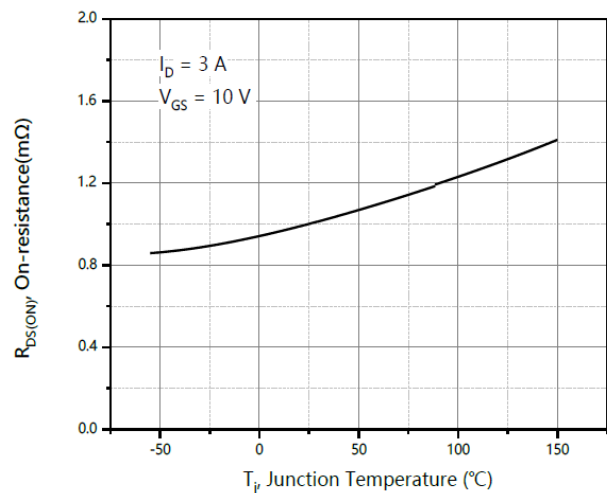


Figure6. Normalized On-Resistance



# YJL03G10A

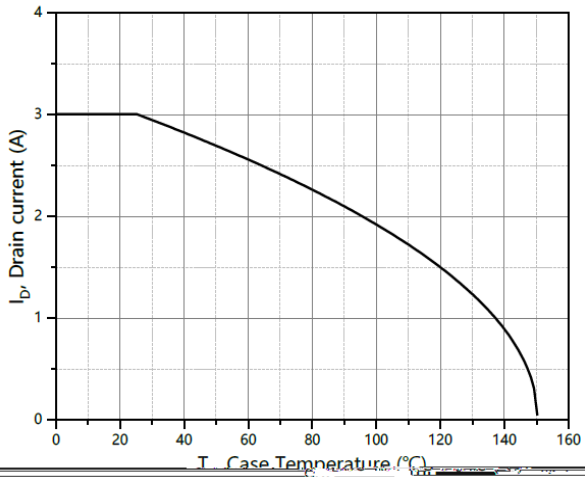


Figure7. Drain current

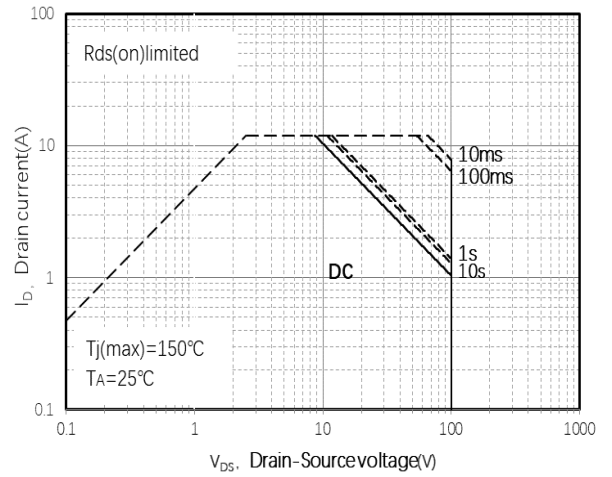


Figure8.Safe Operation Area

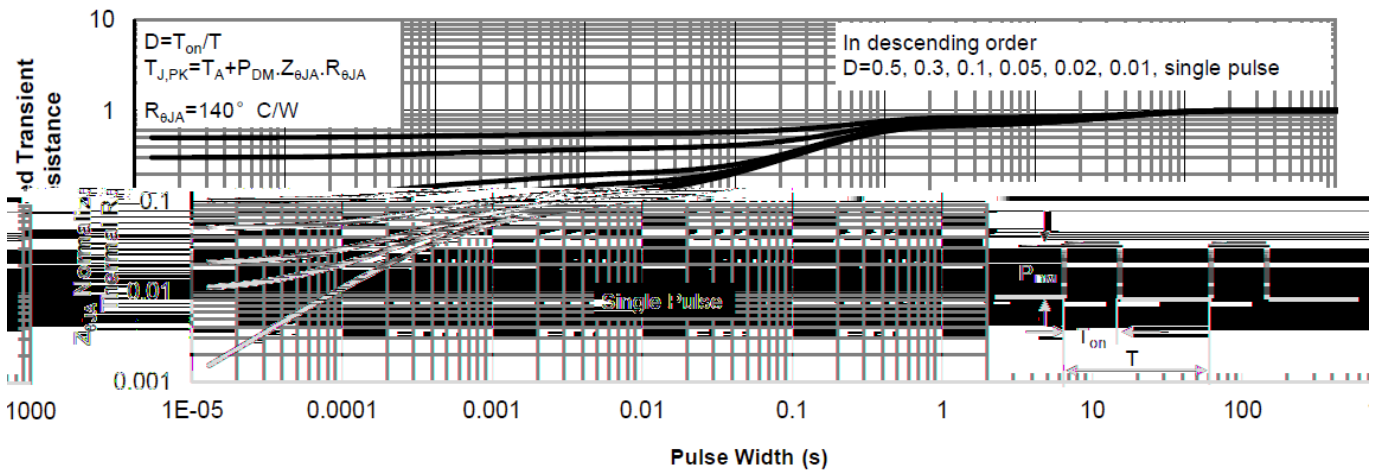


Figure9.Normalized Maximum Transient thermal impedance

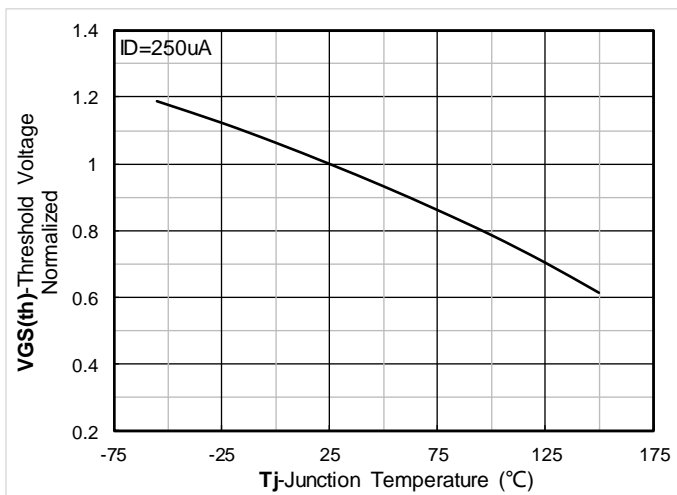
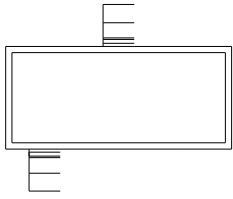


Figure10. Normalized Threshold voltage



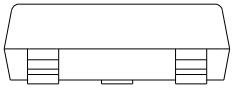
SOT-23 Package information



TOP VIEW



SIDE VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT



## YJL03G10A

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