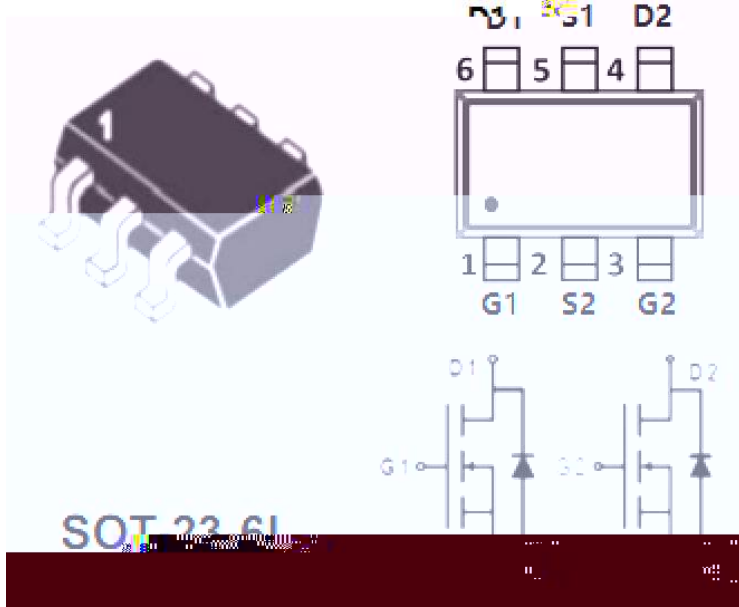




# YJJ2322A

## N-Channel Enhancement Mode Field Effect Transistor



### Product Summary

$V_{DS}$	20V
$I_D$	4.3A
$R_{DS(ON)}$ ( at $V_{GS}= 4.5V$ )	< 30mohm
$R_{DS(ON)}$ ( at $V_{GS}= 2.5V$ )	< 40mohm

### General Description

Trench Power LV MOSFET technology  
 High Density Cell Design for Low  $R_{DS(ON)}$   
 High Speed switching

### Applications

Battery protection  
 Load switch  
 Power management

### Absolute Maximum Ratings ( $T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	20	V
Gate-source Voltage	$V_{GS}$	$\pm 10$	V

Drain Current  $T_A$



# YJJ2322A

## Electrical Characteristics ( $T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	20			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=20V, V_{GS}=0V$			1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 10V, V_{DS}=0V$			$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.55	0.85	1.25	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=3.6A$		21	30	m
		$V_{GS}=2.5V, I_D=3.1A$		28	40	
Diode Forward Voltage	$V_{SD}$	$I_S=4.3A, V_{GS}=0V$		0.8	1.2	V
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=10V, V_{GS}=0V, f=1\text{MHz}$		602		pF
Output Capacitance	$C_{oss}$			79		
Reverse Transfer Capacitance	$C_{rss}$			62		
<b>Switching Parameters</b>						
Total Gate Charge	$Q_g$	$V_{GS}=4.5V, V_{DS}=10V, I_D=4.3A$		6.5		nC
Gate-Source Charge	$Q_{gs}$			1.6		
Gate-Drain Charge	$Q_{gd}$			1.5		
Reverse Recovery Charge	$Q_{rr}$	$I_F=4.3A, di/dt=100A/\mu s$		0.6		ns
Reverse Recovery Time	$t_{rr}$			9.9		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=4.5V, V_{DS}=10V, I_D=4.3A$ $R_{GEN}=3$		8		ns
Turn-on Rise Time	$t_r$			58		
Turn-off Delay Time	$t_{D(off)}$			20		
Turn-off fall Time	$t_f$			68		

A. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ .

B.  $R_{JA}$  is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins.  $R_{JL}$  is guaranteed by design, while  $R_{JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



Typical Performance Characteristics

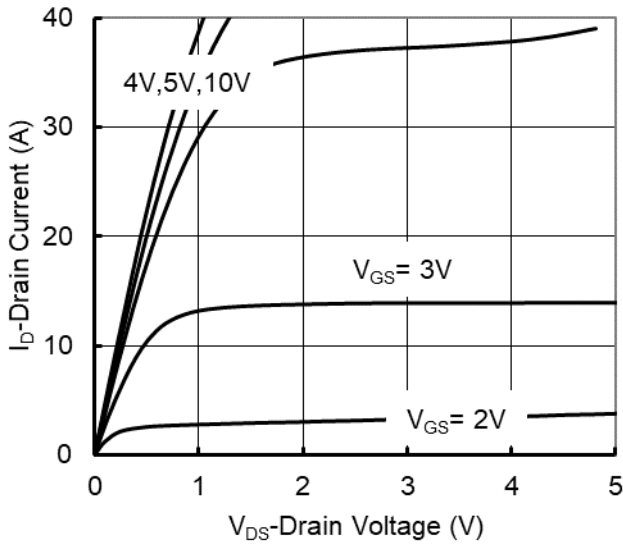


Figure1. Output Characteristics

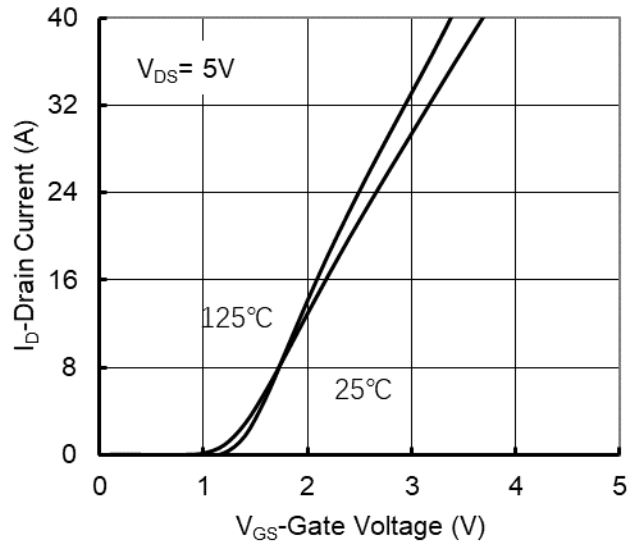


Figure2. Transfer Characteristics

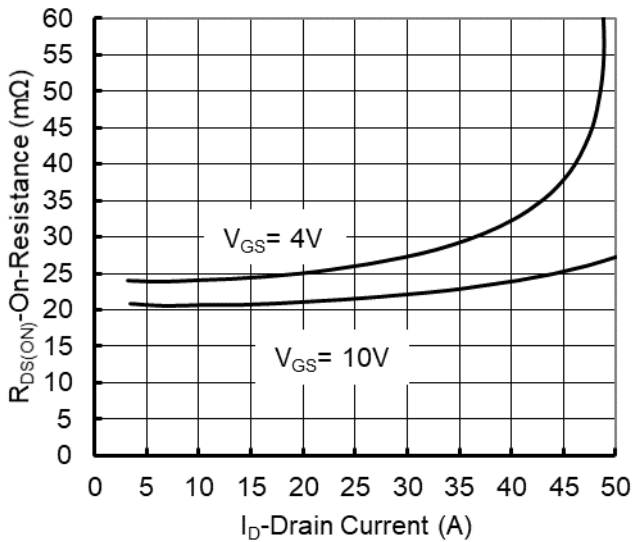


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

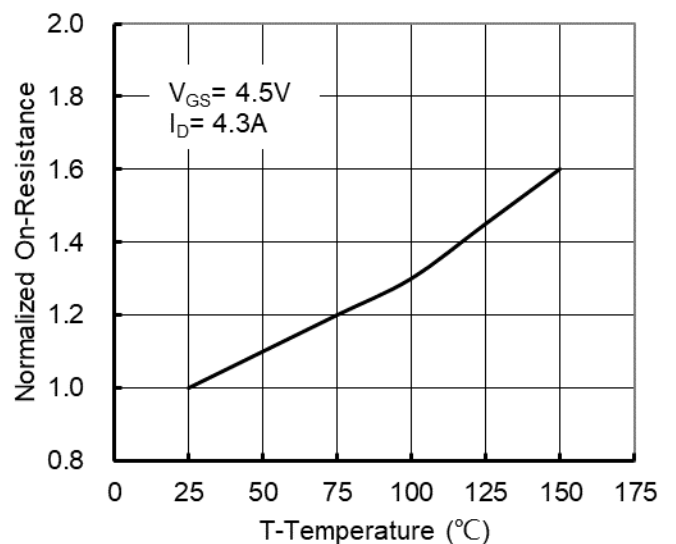


Figure 4: On-Resistance vs. Junction Temperature

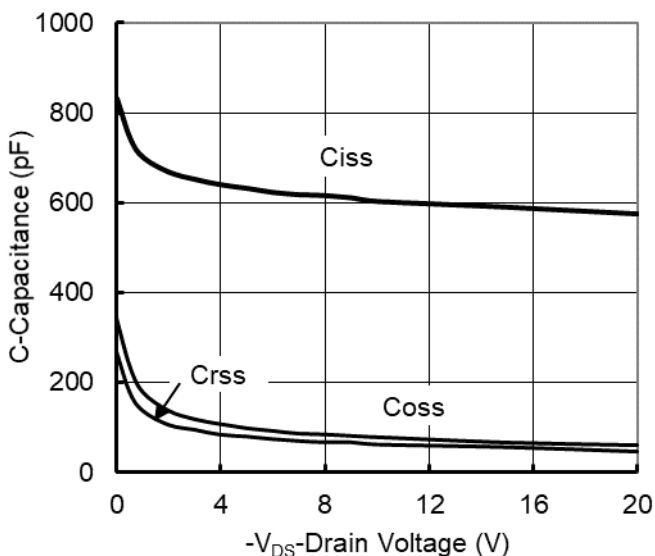


Figure5. Capacitance Characteristics

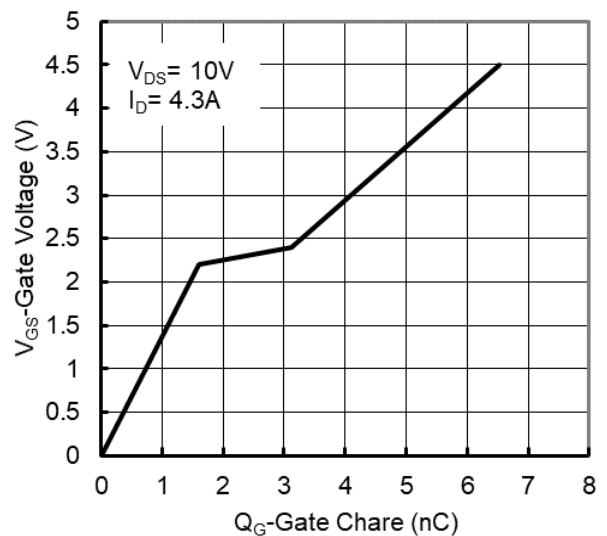


Figure6. Gate Charge

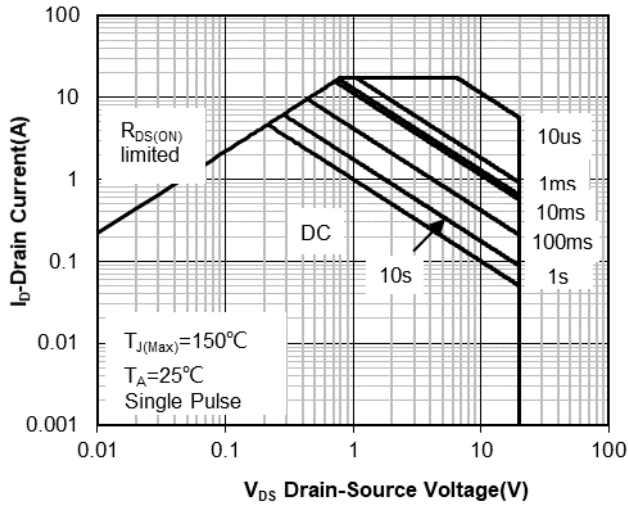


Figure7. Safe Operation Area

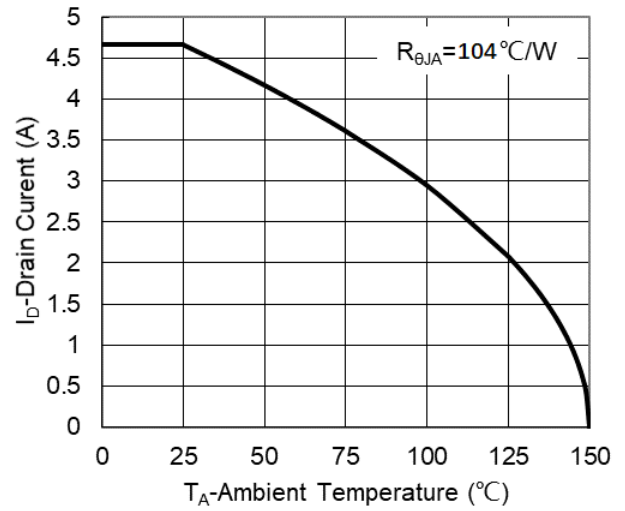


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

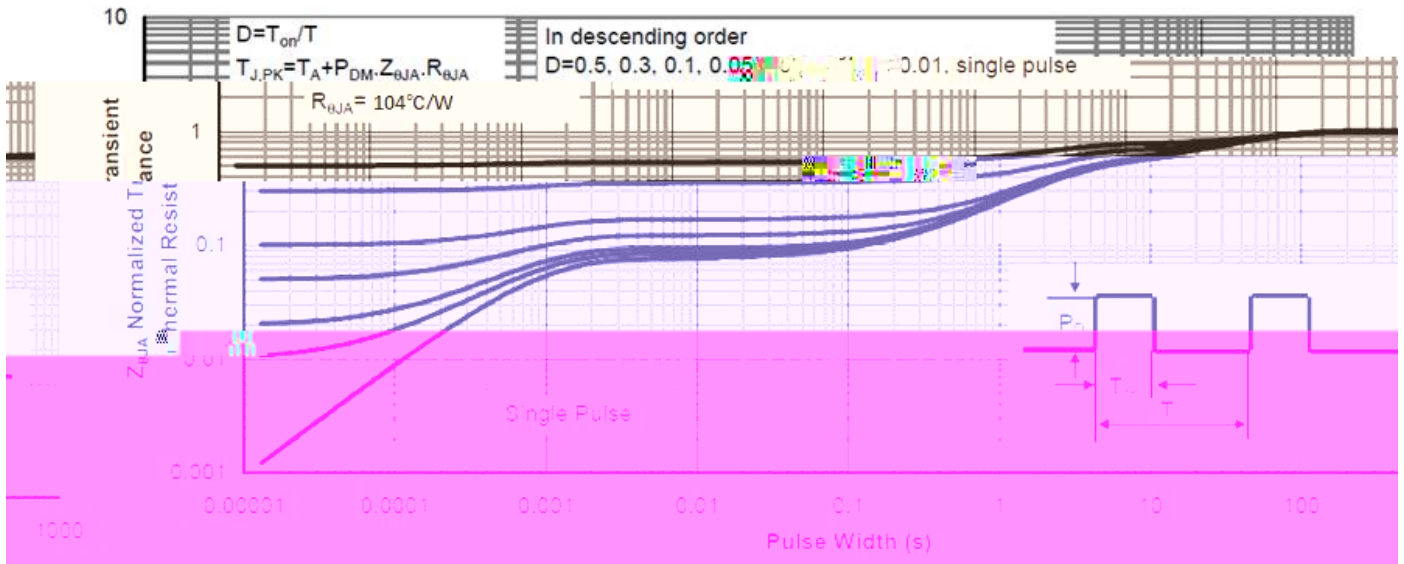
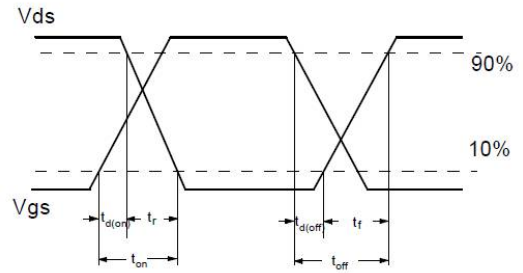
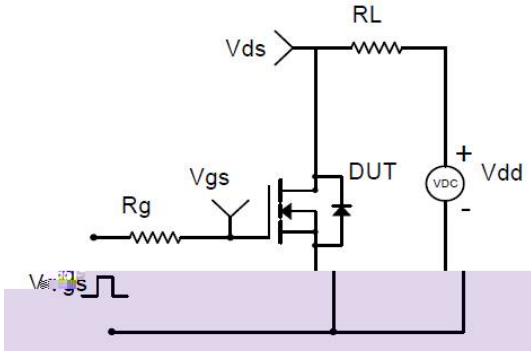
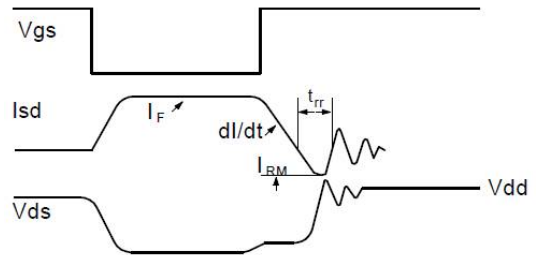
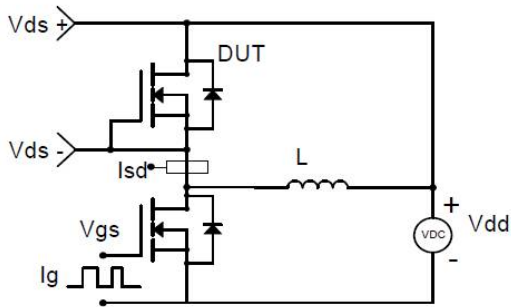


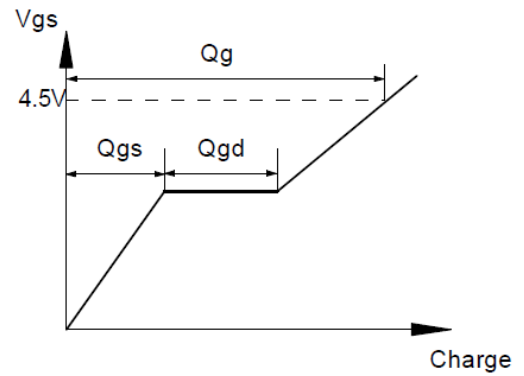
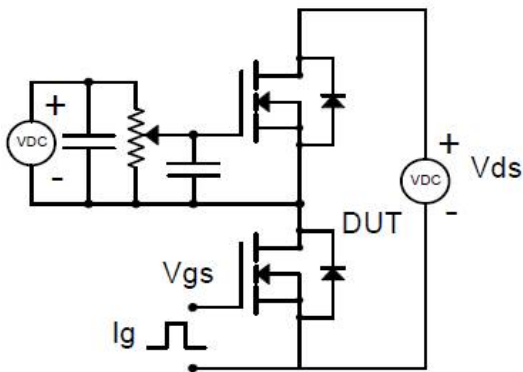
Figure9. Normalized Maximum Transient Thermal Impedance



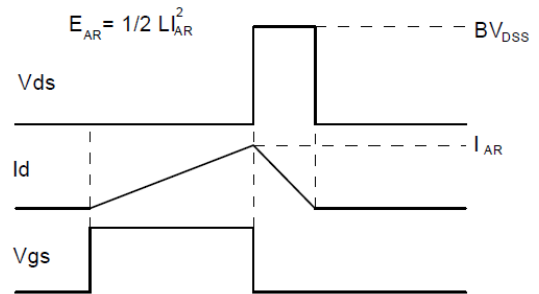
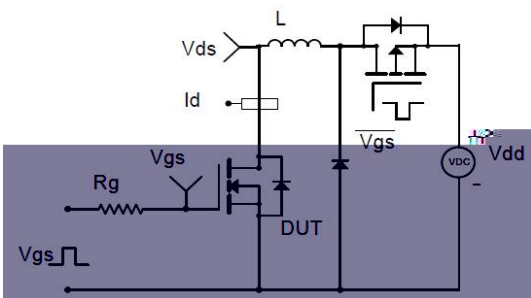
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

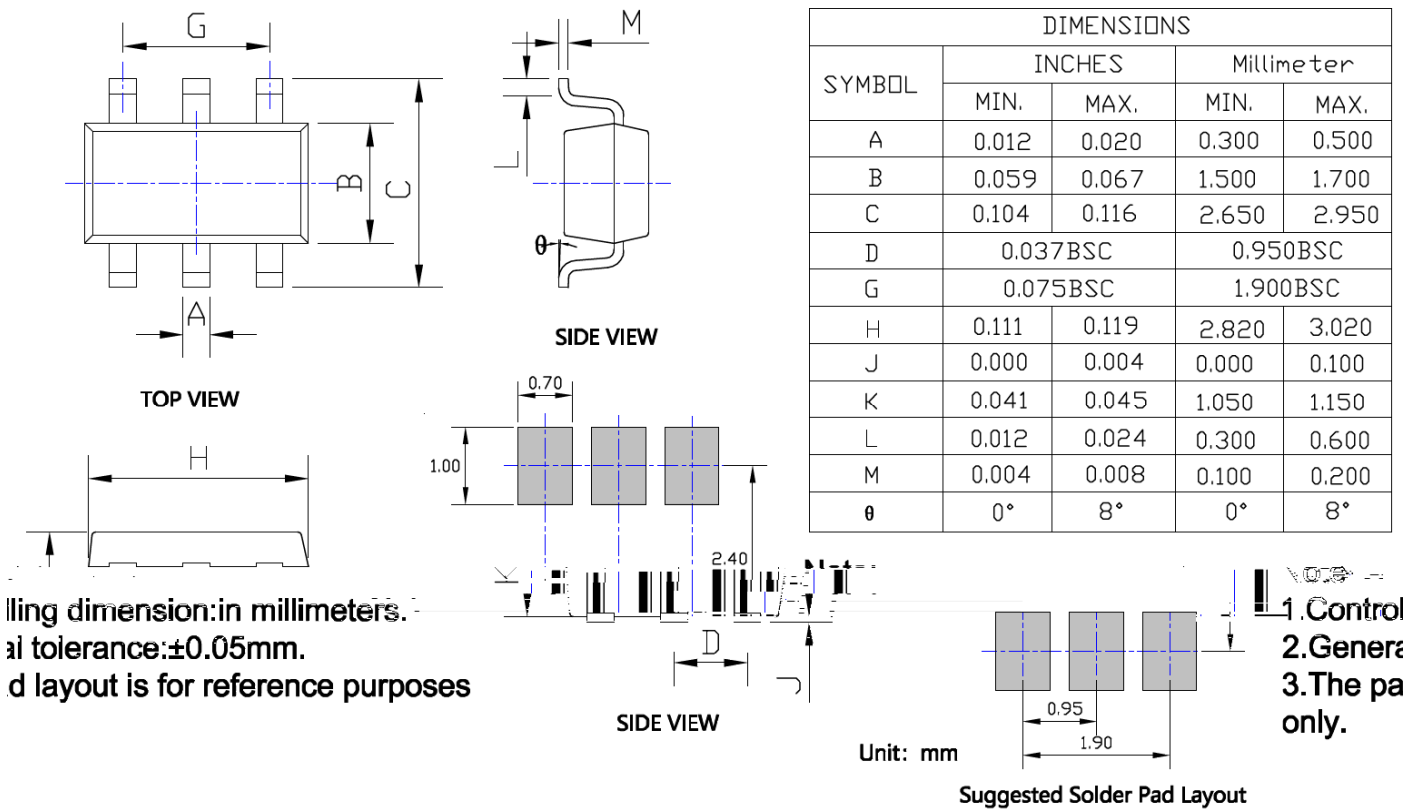


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



# YJJ2322A

## SOT-23-6L Package Information





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