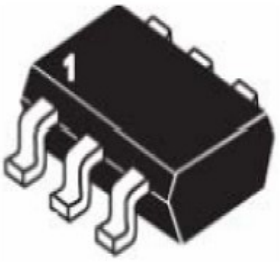
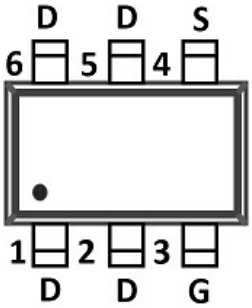
RoHS
COMPLIANT





- V_{DS} 20V
- I_D 8.0A
- $R_{DS(ON)}$(at V_{GS}= 4.5V) 18mohm
- $R_{DS(ON)}$(at V_{GS}= 2.5V) 22mohm
- $R_{DS(ON)}$(at V_{GS}= 1.8V) 39mohm

- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching

- Battery protection
- Load switch
- Power management

■ (T_A=25 unless otherwise noted)

Drain-source Voltage		V_{DS}	20	V
Gate-source Voltage		V_{GS}	10	V
Drain Current	T_A=25	I_D	8	A
	T_A=70		6.4	
Pulsed Drain Current [A]		I_{DM}	32	A
Total Power Dissipation @ T_A=25		P_D	1.5	W
Thermal Resistance Junction-to-Ambient [B]		$R_{\theta JA}$	83	/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +150	

■ (Example)

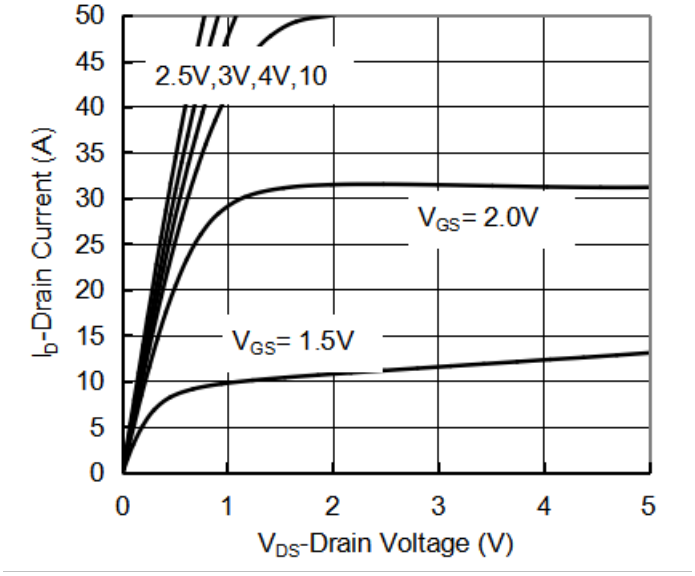
YJJ08N02A	F2	8N02	3000	30000	120000	7’

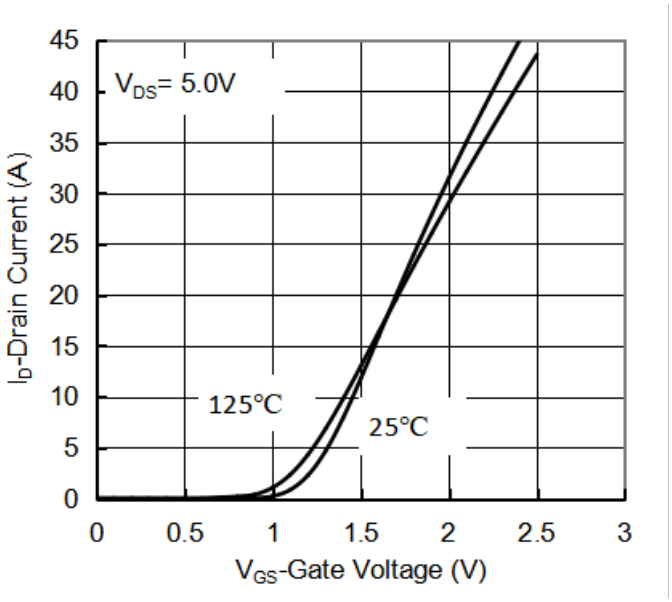
■ (T_J=25 unless otherwise noted)

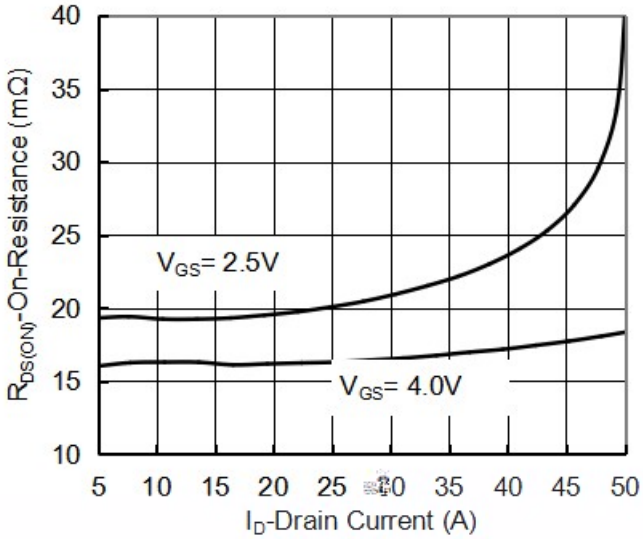
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= 10V, V_{DS}=0V			100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	0.45	0.62	1	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=5.0A		14	18	mΩ
		V_{GS}=2.5V, I_D=3.0A		17	22	
		V_{GS}=1.8V, I_D=1.5A		29	39	
Diode Forward Voltage	V_{SD}	I_S=5.0A,V_{GS}=0V			1.2	V
Input Capacitance	C_{iss}	V_{DS}=10V,V_{GS}=0V,f=1MHZ		888		pF
Output Capacitance	C_{oss}			133		
Reverse Transfer Capacitance	C_{rss}			117		
Total Gate Charge	Q_g	V_{GS}=4.5V,V_{DS}=10V,I_D=6.8A		11.1		nC
Gate-Source Charge	Q_{gs}			1.7		
Gate-Drain Charge	Q_{gd}			3.1		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=4.5V,V_{DD}=10V, I_D=6.8A, R_{GEN}=3Ω		7		
Turn-on Rise Time	t_r			46		
Turn-off Delay Time	$t_{D(off)}$			30		
Turn-off fall Time	t_f			52		

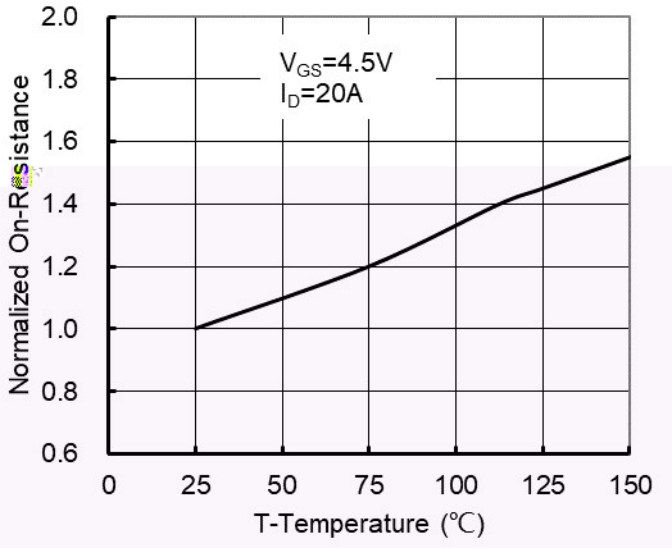
A. Pulse Test: Pulse Width 300us,Duty cycle 2%.

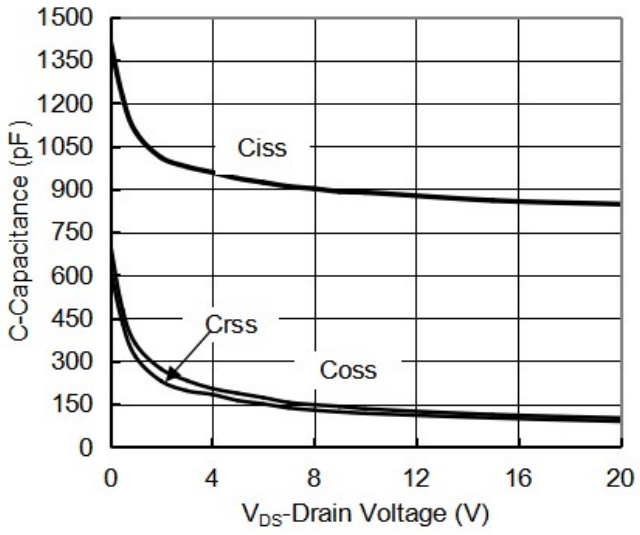
B. $R_{\theta JA}$ is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JL}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

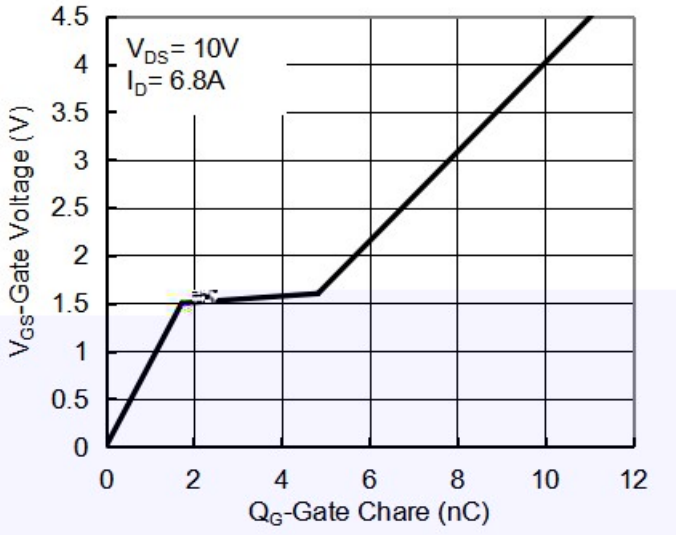

2.5V,3V,4V,10
V_{GS}= 2.0V
V_{GS}= 1.5V
I_D-Drain Current (A)
V_{DS}-Drain Voltage (V)

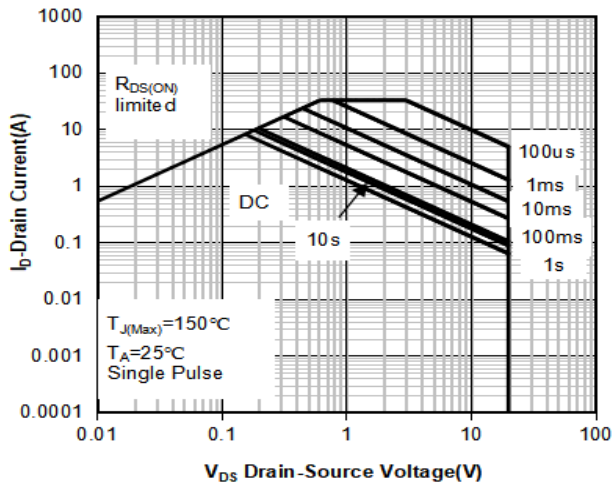

V_{DS}= 5.0V
125℃
25℃
I_D-Drain Current (A)
V_{GS}-Gate Voltage (V)

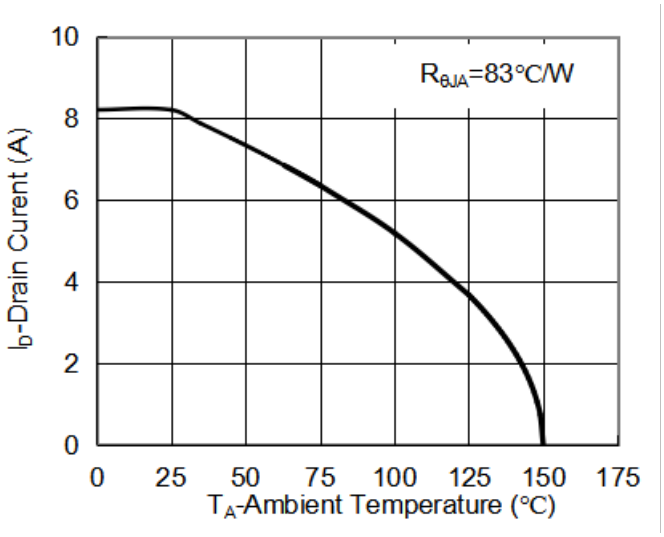

V_{GS}= 2.5V
V_{GS}= 4.0V
$R_{DS(ON)}$-On-Resistance (mΩ)
I_D-Drain Current (A)

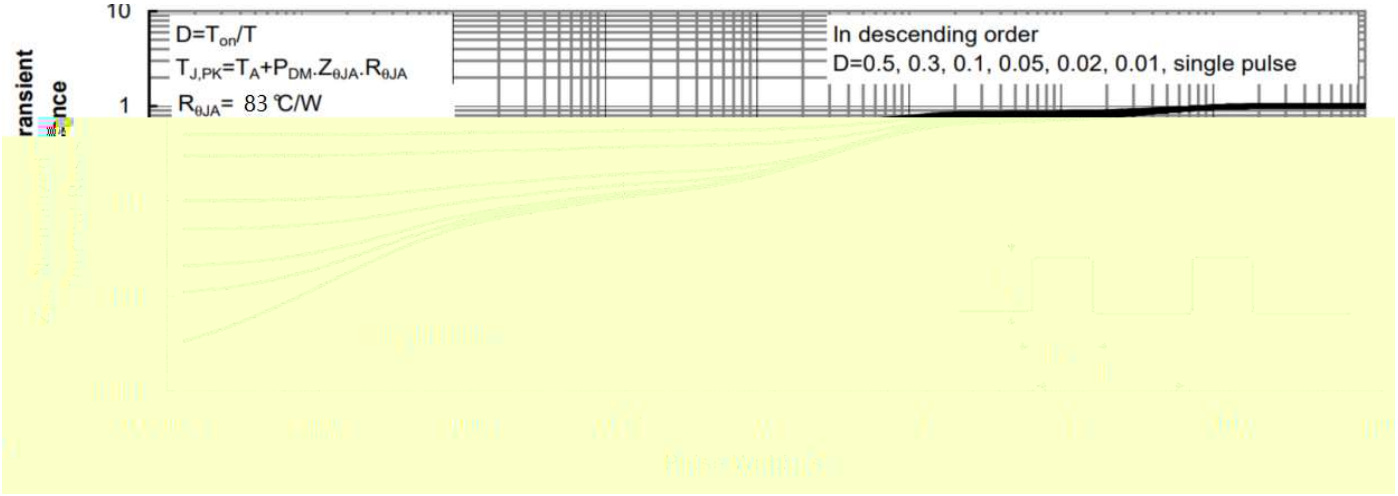

V_{GS}=4.5V
I_D=20A
Normalized On-Resistance
T-Temperature (℃)

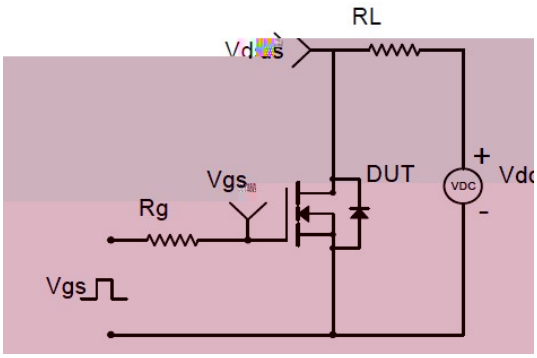

Ciss
Crss
Coss
C-Capacitance (pF)
V_{DS}-Drain Voltage (V)

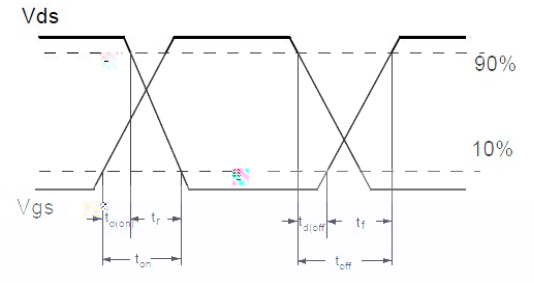

V_{DS}= 10V
I_D= 6.8A
V_{GS}-Gate Voltage (V)
Q_G-Gate Chare (nC)

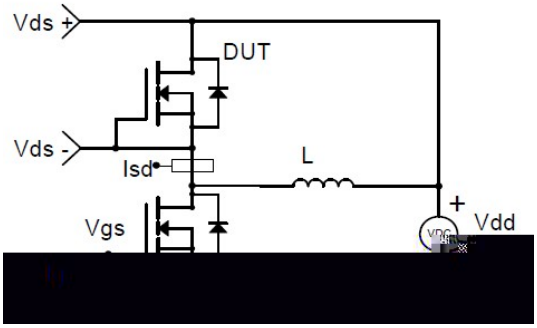

1000
100
10
1
0.1
0.01
0.001
0.0001
0.01
0.1
1
10
100
RDS(ON) limited
DC
10s
100us
1ms
10ms
100ms
1s
TJ(Max)=150℃
TA=25℃
Single Pulse
ID-Drain Current(A)
VDS Drain-Source Voltage(V)

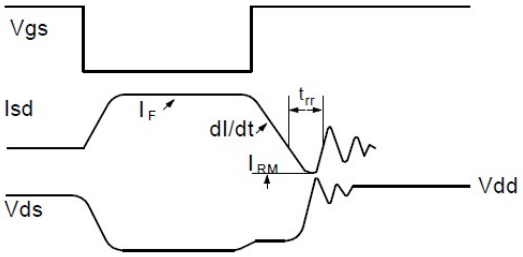

10
8
6
4
2
0
0
25
50
75
100
125
150
175
RθJA=83℃/W
ID-Drain Curent (A)
TA-Ambient Temperature (℃)

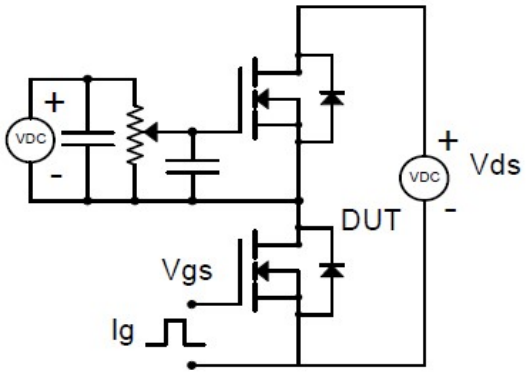

10
1
D=Ton/T
TJ,PK=TA+PDM.ZθJA.RθJA
RθJA= 83℃/W
In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

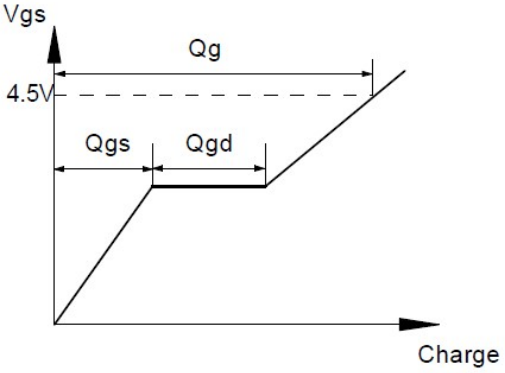

RL
Vds
Vgs
DUT
VDC
Rg
Vgs

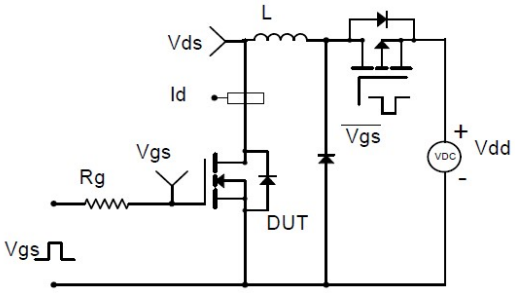

Vds
90%
10%
Vgs

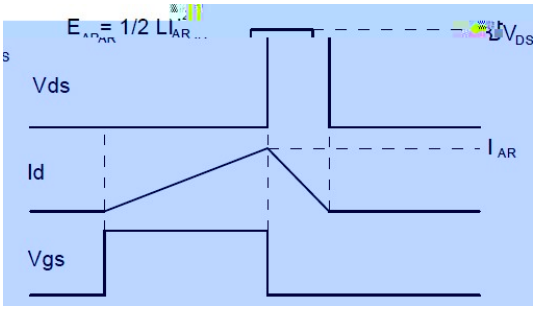

Vds +
DUT
Vds -
Isd
L
Vgs
VDC
Vdd


Vgs
Isd
IF
dI/dt
trr
IRM
Vds
Vdd

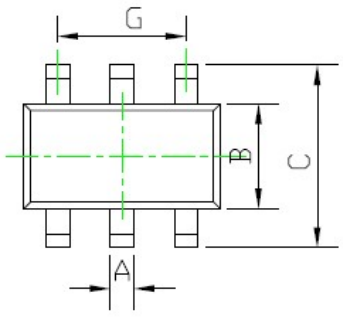

VDC
Vds
DUT
Vgs
Ig


Vgs
Qg
4.5V
Qgs
Qgd
Charge

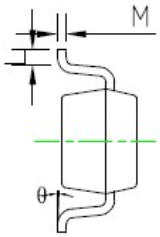

L
Vds
Id
Vgs
Rg
DUT
Vgs
VDC
Vdd
Vgs


Vds
Id
IAR
Vgs

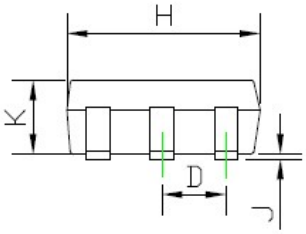
■



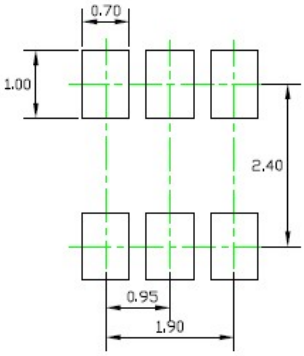
TOP VIEW



SIDE VIEW



SIDE VIEW



Suggested Solder Pad Layout

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.012	0.020	0.300	0.500
B	0.059	0.067	1.500	1.700
C	0.104	0.116	2.650	2.950
D	0.037BSC		0.950BSC	
G	0.075BSC		1.900BSC	
H	0.111	0.119	2.820	3.020
J	0.000	0.004	0.000	0.100
K	0.041	0.045	1.050	1.150
L	0.012	0.024	0.300	0.600
M	0.004	0.008	0.100	0.200
θ	0°	8°	0°	8°

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