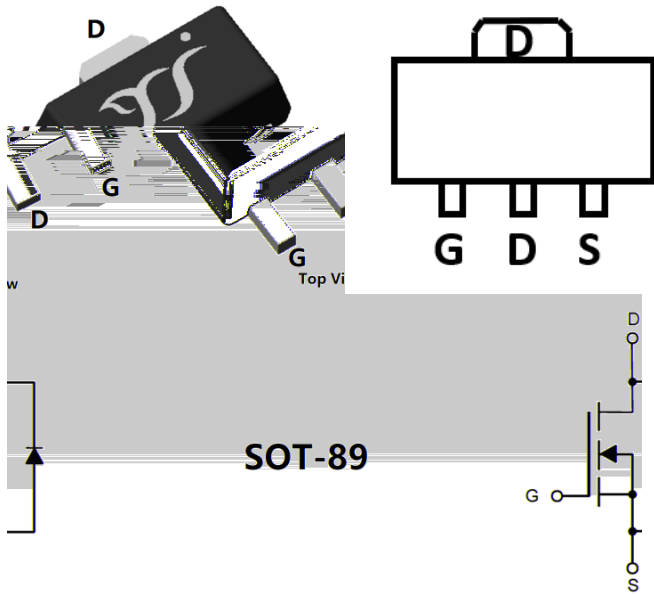


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

V_{DS}	100V
I_D	3.0A
$R_{DS(ON)}$ (at $V_{GS}= 10V$)	<110mohm
$R_{DS(ON)}$ (at $V_{GS}= 4.5V$)	<120mohm

General Description

Trench Power MV MOSFET technology
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

DC-DC Converters
Power management functions

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	3	A
	$T_A=70^\circ\text{C}$		2.4	
Pulsed Drain Current ^A		I_{DM}	12	A
Total Power Dissipation	$T_A=25^\circ\text{C}$	P_D	1.5	W
	$T_C=25^\circ\text{C}$		4.0	
Thermal Resistance Junction-to-Ambient ^B		R_{JA}	83	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Case		R_{JC}	31	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJH03N10A	F1	1003	1000	10000	40000	7" reel
	F2	1003	1000	8000	32000	7" reel



YJH03N10A

Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.1	1.8	3	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =3A		95	110	m
		V _{GS} = 4.5V, I _D =2.4A		100	120	
Diode Forward Voltage	V _{SD}	I _S =3A, V _{GS} =0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	I _S				3	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHZ		1070		pF
Output Capacitance	C _{oss}			33		
Reverse Transfer Capacitance	C _{rss}			30		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =10A		26		nC
Gate-Source Charge	Q _{gs}			5.4		
Gate-Drain Charge	Q _{gd}			5.8		
Reverse Recovery Charge	Q _{rr}	I _F =10A, di/dt=100A/us		30.1		
Reverse Recovery Time	t _{rr}			40		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, R _L =6.4 R _{GEN} =3		7		ns
Turn-on Rise Time	t _r			24		
Turn-off Delay Time	t _{D(off)}			24		
Turn-off fall Time	t _f			31		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R_{JA} is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. R_{JL} is guaranteed by design, while R_{JA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

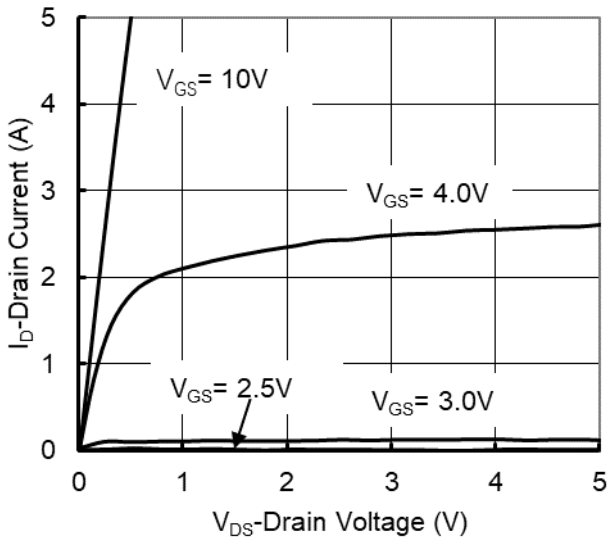


Figure 1. Output Characteristics

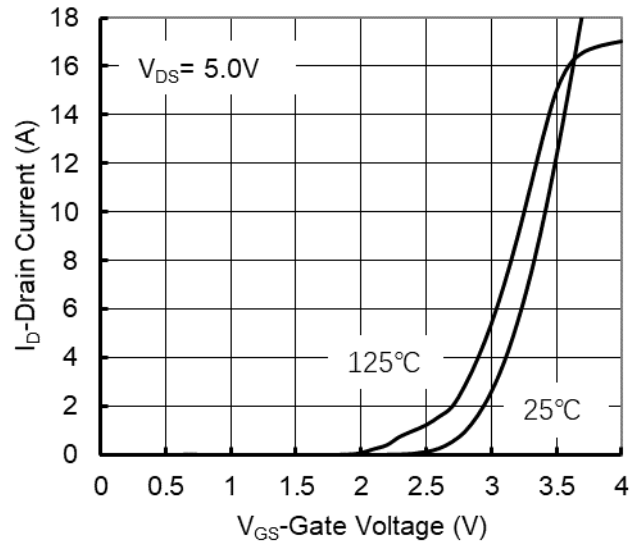


Figure 2. Transfer Characteristics

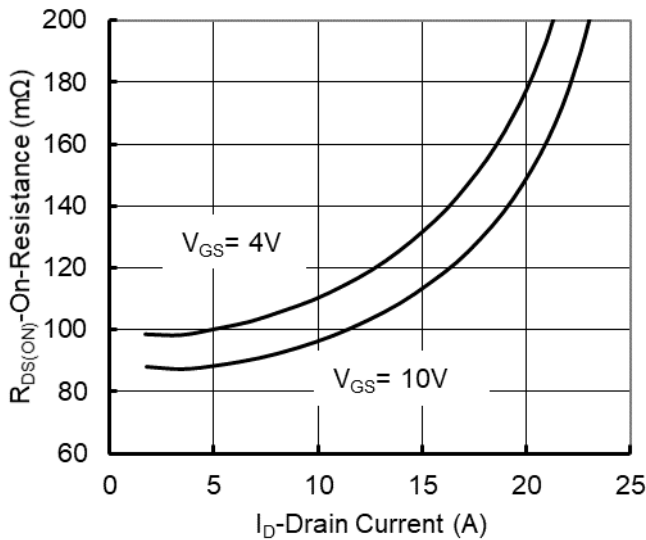


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

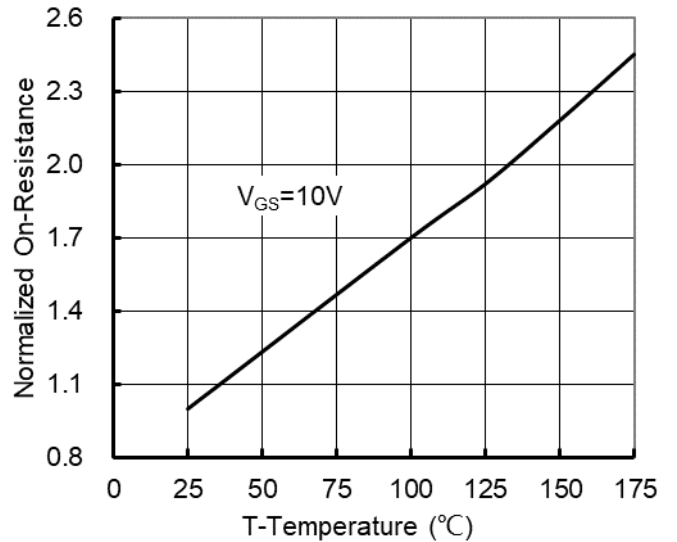


Figure 4. On-Resistance vs. Junction Temperature

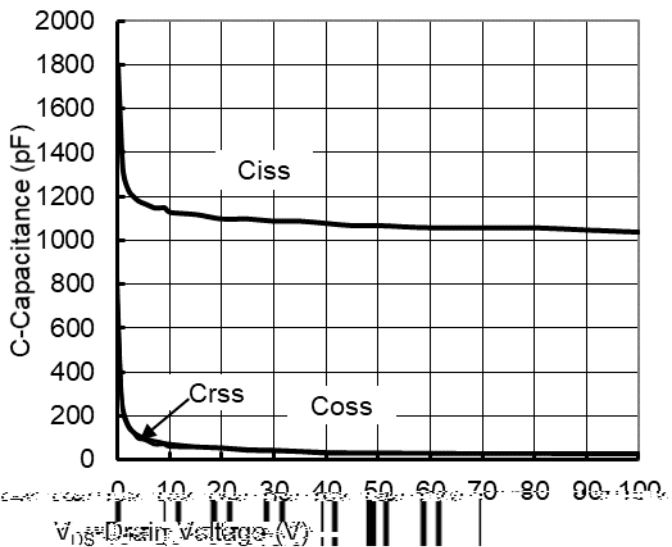


Figure 5. Capacitance Characteristics

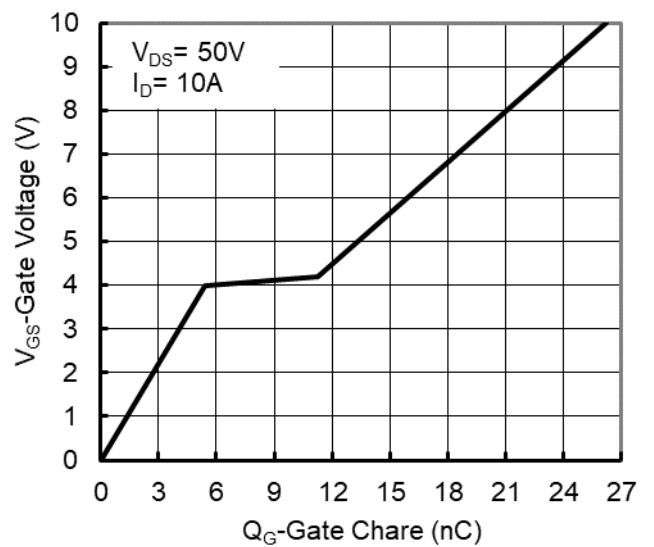


Figure 6. Gate Charge



YJH03N10A

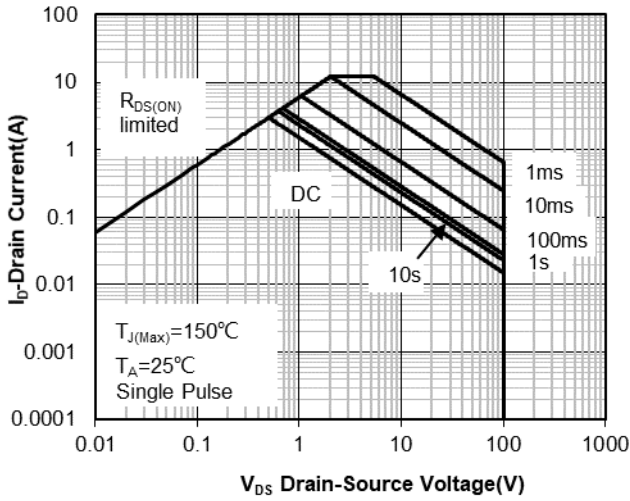


Figure 7. Safe Operation Area

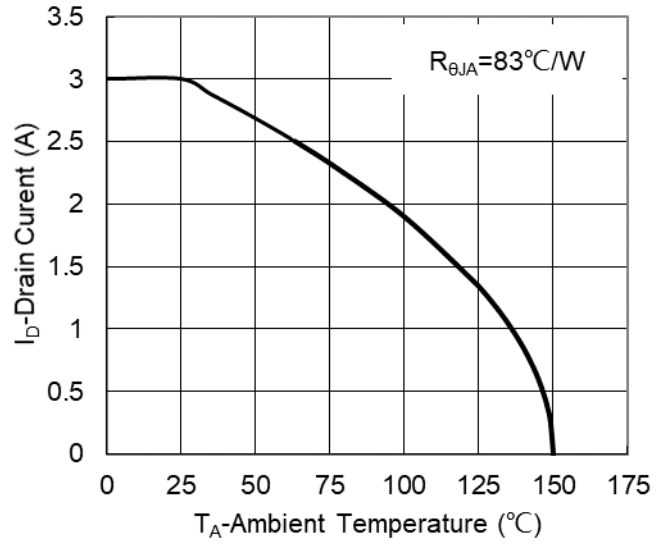


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

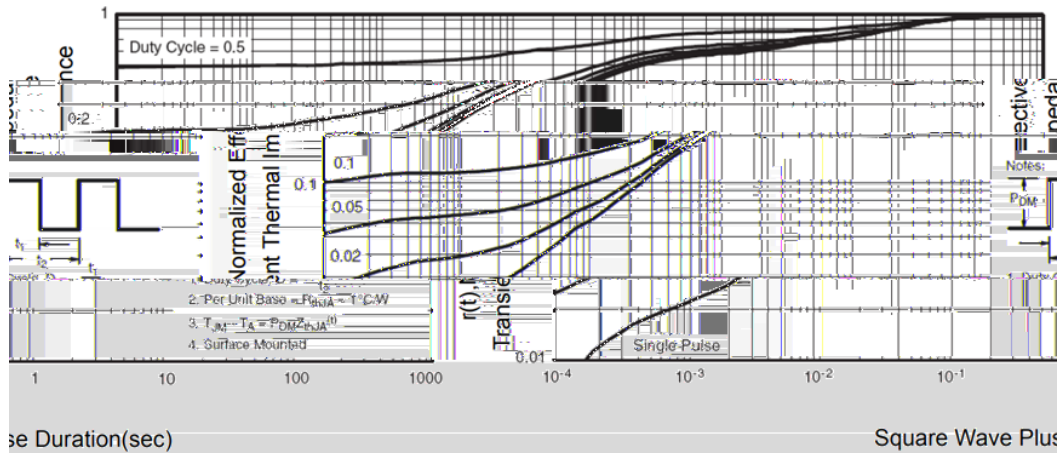
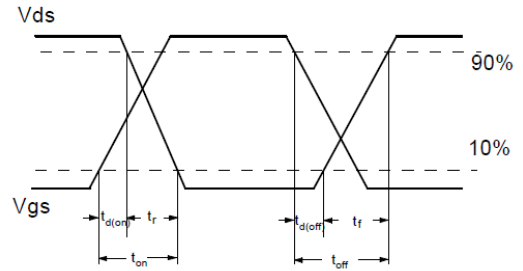
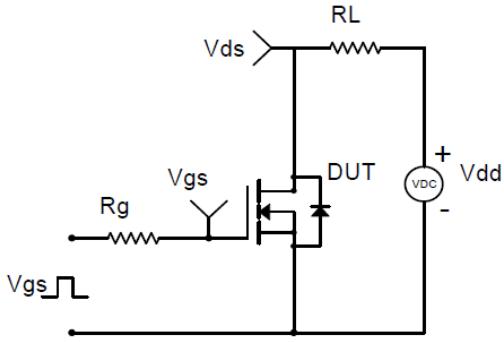
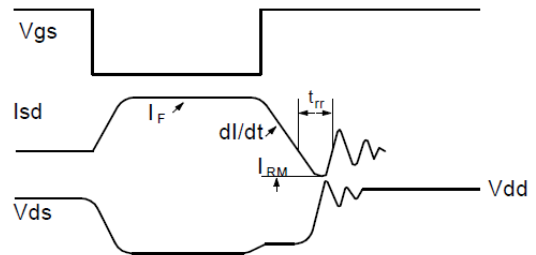
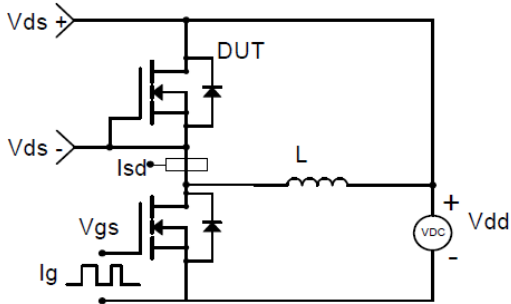


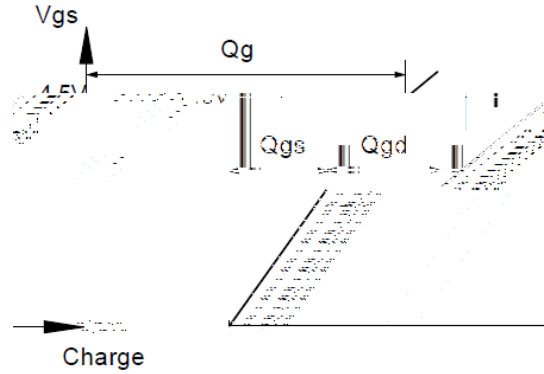
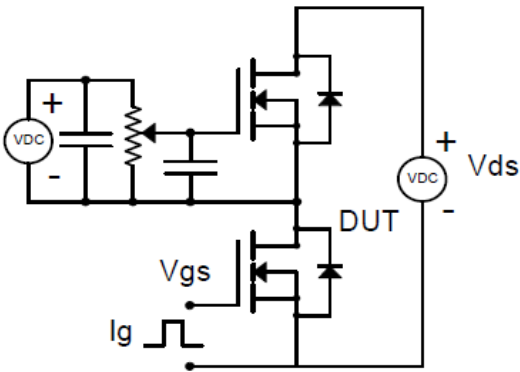
Figure 9. Normalized Maximum Transient Thermal Impedance



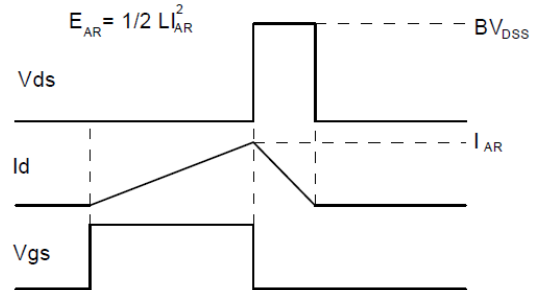
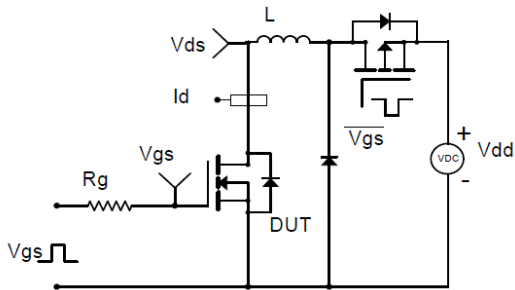
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform



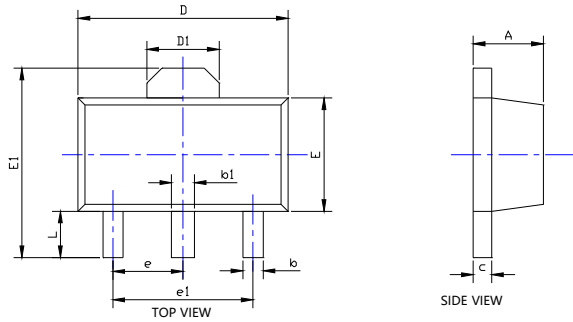
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



YJH03N10A

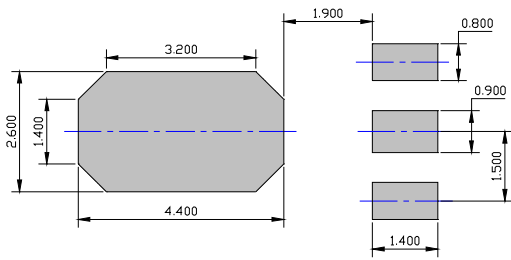
SOT-89 Package information

TYPE A(PACKING CODE:F1):



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.055	0.059	0.063	1.400	1.500	1.600
b	0.014	---	0.020	0.350	---	0.520
b1	0.016	---	0.023	0.400	---	0.580
c	0.014	---	0.017	0.350	---	0.440
D	0.173	0.177	0.181	4.400	4.500	4.600
D1	0.061REF			1.550REF		
E	0.093	0.096	0.100	2.350	2.450	2.550
E1	0.155	---	0.167	3.940	---	4.250
e	0.059TYP			1.500TYP		
e1	0.118TYP			3.000TYP		
L	0.035	0.039	0.043	0.900	1.000	1.100

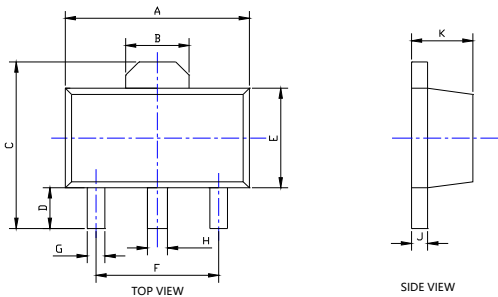
- NOTE:
 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



SUGGESTED SOLDER PAD LAYOUT

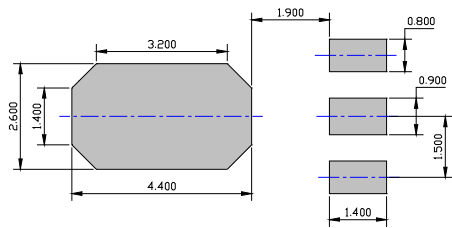
UNIT: mm

TYPE B(PACKING CODE:F2):



DIM	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.169	0.185	4.300	4.700
B	0.061TYP		1.550TYP	
C	0.154	0.171	3.910	4.350
D	0.031	0.047	0.800	1.200
E	0.089	0.104	2.250	2.650
F	0.118TYP		3.000TYP	
G	0.013	0.020	0.330	0.520
H	0.016	0.023	0.400	0.580
J	0.014	0.017	0.350	0.440
K	0.055	0.063	1.400	1.600
L	0.059TYP		1.500TYP	

- NOTE:
 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



SUGGESTED SOLDER PAD LAYOUT

UNIT: mm



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