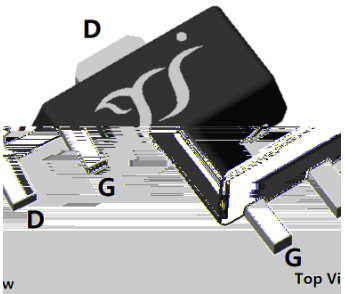
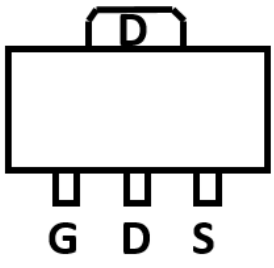
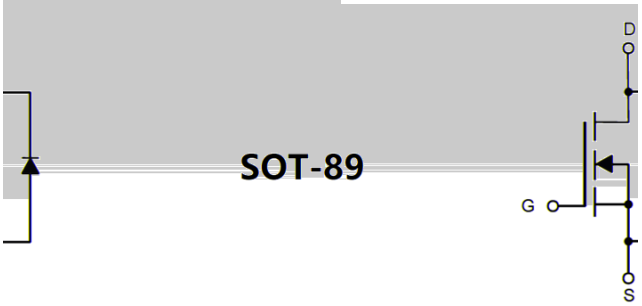
N-Channel Enhancement Mode Field Effect Transistor







Product Summary

- V_{DS} 60V
- I_D 3.5A
- $R_{DS(ON)}$(at V_{GS}= 10V) 100mohm
- $R_{DS(ON)}$(at V_{GS}= 4.5V) 120mohm
- $R_{DS(ON)}$(at V_{GS}= 2.5V) 200mohm

General Description

- Trench Power LV MOSFET technology
- High Density Cell Design for Low $R_{DS(ON)}$
- High Speed switching
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	±16	V
Drain Current	T_A=25	I_D	3.5	A
	T_A=70		2.8	
Pulsed Drain Current [A]		I_{DM}	14	A
Total Power Dissipation @ T_A=25 Steady State		P_D	1.7	W
Thermal Resistance Junction-to-Ambient [B]		$R_{\theta JA}$	74	/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +150	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJH03N06B	F1	6003	1000	10000	40000	7“ reel
	F2	6003	1000	8000	32000	7“ reel

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}= 60V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D= 250μA	0.65	0.95	1.55	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D= 3A		86	100	mΩ
		V_{GS}= 4.5V, I_D= 2A		90	120	
		V_{GS}= 2.5V, I_D= 1A		100	200	
Diode Forward Voltage	V_{SD}	I_S= 3.0A,V_{GS}=0V		0.8	1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=30V,V_{GS}=0V,f=1MHZ		451		pF
Output Capacitance	C_{oss}			38		
Reverse Transfer Capacitance	C_{rss}			31		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}= 10V,V_{DS}= 30V,I_D= 3.0A		13.8		nC
Gate-Source Charge	Q_{gs}			2.2		
Gate-Drain Charge	Q_{gd}			1.9		
Reverse Recovery Chrage	Q_{rr}	I_F= 3A, di/dt=100A/us		7.6		
Reverse Recovery Time	t_{rr}			30		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}= 10V, V_{DS}= 30V, I_D= 1.5A R_{GEN}= 3Ω		3		
Turn-on Rise Time	t_r			18		
Turn-off Delay Time	$t_{D(off)}$			17		
Turn-off fall Time	t_f			22		

A. Pulse Test: Pulse Width ≤ 300us,Duty cycle ≤ 2%.

B. $R_{\theta JA}$ is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JL}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

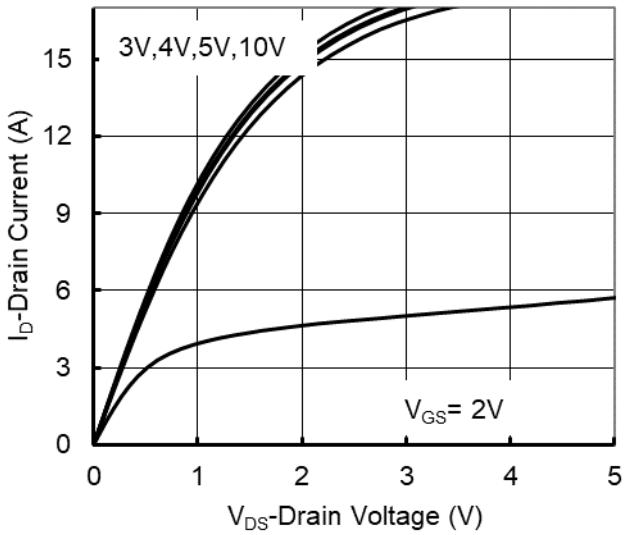


Figure1. Output Characteristics

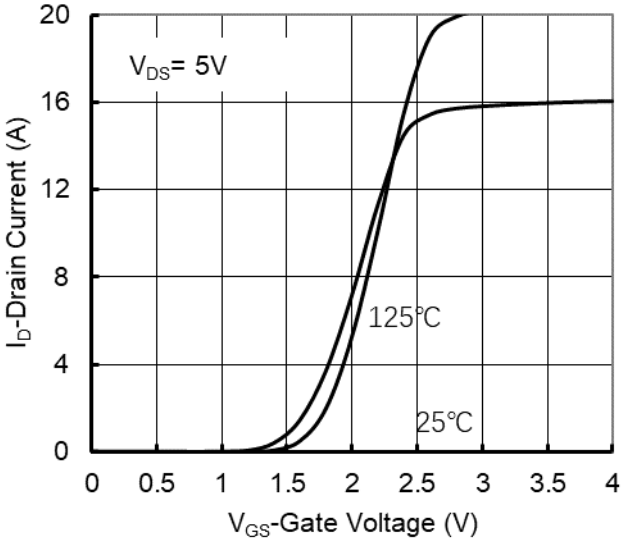


Figure2. Transfer Characteristics

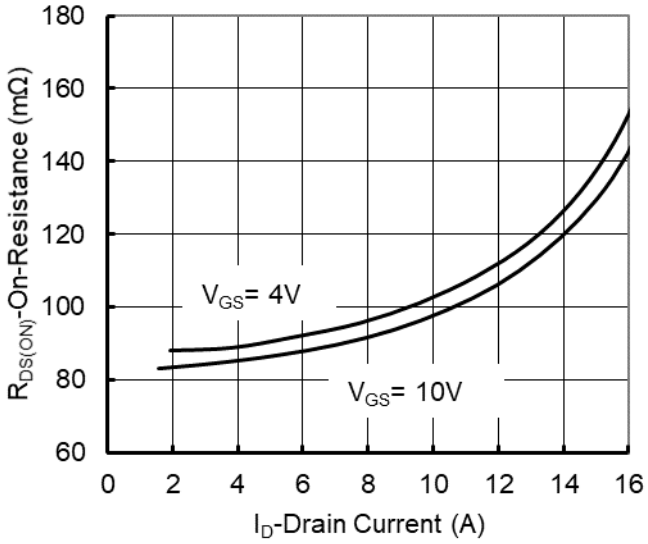


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

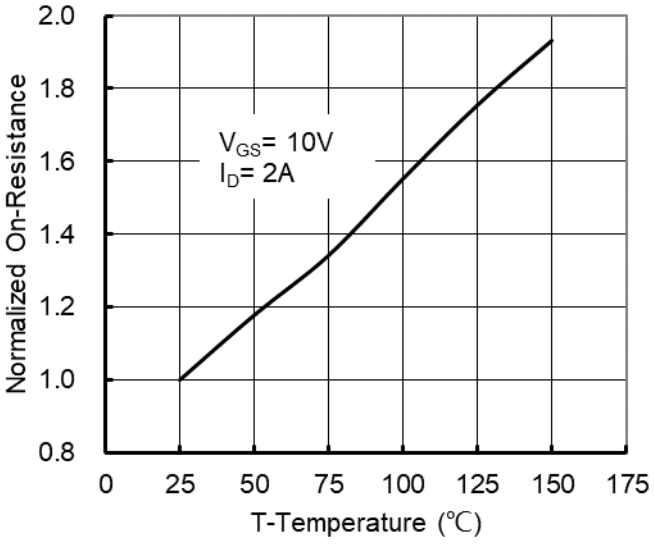


Figure 4: On-Resistance vs. Junction Temperature

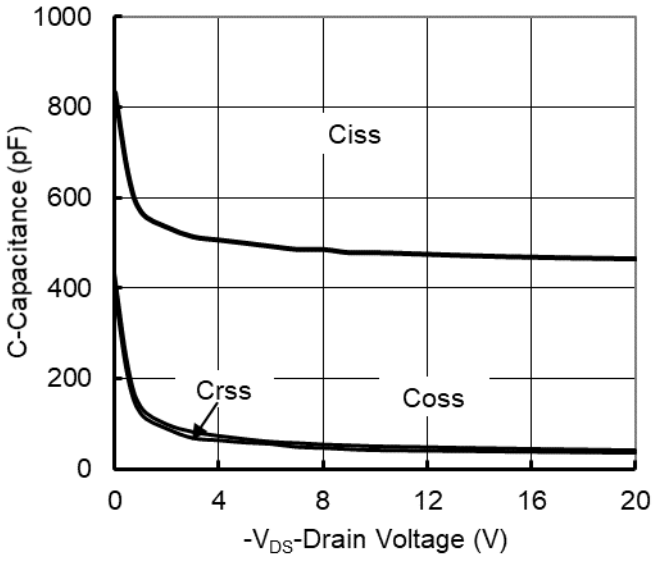


Figure5. Capacitance Characteristics

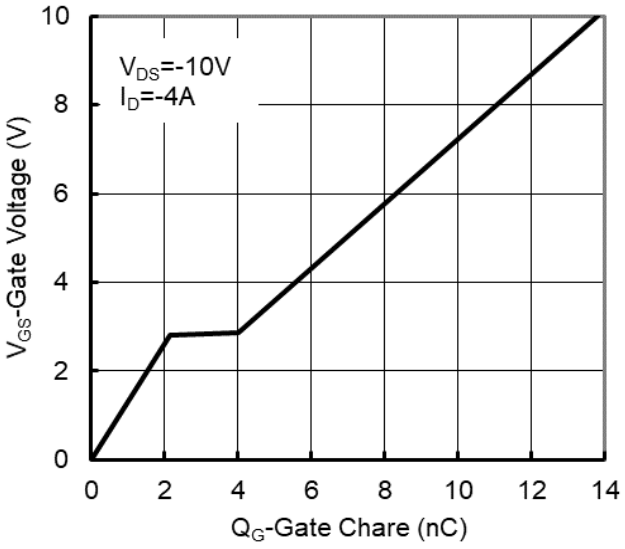


Figure6. Gate Charge

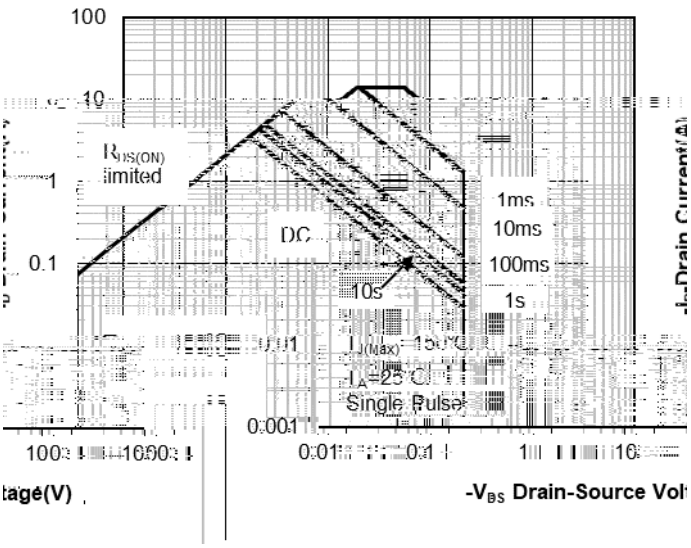


Figure7. Safe Operation Area

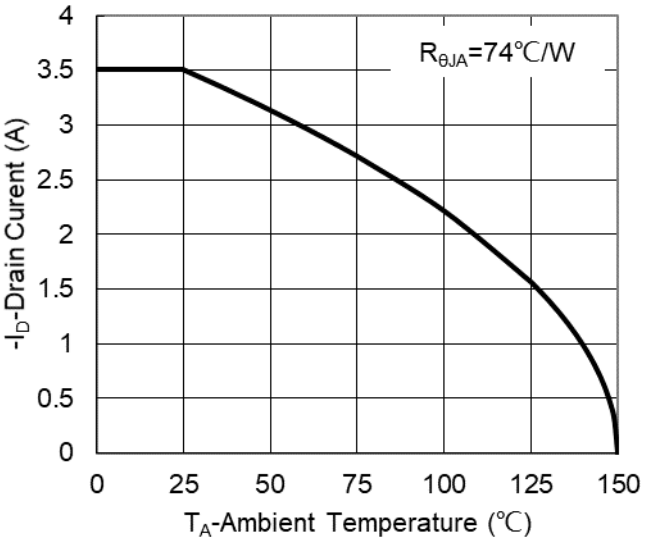


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

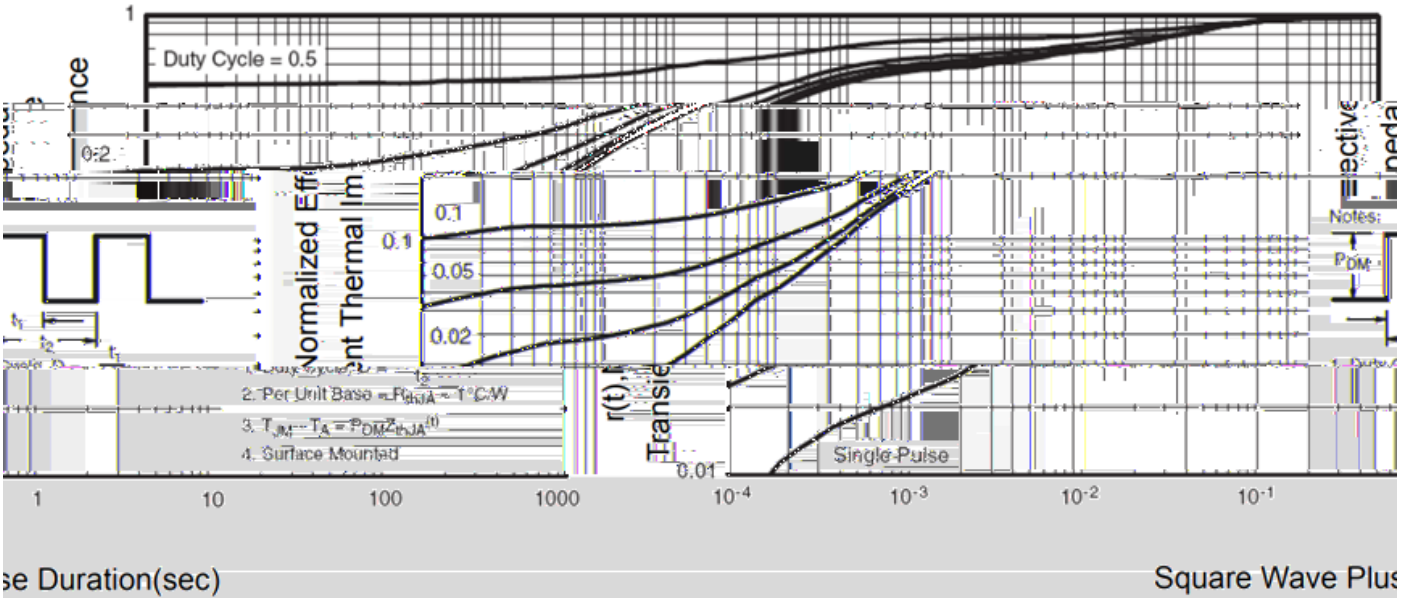
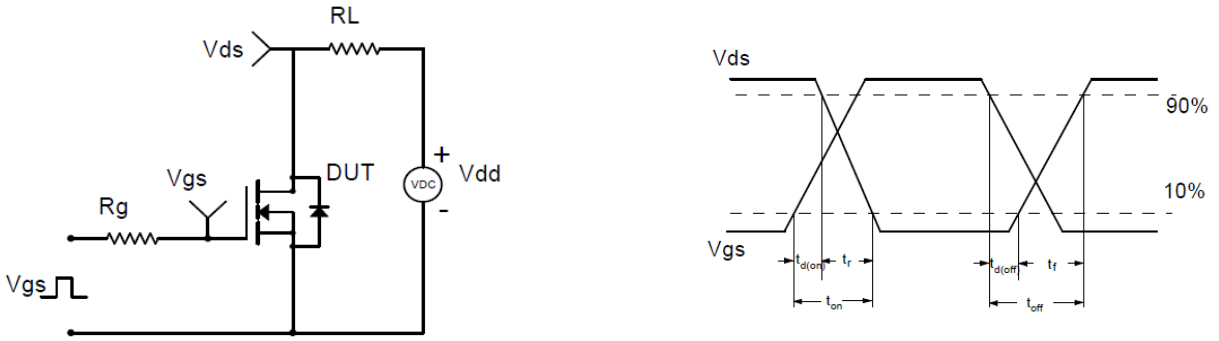
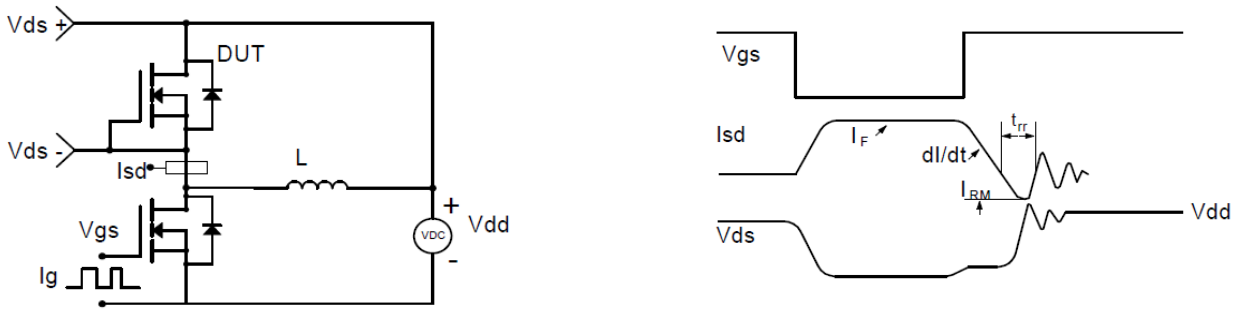


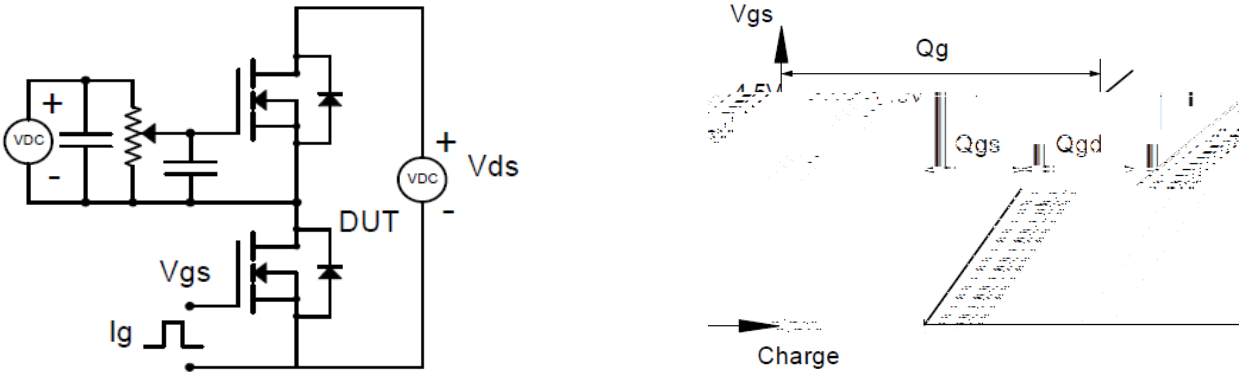
Figure9. Normalized Maximum Transient Thermal Impedance



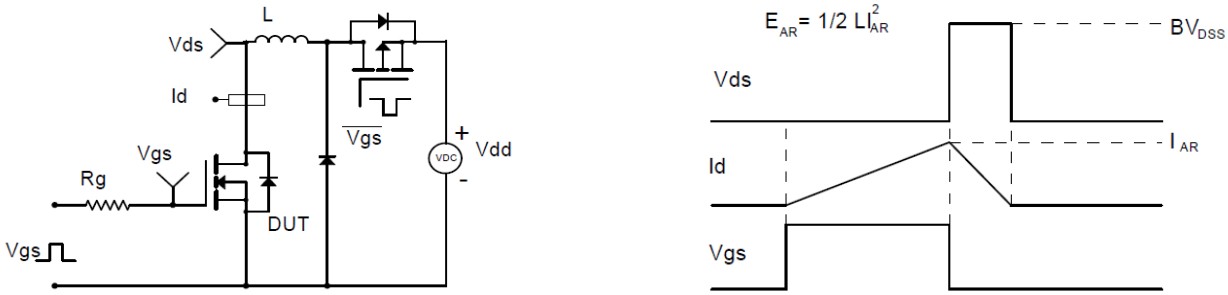
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



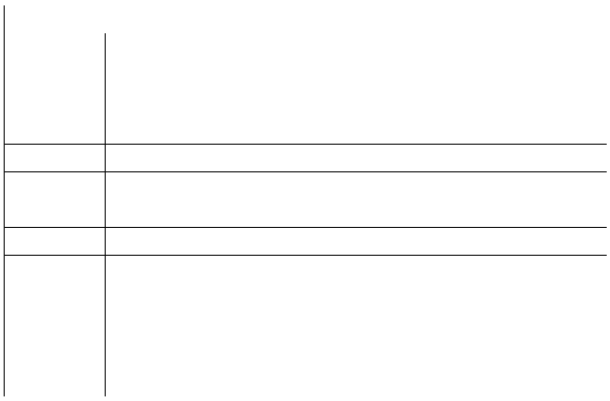
Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

■ SOT-89 Package Information

TYPE A(PACKING CODE:F1):



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