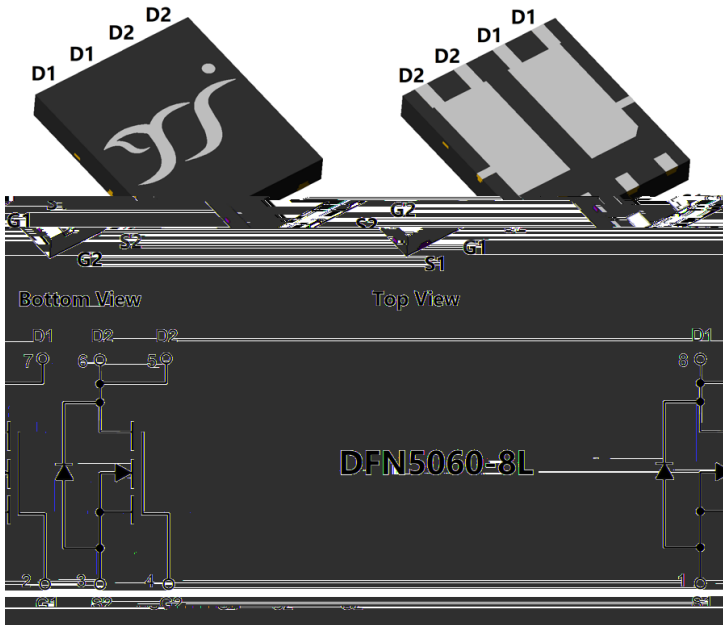


## N-Channel and N-Channel Complementary MOSFET



### Product Summary

- $V_{DS}$  30V
- $I_D$  45A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ ) 9m $\Omega$
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ ) 12m $\Omega$
- 100% EAS Tested

### General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- Power switching application
- Uninterruptible power supply
- DC-DC converter

### ■ Absolute Maximum Ratings ( $T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	30	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ C$	$I_D$	12	A
	$T_A=100^\circ C$		7.5	
	$T_C=25^\circ C$		45	
	$T_C=100^\circ C$		28	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	180	A
Avalanche energy <sup>B</sup>		EAS	128	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ C$	$P_D$	2.5	W
	$T_A=100^\circ C$		1	
	$T_C=25^\circ C$		100	
	$T_C=100^\circ C$		40	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 +150	$^\circ C$

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State	$R_{\theta JA}$	40	50	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1	1.25	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJGD45N03A	F1	YJGD45N03A	5000	10000	100000	13" reel



# YJGD45N03A

## ■ Electrical Characteristics ( $T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=30V, V_{GS}=0V$	-	-	1	$\mu A$
		$V_{DS}=30V, V_{GS}=0V, T_J=150^\circ C$	-	-	100	
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.6	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=22.5A$	-	6.5	9	m $\Omega$
		$V_{GS}=10V, I_D=20A$	-	6.5	9	
		$V_{GS}=4.5V, I_D=20A$	-	9	1	



# YJGD45N03A

## Typical Electrical and Thermal Characteristics Diagrams

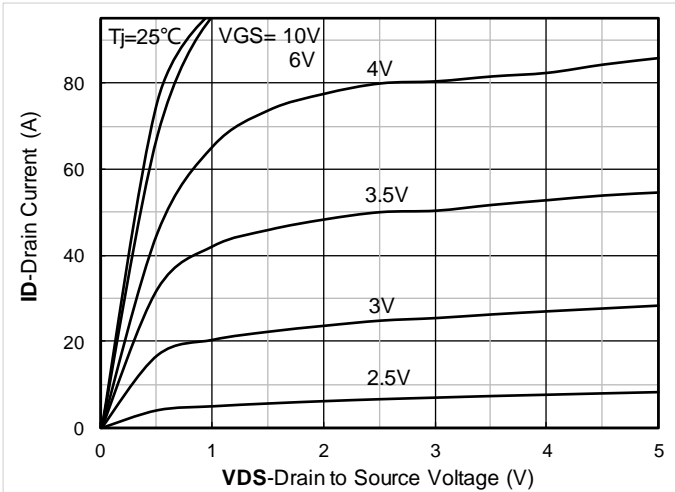


Figure 1. Output Characteristics

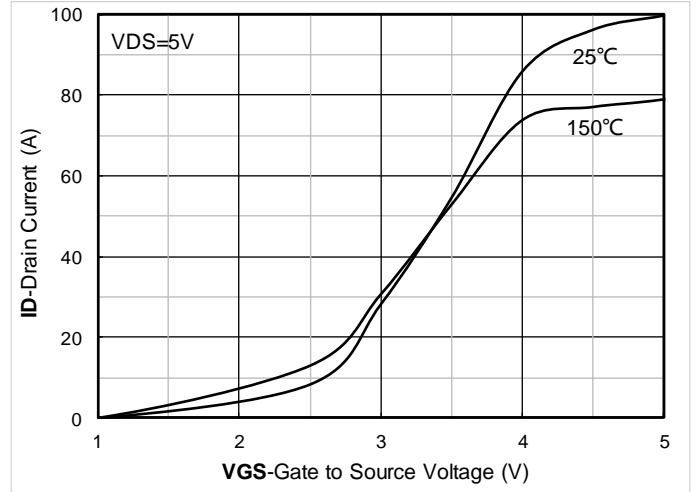


Figure 2. Transfer Characteristics

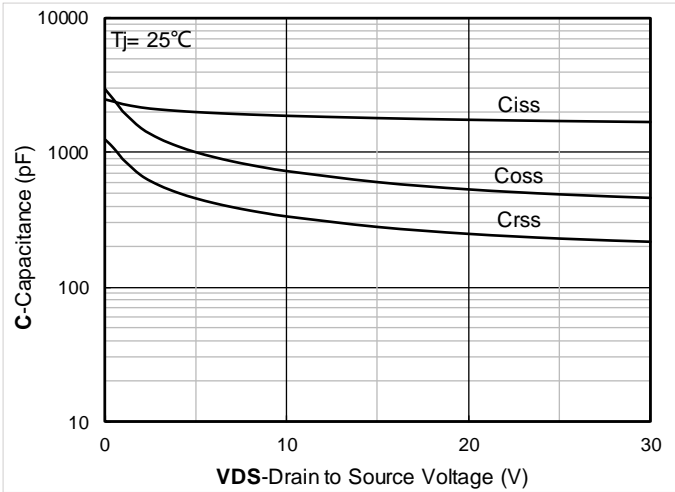


Figure 3. Capacitance Characteristics

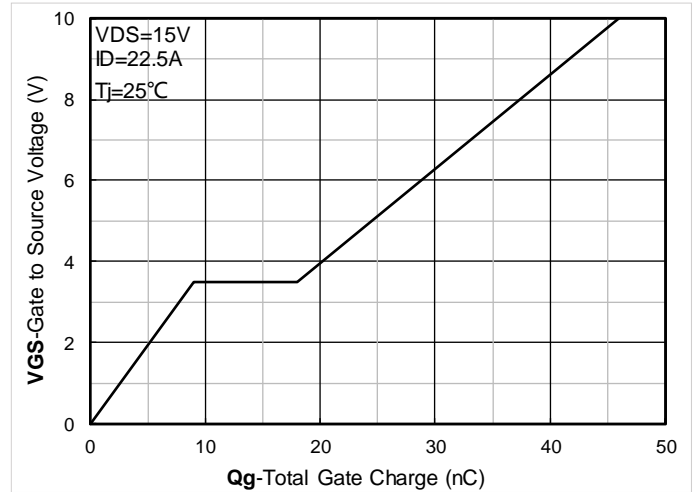


Figure 4. Gate Charge

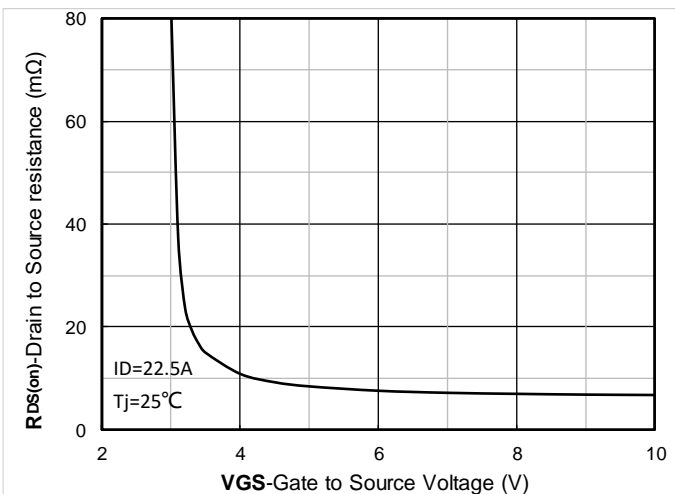


Figure 5. On-Resistance vs Gate to Source Voltage

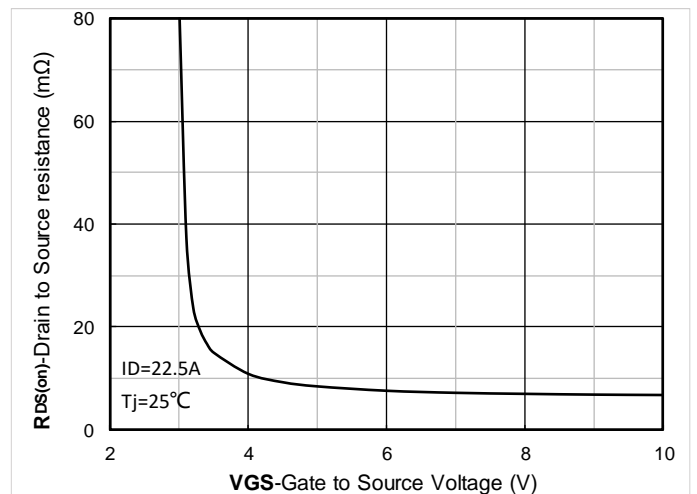


Figure 6. Normalized On-Resistance



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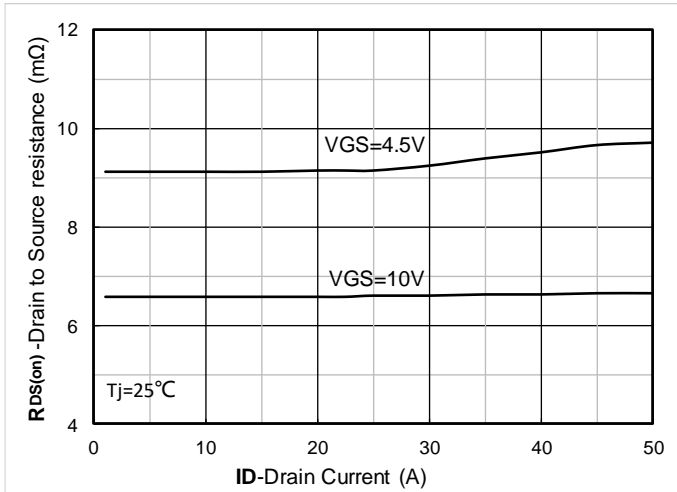


Figure 7.  $R_{DS(on)}$  VS Drain Current

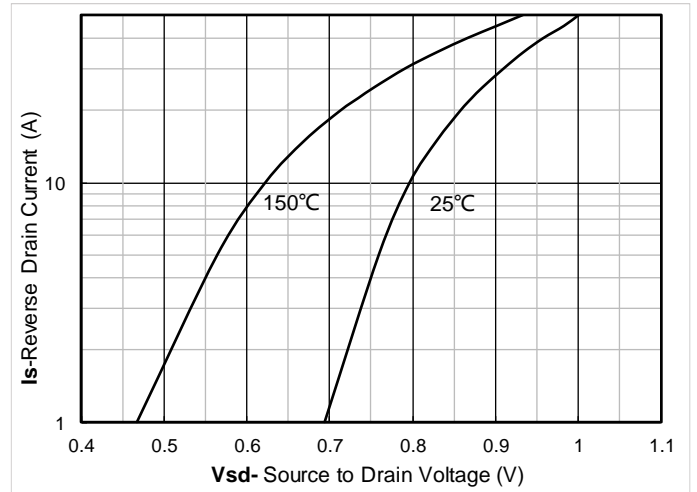


Figure 8.

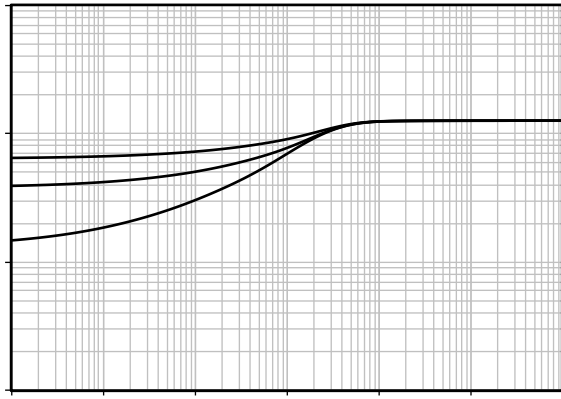


Figure 13. Maximum Transient Thermal Impedance

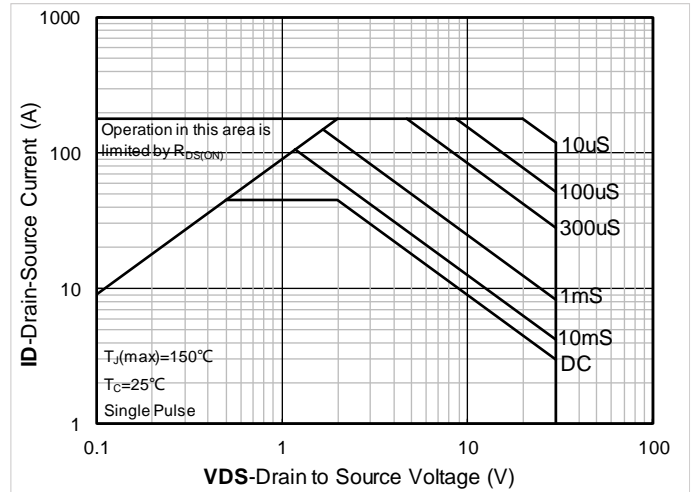


Figure 14. Safe Operation Area

## ■ Test Circuits & Waveforms

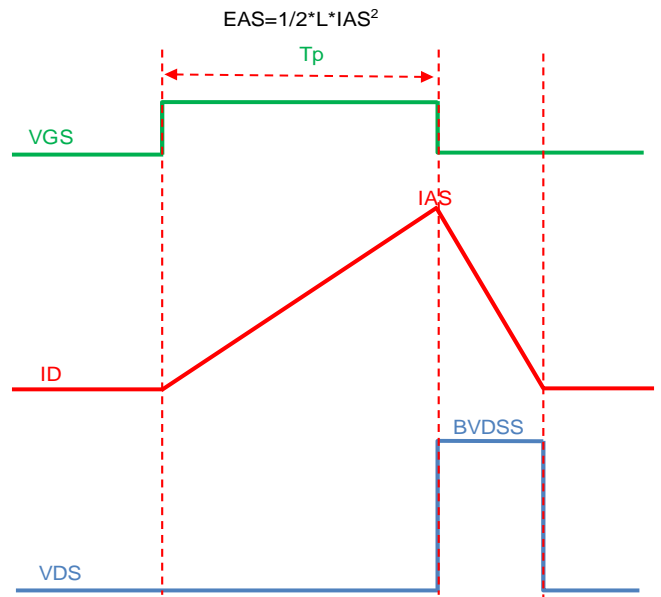
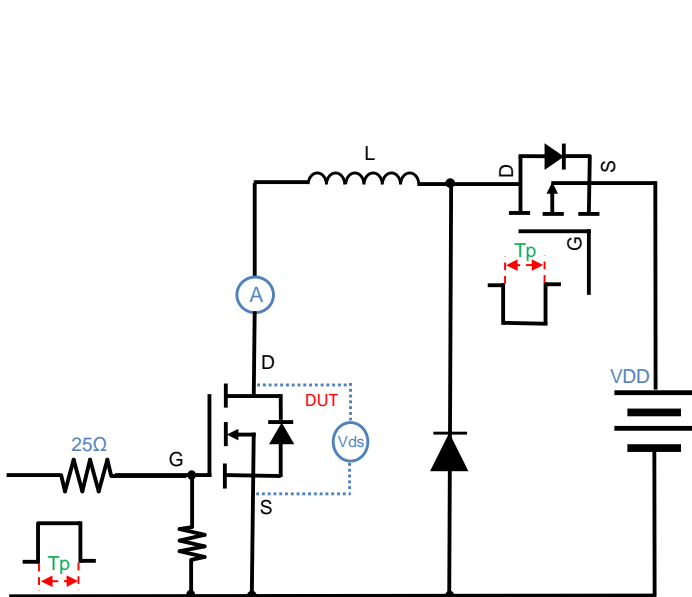


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

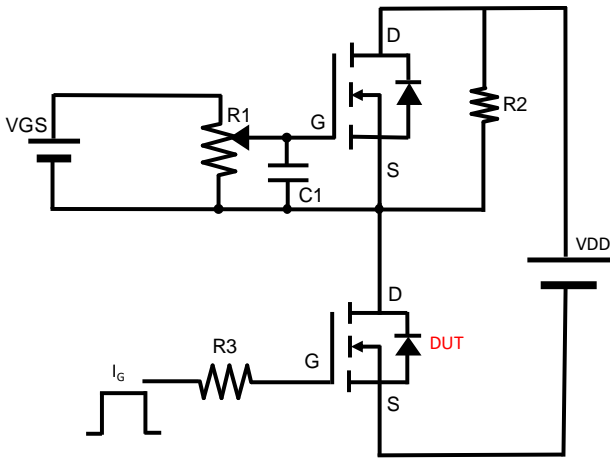


Figure B. Gate Charge Test Circuit & Waveform



Figure C. Resistive Switching Test Circuit & Waveform



Figure D. Diode Recovery Test Circuit & Waveform



## ■ DFN5060-8L Package information

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	4.90	5.00	5.10
E	5.90	6.00	6.10
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	1.60	1.70	1.80
E1	3.65	3.75	3.85
L1	0.45	0.55	0.65
L2	0.80 BSC		
b	0.30	0.40	0.50
e	1.27 BSC		



**Note:**

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.

Suggested Solder Pad Layout  
Top View



## YJGD45N03A

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