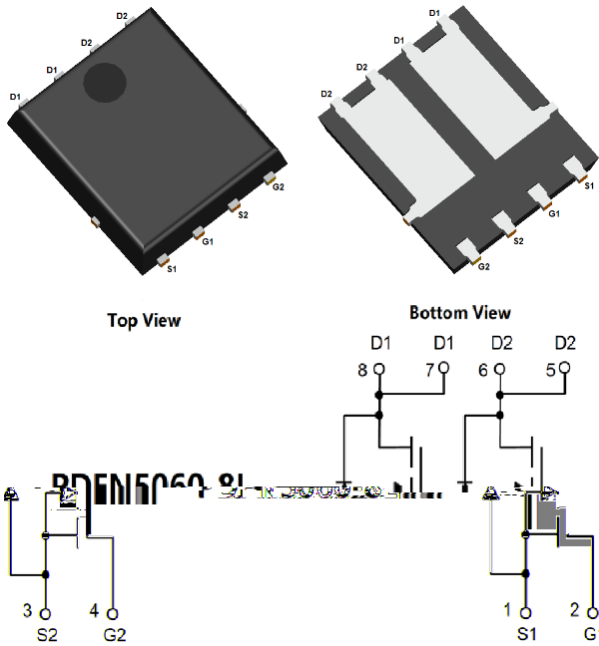


## N-Channel Enhancement Mode Field Effect Transistor



### Product Summary

NMOS(Die1/Die2)

- $V_{DS}$  60V
- $I_D$  20A
- $R_{DS(ON)}$ ( at  $V_{GS}=10V$ ) <30m $\Omega$
- $R_{DS(ON)}$ ( at  $V_{GS}=4.5V$ ) <40m $\Omega$
- 100% EAS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Part no. with suffix "Q" means AEC-Q101 qualified

### Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- 12V, 24V Automotive systems

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit(N-Die1/Die2)	Unit
Drain-source Voltage		$V_{DS}$	60	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ\text{C}$	$I_D$	6	A
	$T_A=100^\circ\text{C}$		4	
	$T_C=25^\circ\text{C}$		20	
	$T_C=100^\circ\text{C}$		12.5	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	50	A
Avalanche energy <sup>B</sup>		EAS	40	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ\text{C}$	$P_D$	2.5	W
	$T_A=100^\circ\text{C}$		1	
	$T_C=25^\circ\text{C}$		69	
	$T_C=100^\circ\text{C}$		27	
Thermal Resistance Junction-to-Ambient <sup>D</sup>		$R_{\theta JA}$	50	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	1.8	$^\circ\text{C/W}$
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJGD20N06AQ	F1	YJGD20N06A	5000	10000	100000	13" reel



# YJGD20N06AQ

## ■ NMOS(Die1/Die2) Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.5	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		23	30	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A		28	40	mΩ
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V			1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz		2		Ω
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		1250		pF
Output Capacitance	C <sub>oss</sub>			80		
Reverse Transfer Capacitance	C <sub>rss</sub>			60		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =20A	-	23	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	3	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	6	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=100A/us	-	17.5	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	23.5	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =30V, I <sub>D</sub> =20A R <sub>GEN</sub> =3Ω	-	5	-	ns
Turn-on Rise Time	t <sub>r</sub>			44		
Turn-off Delay Time	t <sub>D(off)</sub>			19		
Turn-off fall Time	t <sub>f</sub>			2		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T<sub>J</sub>=25°C, V<sub>DD</sub>=40V, V<sub>G</sub>=10V, L=1mH, I<sub>AS</sub>=9A.

C. P<sub>d</sub> is based on max. junction temperature, using junction-case thermal resistance.

D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation PDSM is based on RθJA ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



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## ■NMOS(Die1/Die2) Typical Electrical and Thermal Characteristics Diagrams

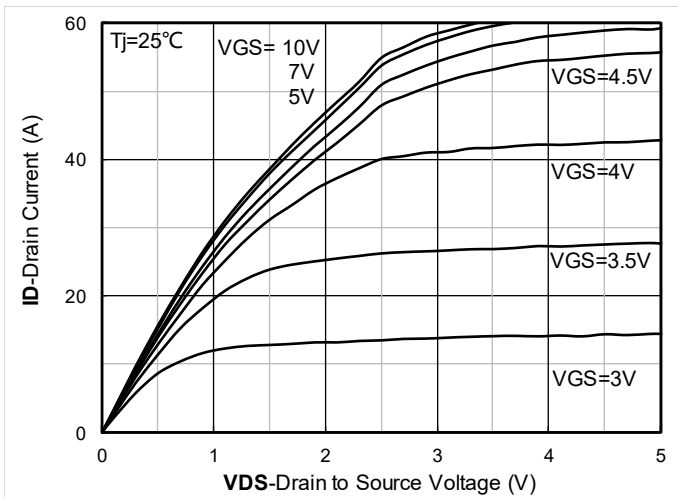


Figure 1. Output Characteristics

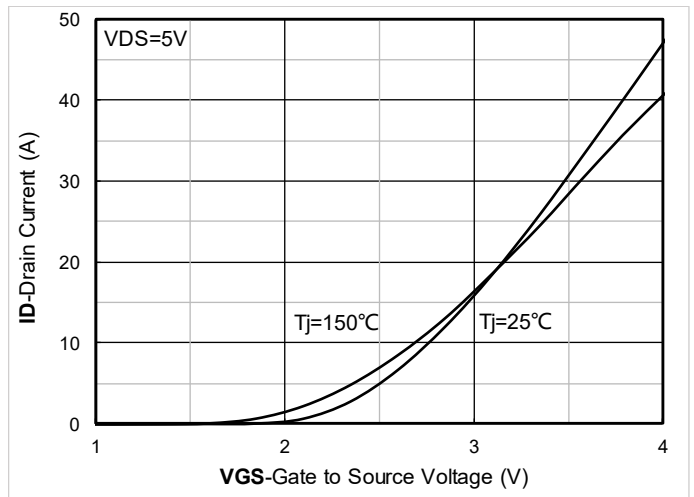


Figure 2. Transfer Characteristics

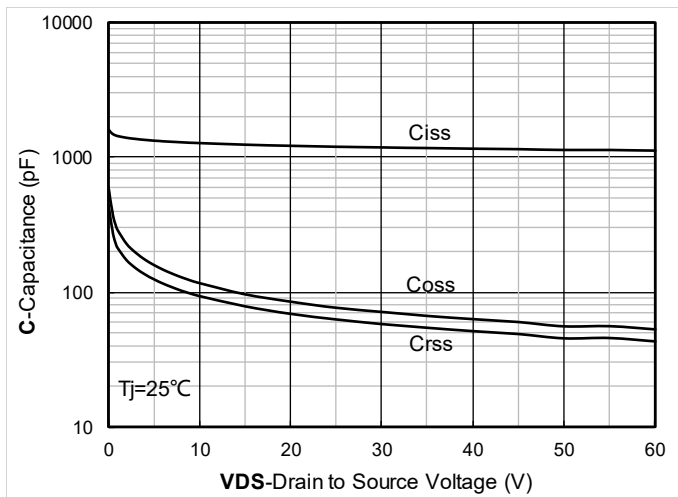


Figure 3. Capacitance Characteristics

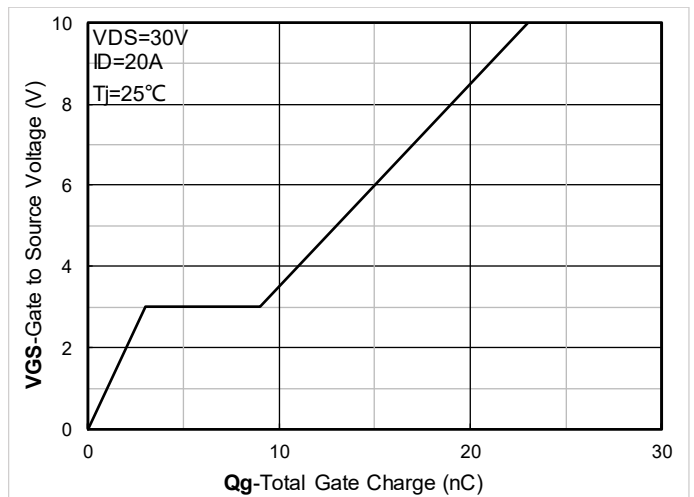


Figure 4. Gate Charge

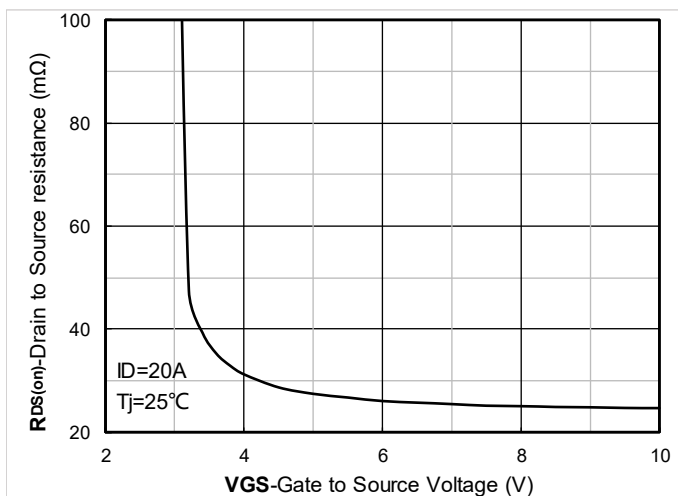


Figure 5. On-Resistance vs Gate to Source Voltage

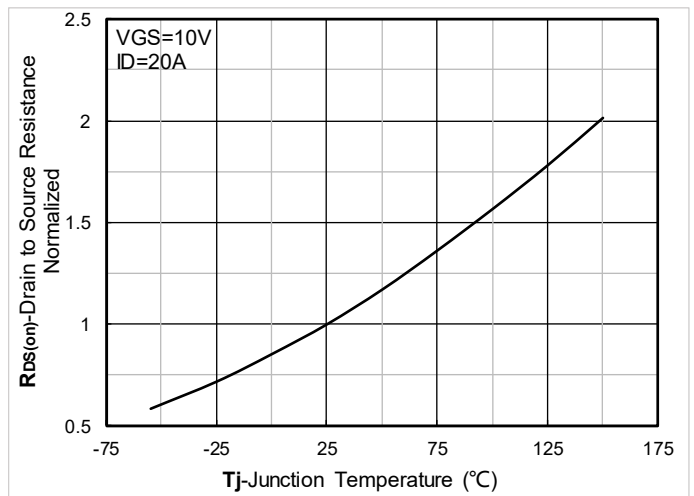


Figure 6. Normalized On-Resistance



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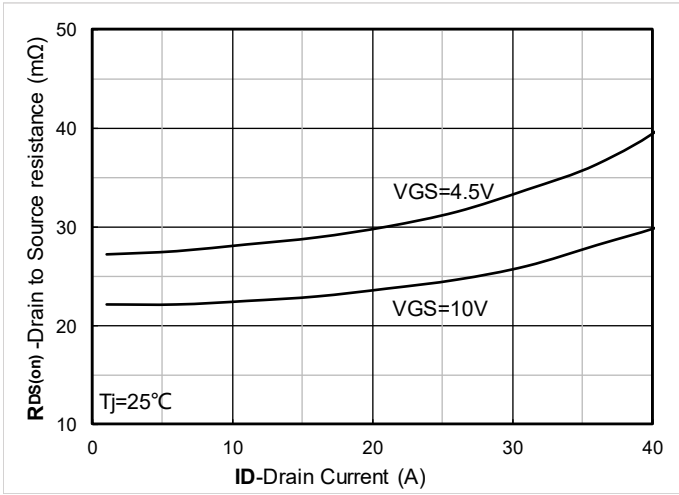


Figure 7.  $R_{DS(on)}$  VS Drain Current

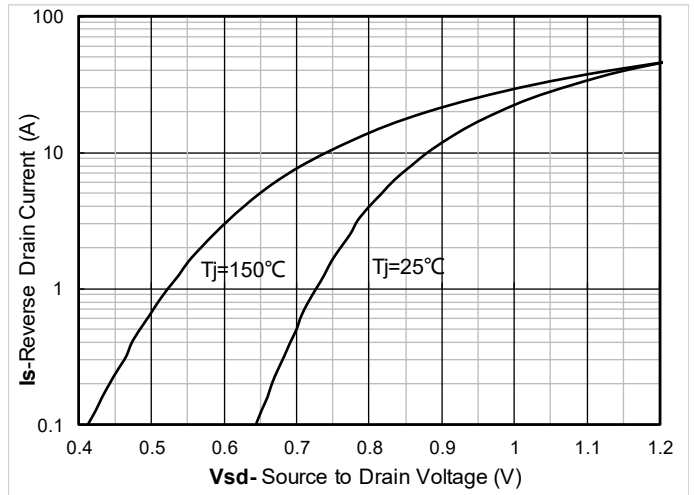


Figure 8. Forward characteristics of reverse diode

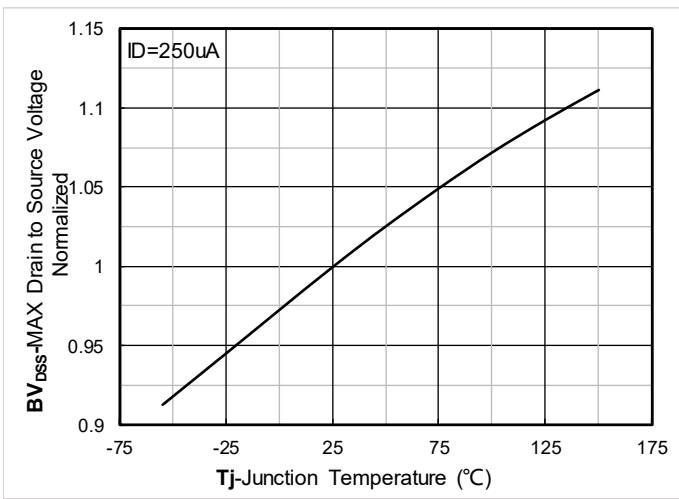


Figure 9. Normalized breakdown voltage

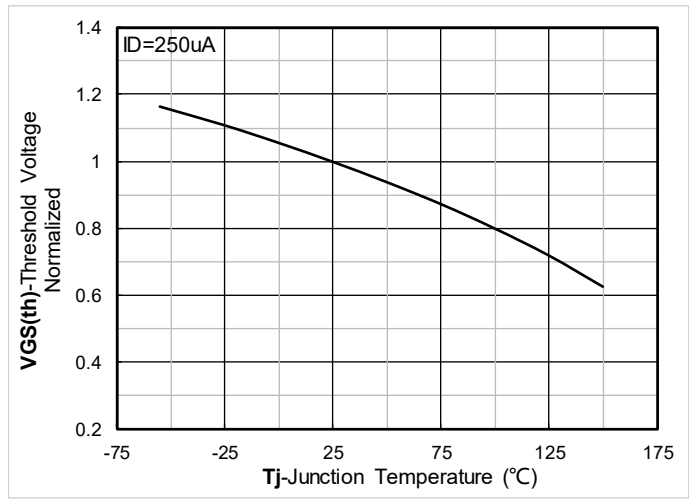


Figure 10. Normalized Threshold voltage

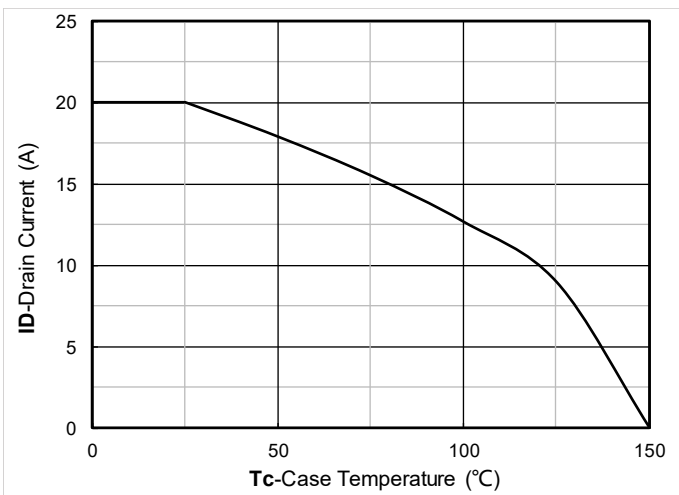


Figure 11. Current dissipation

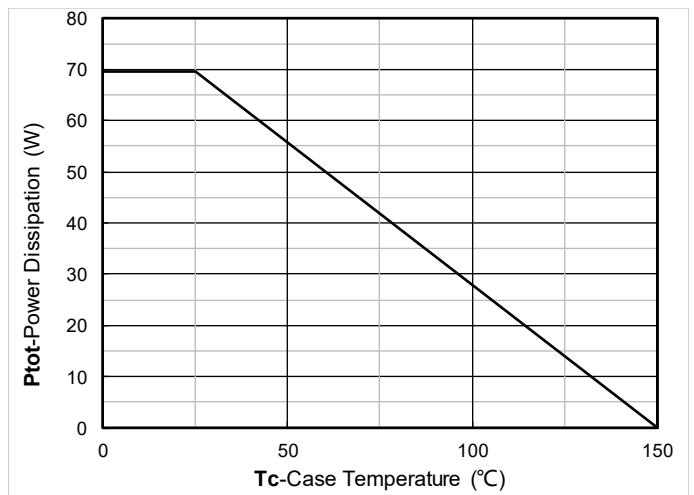


Figure 12. Power dissipation

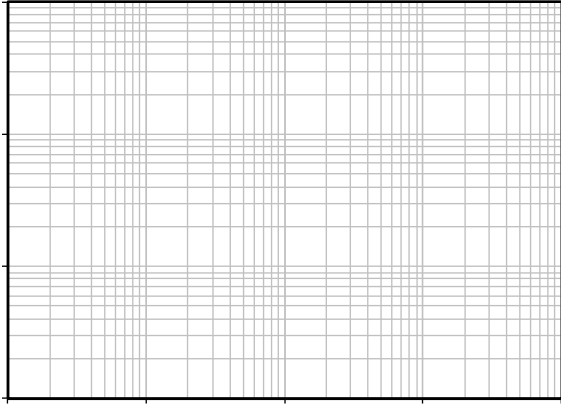


Figure 13. Maximum Transient Thermal Impedance

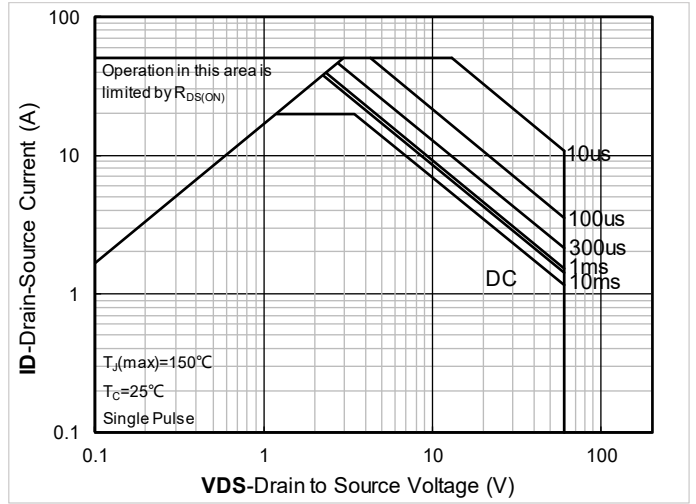
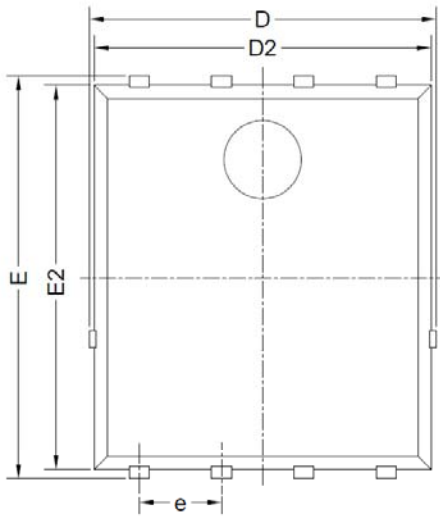


Figure 14. Safe Operation Area

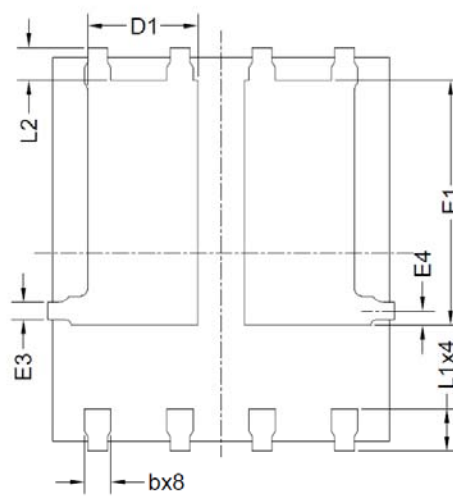


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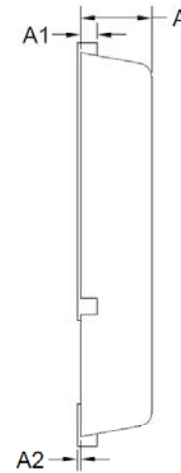
## ■ PDFN5060-8L-E-1.1MM Package information



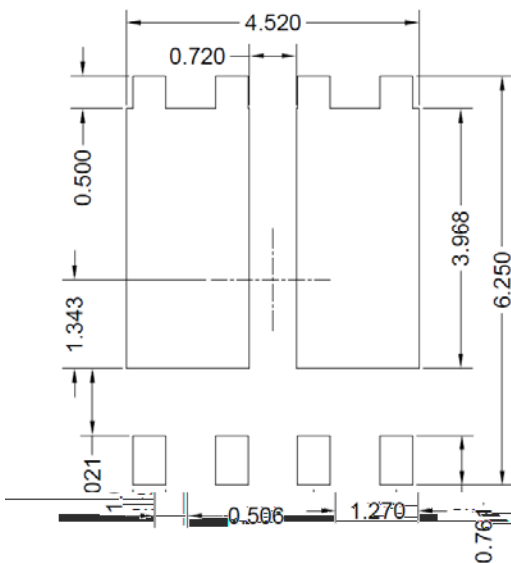
Top View  
正面视图



Bottom View  
背面视图



Side View  
侧面视图



Suggested Solder Pad Layout  
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	1.50	1.70	1.90
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	12/BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$  mm.
3. The pad layout is for reference purposes only.



## YJGD20N06AQ

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