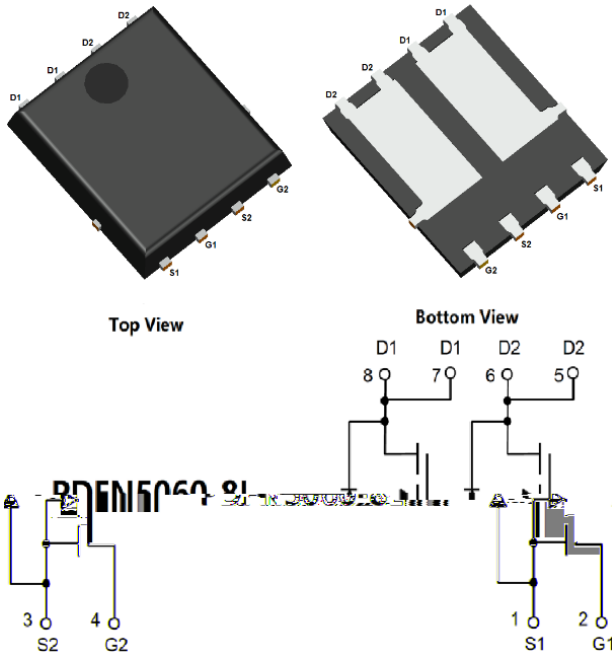


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

NMOS(Die1/Die2)

- V_{DS} 100V
- I_D 20A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <22 mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <27 mohm

General Description

- Split gate trench MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- DC-DC Converters
- Power management functions
- Industrial and Motor Drive application
- 12V, 24V and 48V Automotive systems

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	N-Die1/Die2	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	20	A
	$T_C=100^\circ\text{C}$		13	
	$T_A=25^\circ\text{C}$		7	
	$T_A=100^\circ\text{C}$		4.5	
Pulsed Drain Current ^A		I_{DM}	80	A
Avalanche energy ^B		E_{AS}	81	mJ
Total Power Dissipation ^C	$T_C=25^\circ\text{C}$	P_D	50	W
	$T_C=100^\circ\text{C}$		20	
	$T_A=25^\circ\text{C}$		2.5	
	$T_A=100^\circ\text{C}$		1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	$R_{\theta JA}$	40	50	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	2	2.5	



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■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJGD20G10BQ	F1	YJGD20G10B	5000	10000	100000	13" reel

■ NMOS(Die1/Die2) Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =20A		16	22	mΩ
		V _{GS} = 4.5V, I _D =10A		18	27	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V		0.9	1.3	V
Gate Resistance	R _g	f=1MHz		1.5		Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHZ		1240		pF
Output Capacitance	C _{oss}			740		
Reverse Transfer Capacitance	C _{rss}			25		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =20A		17		nC
Gate-Source Charge	Q _{gs}			6		
Gate-Drain Charge	Q _{gd}			3		
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=100A/us		42		ns
Reverse Recovery Time	t _{rr}			40		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =20A R _{GEN} =3.0Ω		40		ns
Turn-on Rise Time	t _r			12		
Turn-off Delay Time	t _{D(off)}			55		
Turn-off fall Time	t _f			16		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V_{DD}=50V, R_G=25Ω, L=2mH, I_{AS}=9A.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The Power dissipation PDSM is based on RθJA ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.



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■ NMOS(Die1/Die2) Typical Performance Characteristics

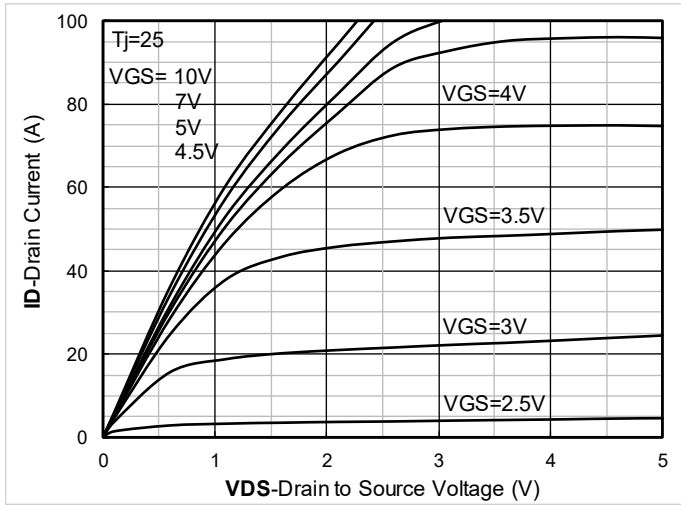


Figure1. Output Characteristics

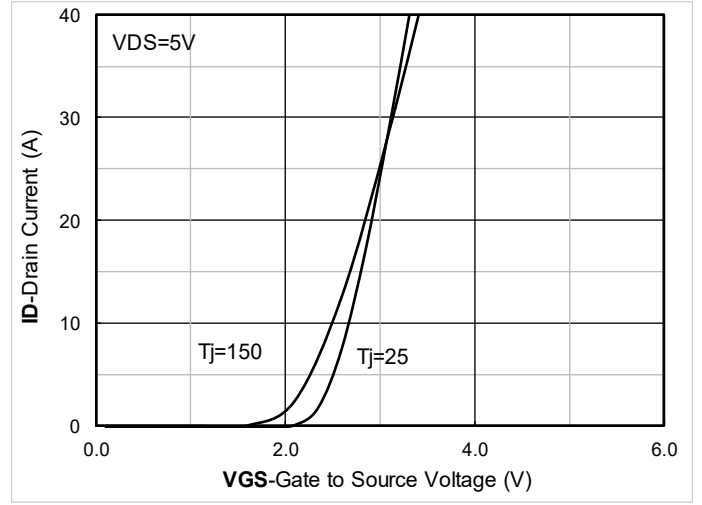


Figure2. Transfer Characteristics

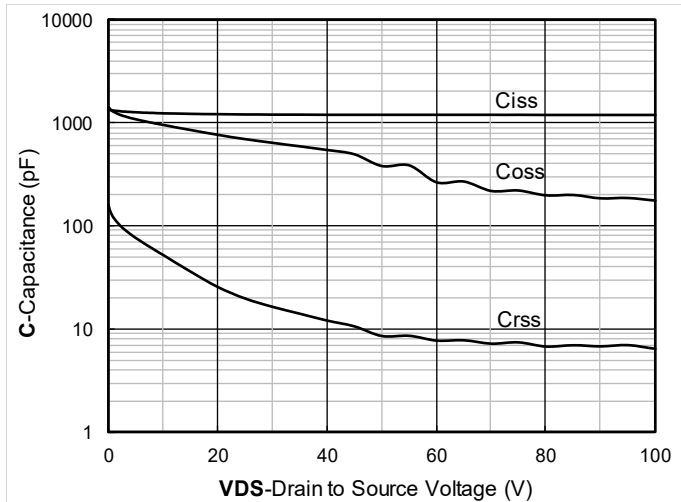


Figure3. Capacitance Characteristics

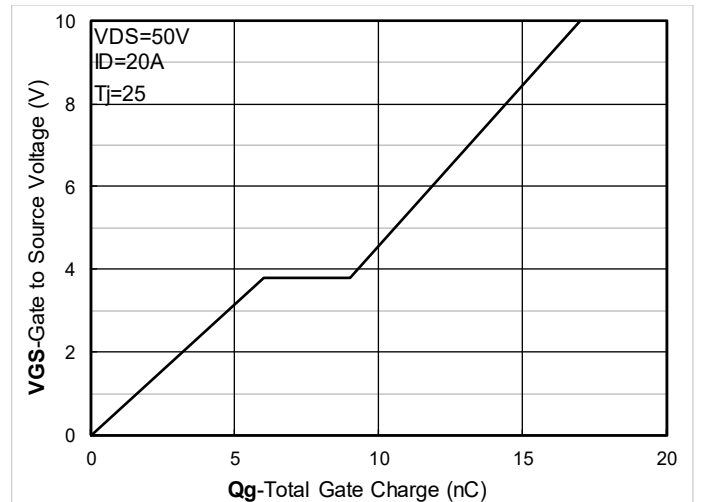


Figure4. Gate Charge

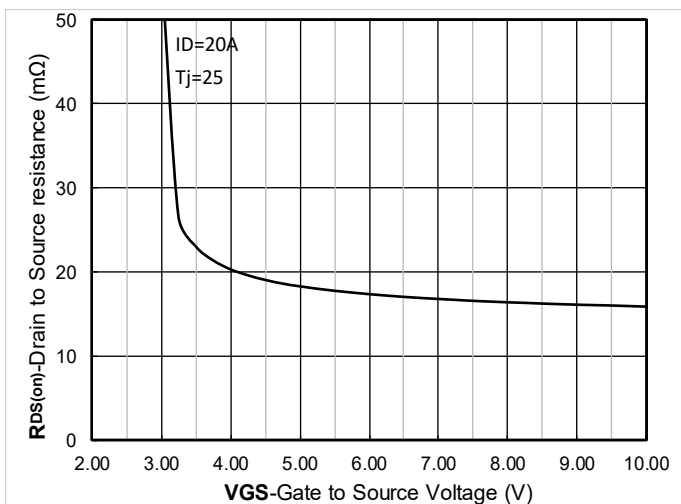


Figure5. On-Resistance vs. Gate to Source Voltage

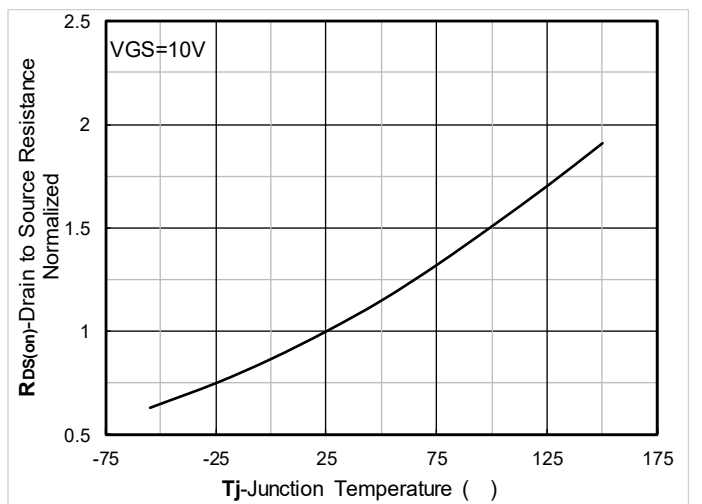


Figure6. Normalized On-Resistance



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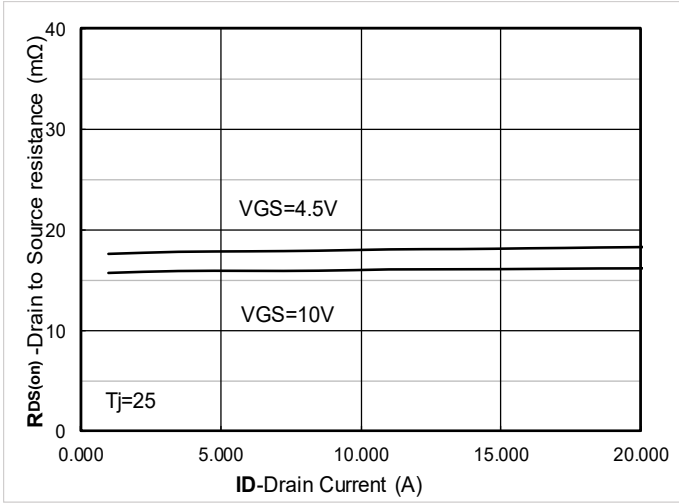


Figure 7. RDS(on) VS Drain Current

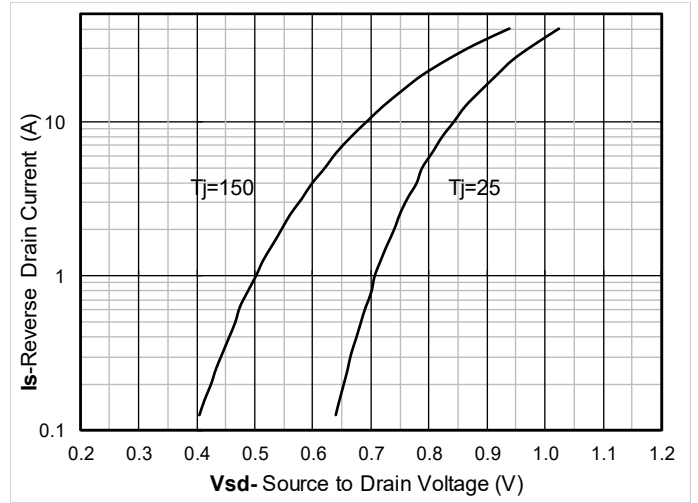


Figure 8. Forward characteristics of reverse diode

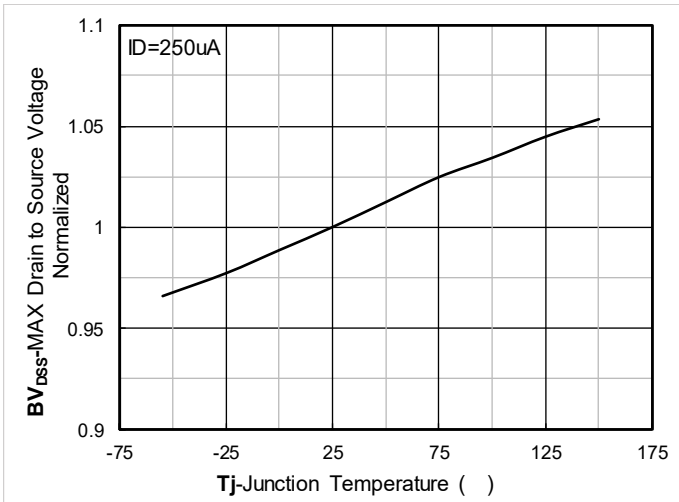


Figure 9. Normalized breakdown voltage

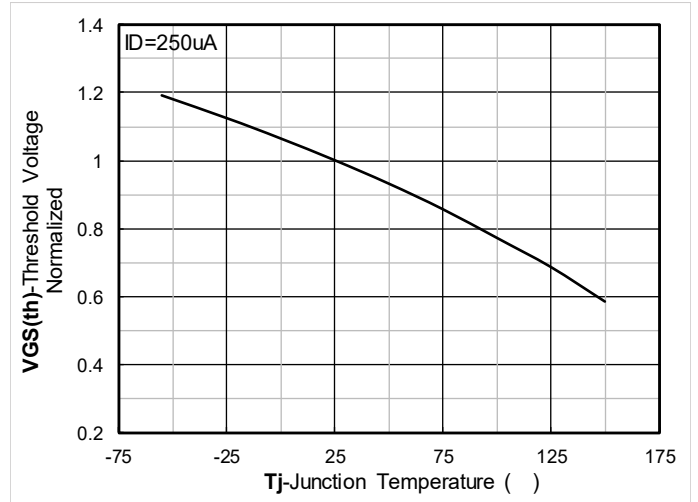


Figure 10. Normalized Threshold voltage

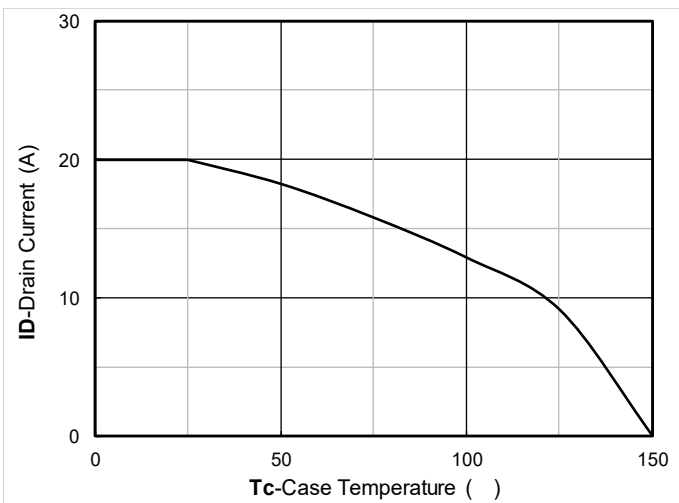


Figure 11. Current dissipation

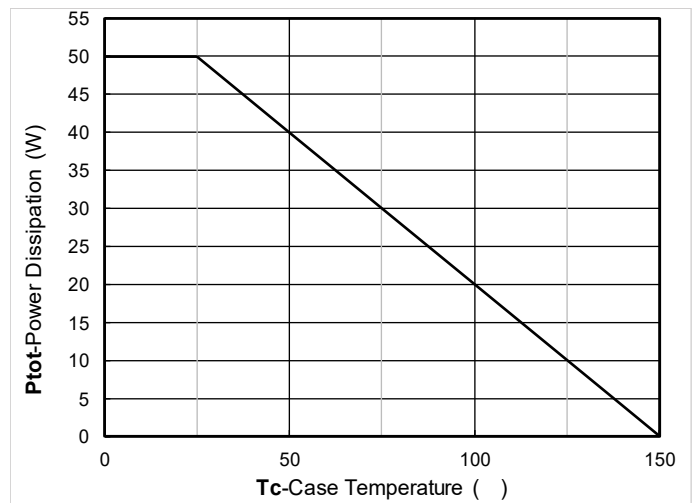


Figure 12. Power dissipation



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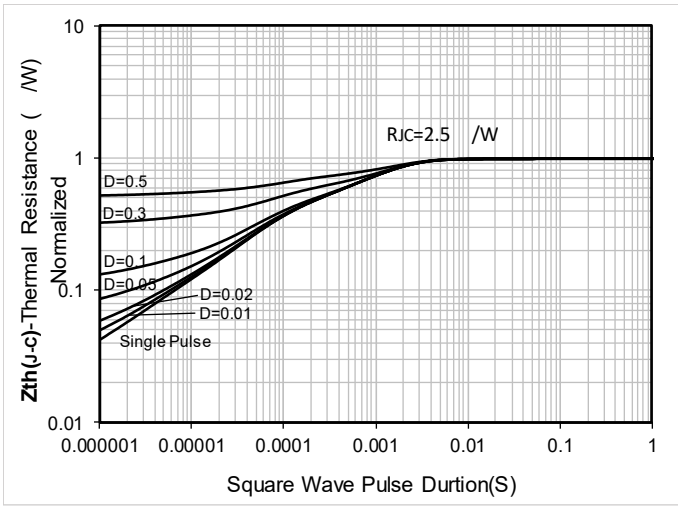


Figure 13. Maximum Transient Thermal Impedance

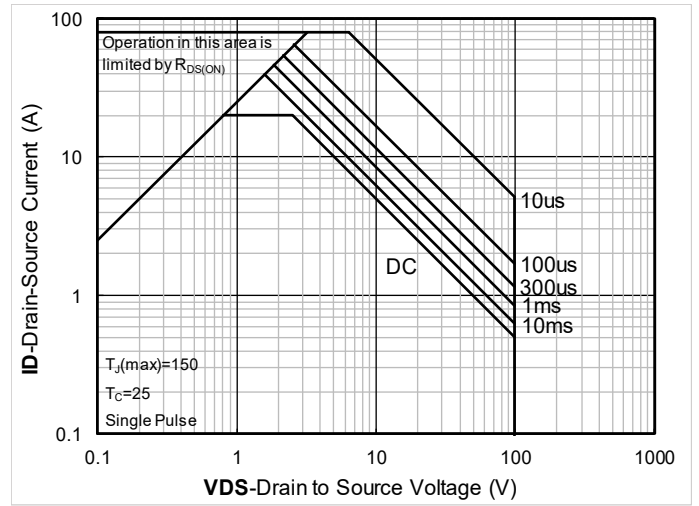
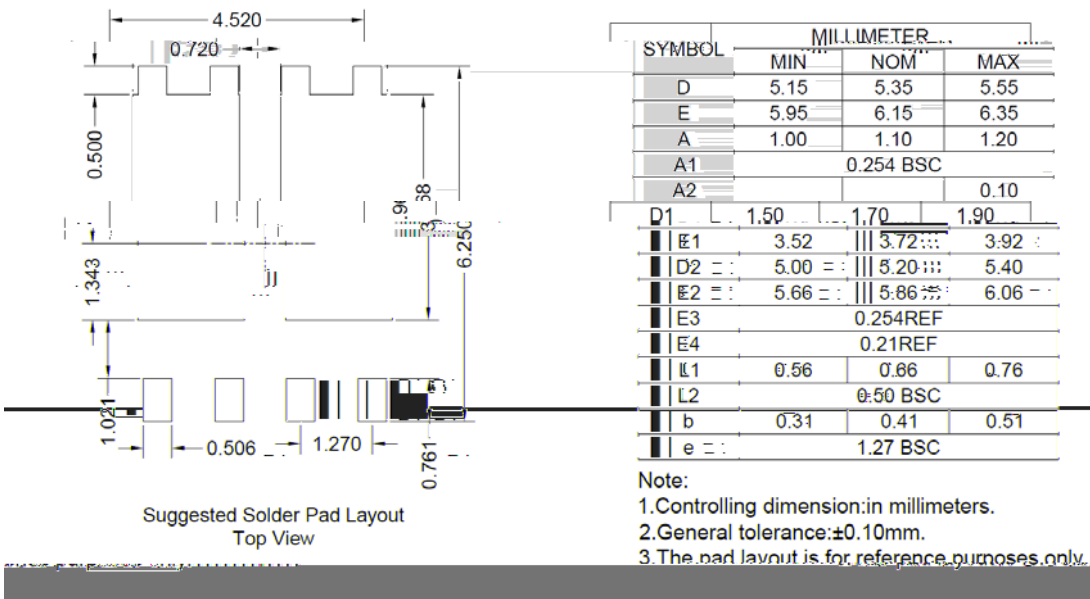
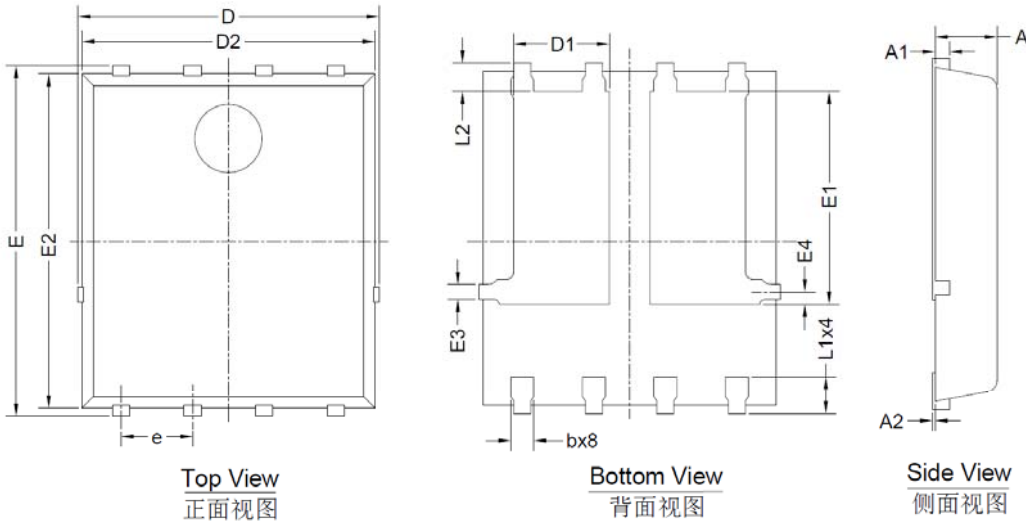


Figure 14. Safe Operation Area



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■ PDFN5060-8L Package information





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