



N-Channel and N-Channel Complementary MOSFET

Product Summary

- V_{DS} 100V
- I_D 3A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) 260m Ω
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) 270m Ω
- 100% EAS Tested

General Description

- Trench Power MV MOSFET technology
- Voltage controlled small signal switch
- Fast Switching Speed
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

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YJGD03N10A

=25 unless otherwise noted)

Symbol	Conditions	Min	Typ	Max	Units
BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
	$V_{DS}=100V, V_{GS}=0V, T_j=150^\circ C$	-	-	100	
I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.1	1.8	3.0	V
$R_{DS(ON)}$	$V_{GS}=10V, I_D=3A$	-	195	260	m Ω
	$V_{GS}=4.5V, I_D=1A$	-	200	270	
V_{SD}	$I_S=3A, V_{GS}=0V$	-	0.85	1.2	V
R_G	$f=1MHz$	-	1.7	-	Ω
I_S		-	-	3	A
C_{iss}	$V_{DS}=50V, V_{GS}=0V, f=1MHz$	-	380	-	pF
C_{oss}		-	15	-	
C_{rss}		-	10	-	
Q_g	$V_{GS}=10V, V_{DS}=50V, I_D=1A$	-	8	-	nC
Q_{gs}		-	1	-	
Q_{gd}		-	1.6	-	
Q_{rr}	$I_F=1A, di/dt=600A/us$	-	22	-	nC
t_{rr}		-	8	-	ns
$t_{D(on)}$	$V_{GS}=10V, V_{DD}=50V, I_D=1A$ $R_{GEN}=2.2\Omega$	-	4.5	-	ns
t_r		-	6.5	-	
$t_{D(off)}$		-	12	-	
t_f		-	3.8	-	



Typical Electrical and Thermal Characteristics Diagrams

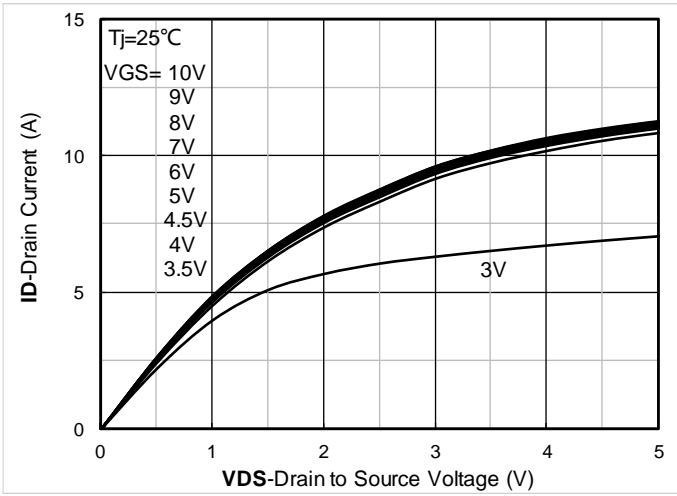


Figure 1. Output Characteristics

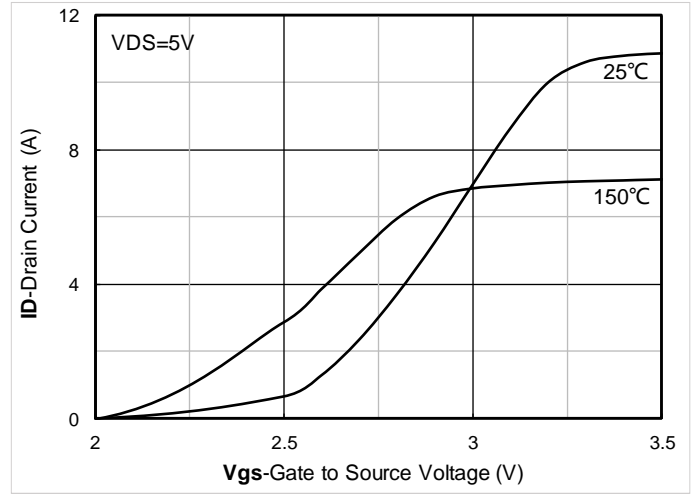


Figure 2. Transfer Characteristics

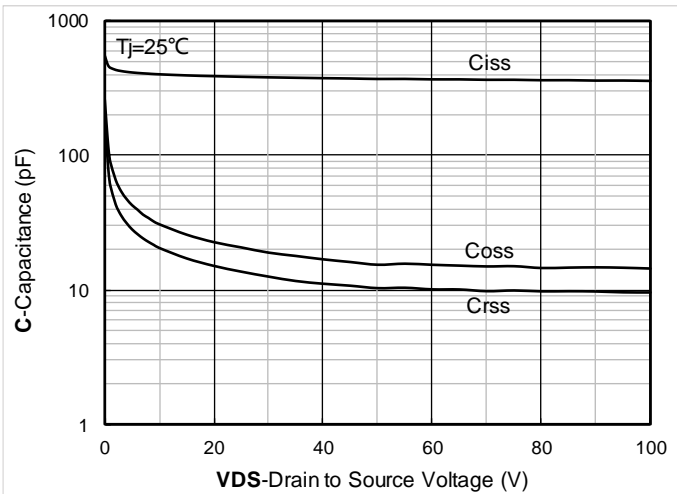


Figure 3. Capacitance Characteristics

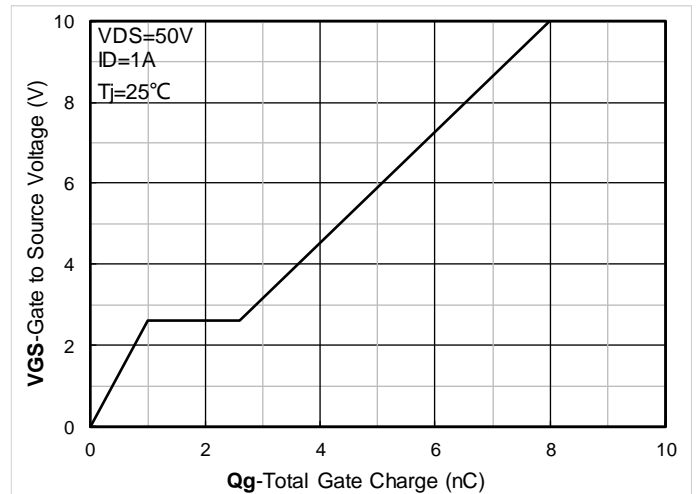


Figure 4. Gate Charge

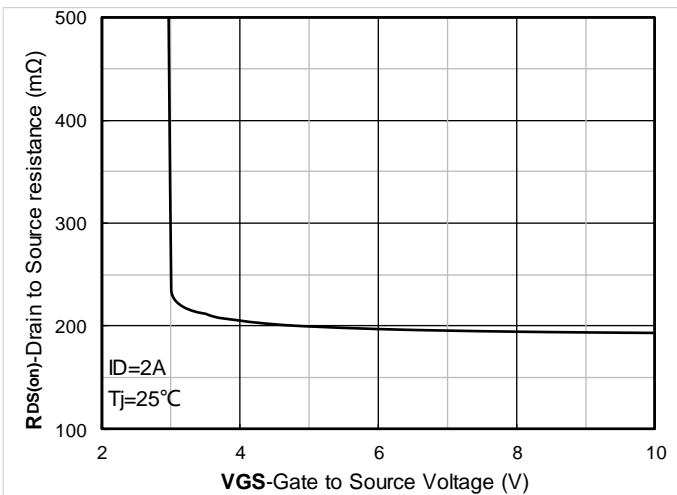


Figure 5. On-Resistance vs Gate to Source Voltage

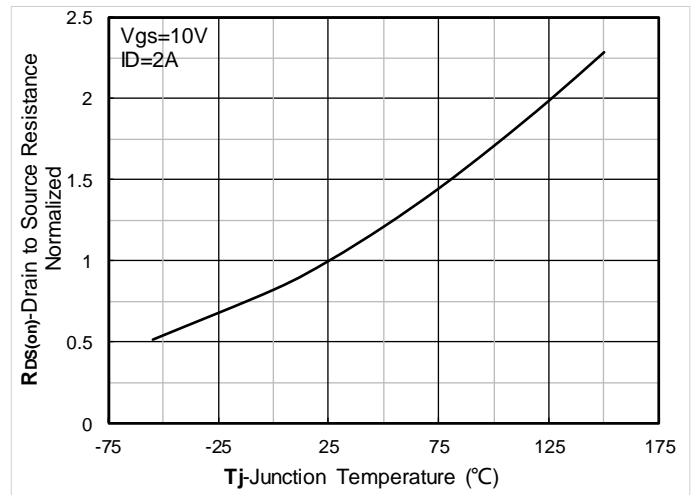


Figure 6. Normalized On-Resistance



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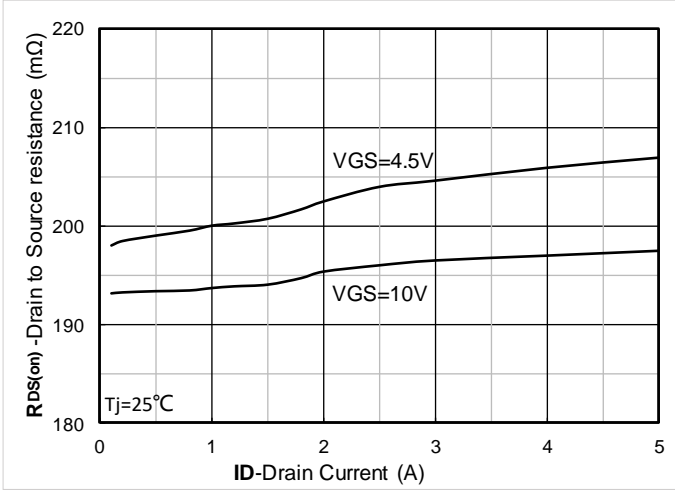


Figure 7. $R_{DS(on)}$ VS Drain Current

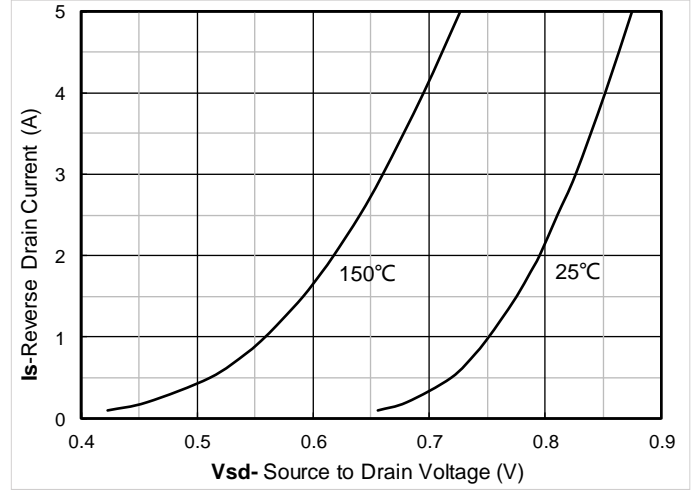


Figure 8. Forward characteristics of reverse diode

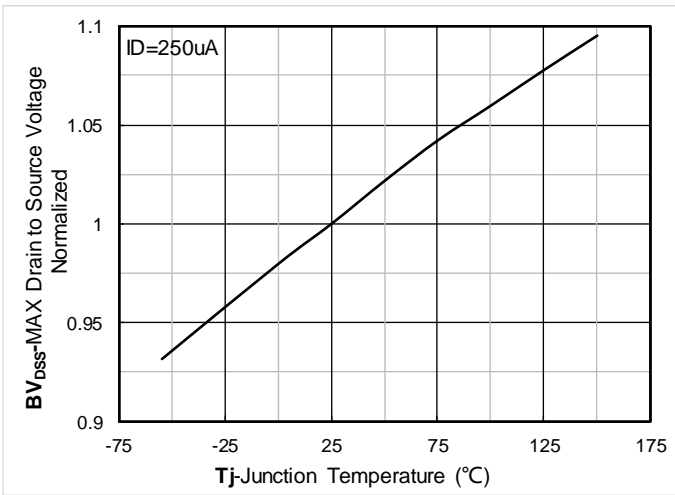


Figure 9. Normalized breakdown voltage

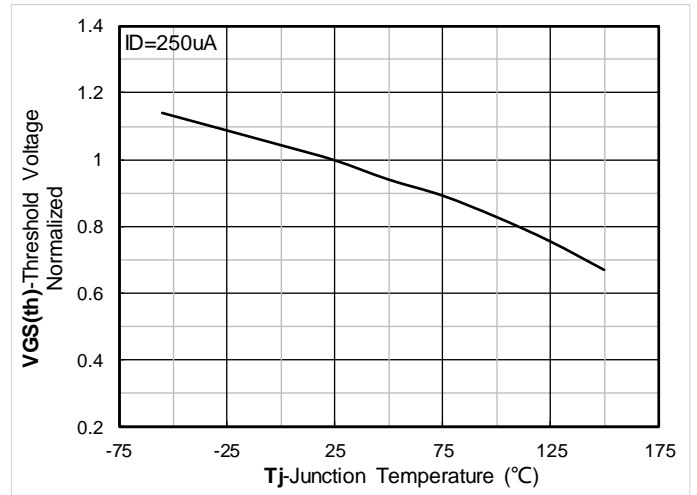


Figure 10. Normalized Threshold voltage

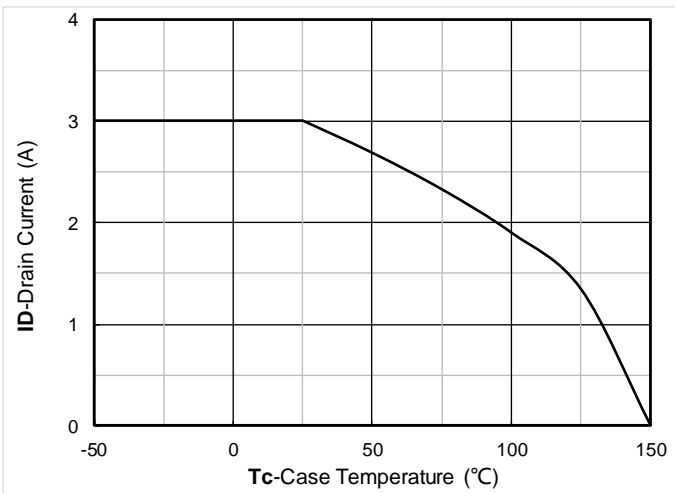


Figure 11. Current dissipation

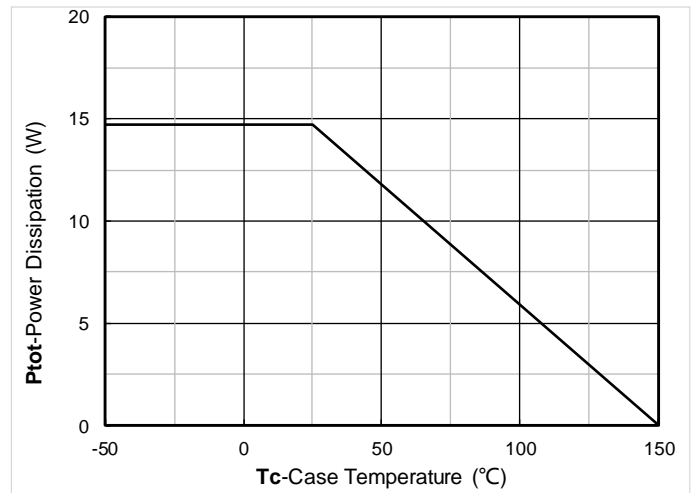


Figure 12. Power dissipation

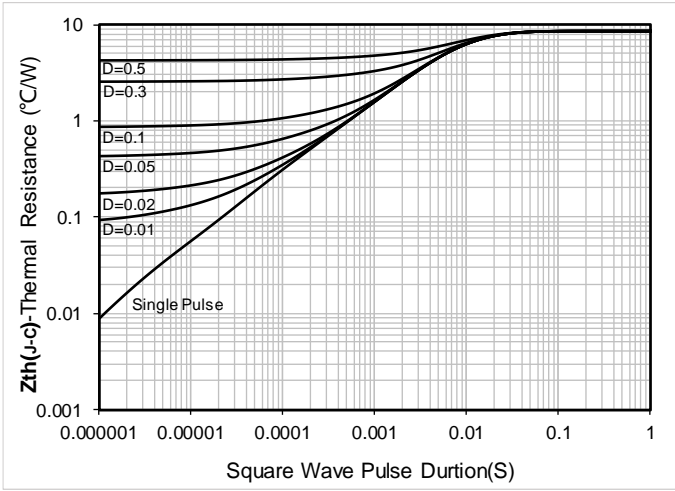


Figure 13. Maximum Transient Thermal Impedance

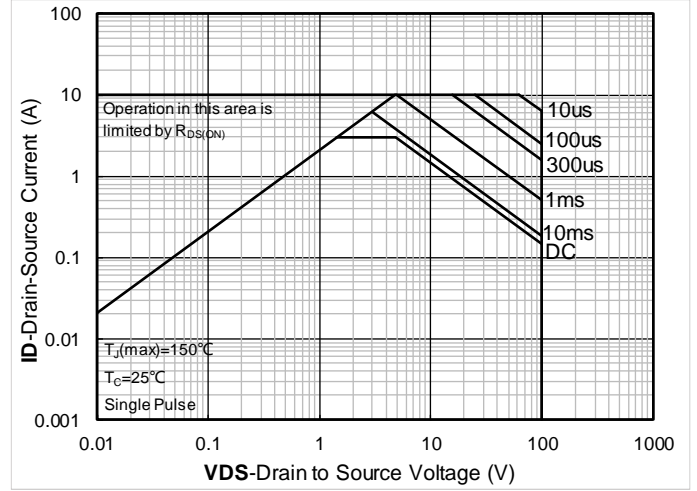


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

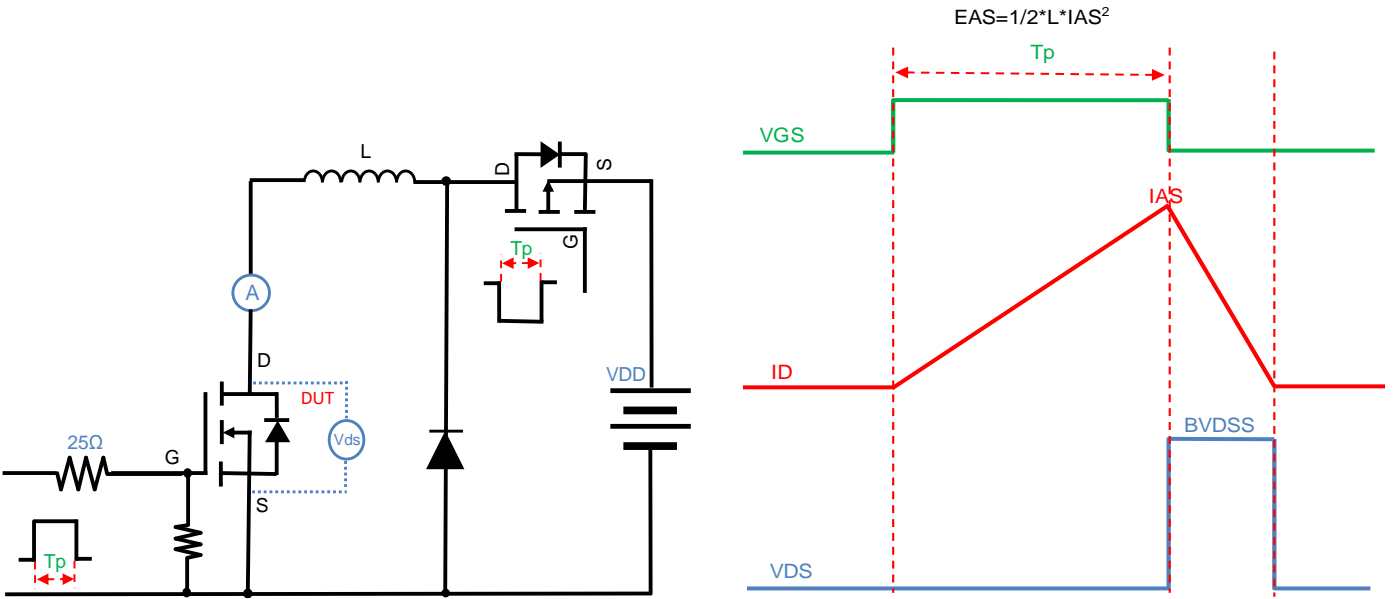


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

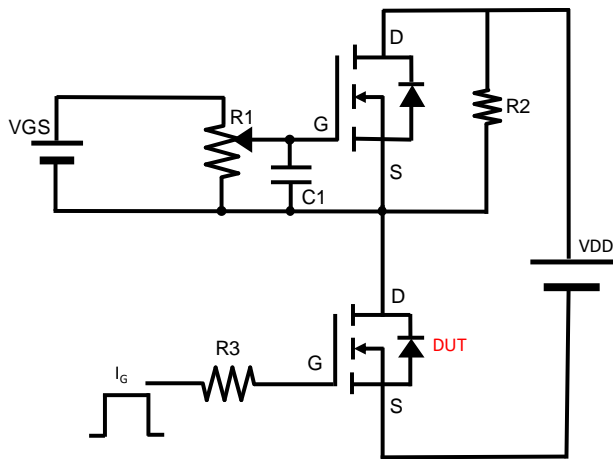


Figure B. Gate Charge Test Circuit & Waveform

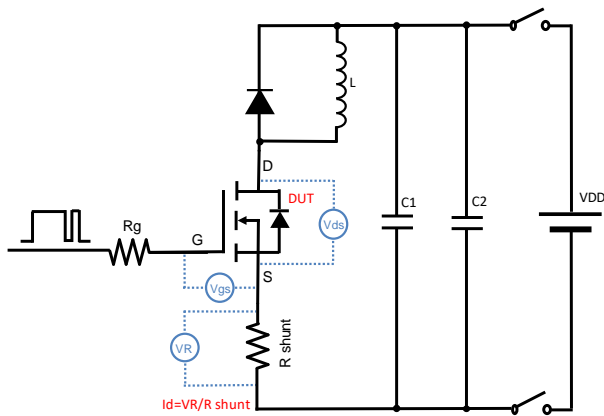


Figure C. Resistive Switching Test Circuit & Waveform

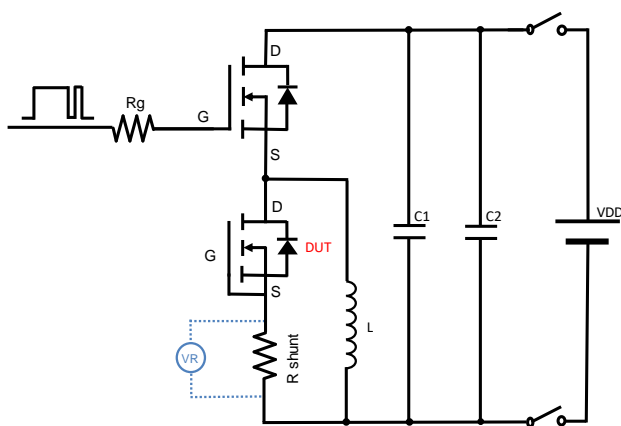


Figure D. Diode Recovery Test Circuit & Waveform



■ DFN5060-8L Package information

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	4.90	5.00	5.10
E	5.90	6.00	6.10
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	1.60	1.70	1.80
E1	3.65	3.75	3.85
L1	0.45	0.55	0.65
L2	0.80 BSC		
b	0.30	0.40	0.50
e	1.27 BSC		



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.

Suggested Solder Pad Layout
Top View



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