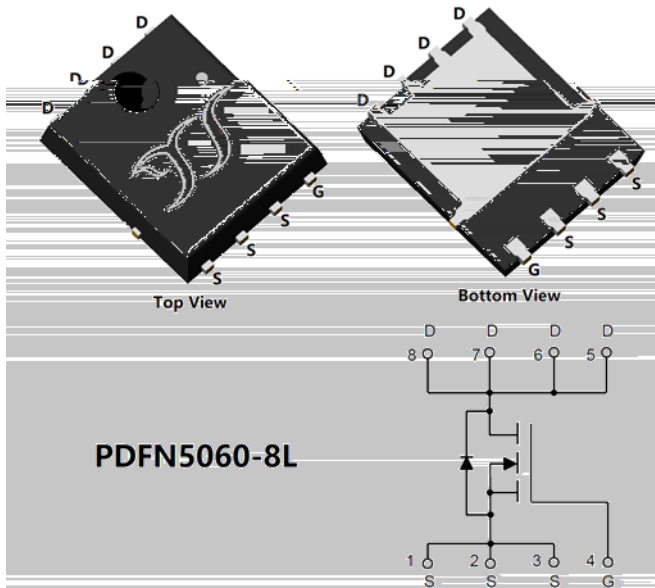


## N-Channel Enhancement Mode Field Effect Transistor



### Product Summary

$V_{DS}$	60V
$I_D$	95A
$R_{DS(ON)}$ ( at $V_{GS}=10V$ )	<2.5 mohm
$R_{DS(ON)}$ ( at $V_{GS}=4.5V$ )	<3.4 mohm
100% EAS Tested	
100% $\nabla V_{DS}$ Tested	

### General Description

Split Gate Trench MOSFET technology  
 Excellent package for heat dissipation  
 High density cell design for low  $R_{DS(ON)}$   
 Moisture Sensitivity Level 1  
 Epoxy Meets UL 94 V-0 Flammability Rating  
 Halogen Free

### Applications

DC-DC Converters  
 Power management functions  
 Synchronous-rectification applications

### Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	60	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current (Silicon limited)	$I_D$	155	A
Drain Current <sup>A</sup>	$I_D$	$T_C=25^\circ\text{C}$	95
		$T_C=100^\circ\text{C}$	60
Pulsed Drain Current <sup>B</sup>	$I_{DM}$	390	A
Avalanche energy <sup>C</sup>	EAS	500	mJ
Total Power Dissipation <sup>D</sup>	$P_D$	120	W
Thermal Resistance Junction-to-Case	$R_{JC}$	1.04	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Ambient <sup>E</sup>	$R_{JA}$	20	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG95G06A	F1	YJG95G06A	5000	10000	50000	13 reel



# YJG95G06A

## Electrical Characteristics (T<sub>J</sub>=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250 ;	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	;
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250 ;	1.2	1.6	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =20A		2.1	2.5	m
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =15A		2.7	3.4	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V			1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				95	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=100KHZ		5950		pF
Output Capacitance	C <sub>oss</sub>			1250		
Reverse Transfer Capacitance	C <sub>rss</sub>			85		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =50A		93		nC
Gate-Source Charge	Q <sub>gs</sub>			17		
Gate-Drain Charge	Q <sub>gd</sub>			14		
Reverse Recovery Chrage	Q <sub>rr</sub>	I <sub>F</sub> =25A, di/dt=100A/us		73		
Reverse Recovery Time	t <sub>rr</sub>			68		
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =30V, I <sub>D</sub> =25A R <sub>GEN</sub> =2		22.5		ns
Turn-on Rise Time	t <sub>r</sub>			6.7		
Turn-off Delay Time	t <sub>d(off)</sub>			80.3		
Turn-off fall Time	t <sub>f</sub>			26.9		

**Note:**

- The maximum current rating is package limited.
- Repetitive rating; pulse width limited by max. junction temperature.
- V<sub>DD</sub>=50 V, R<sub>G</sub>=25 Ω, L=0.5mH, starting T<sub>J</sub>=25 °C.
- P<sub>D</sub> is based on max. junction temperature, using junction-case thermal resistance.
- The value of R<sub>JA</sub> is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with Ta=25 °C.



# YJG95G06A

## Typical Performance Characteristics

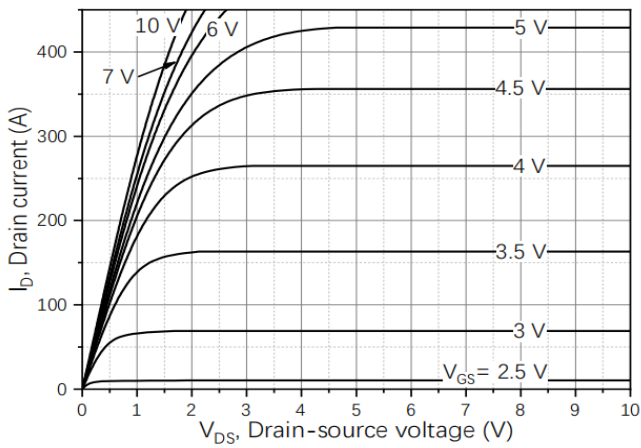


Figure1. Output Characteristics

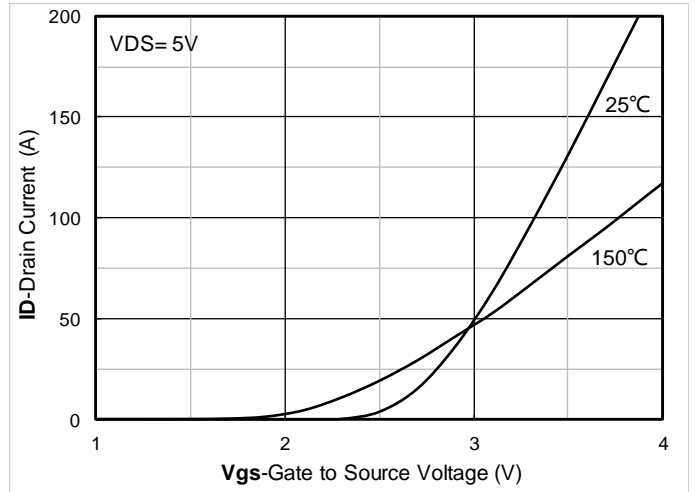


Figure2. Transfer Characteristics

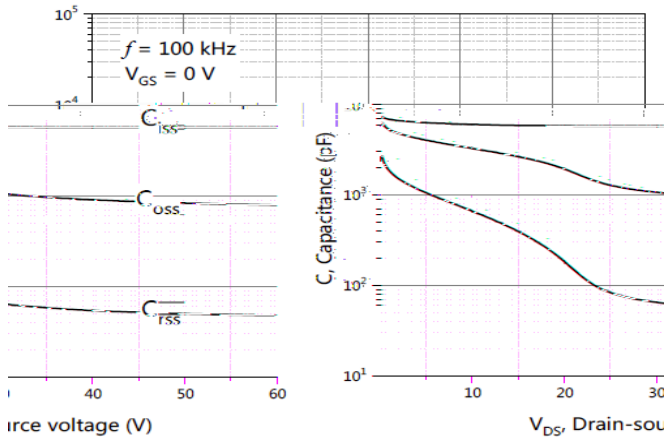


Figure3. Capacitance Characteristics

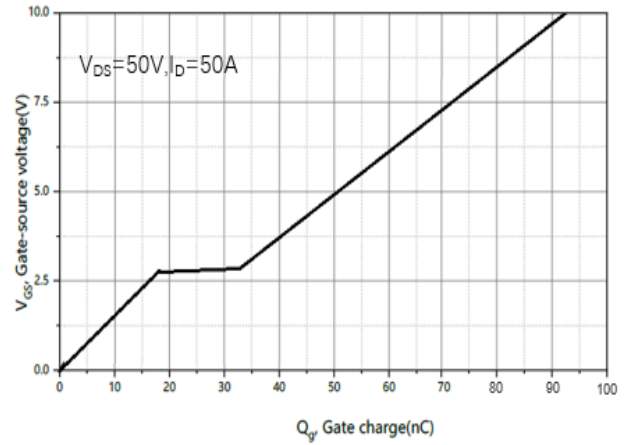


Figure4. Gate Charge

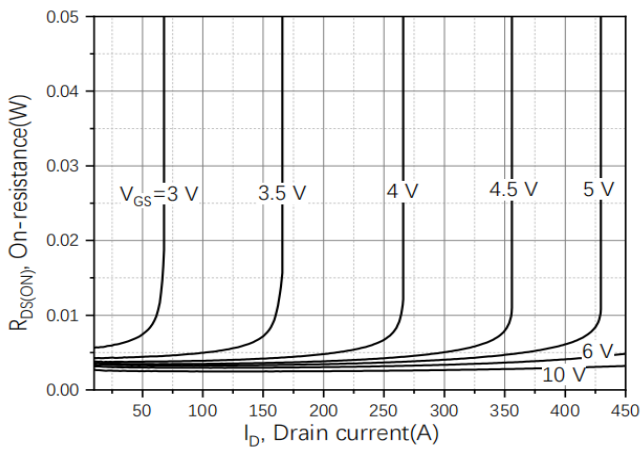


Figure5. Drain-Source on Resistance

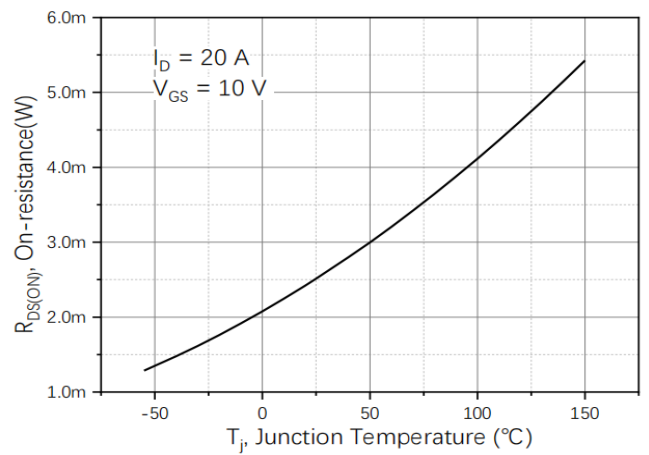


Figure6. Drain-Source on Resistance



# YJG95G06A

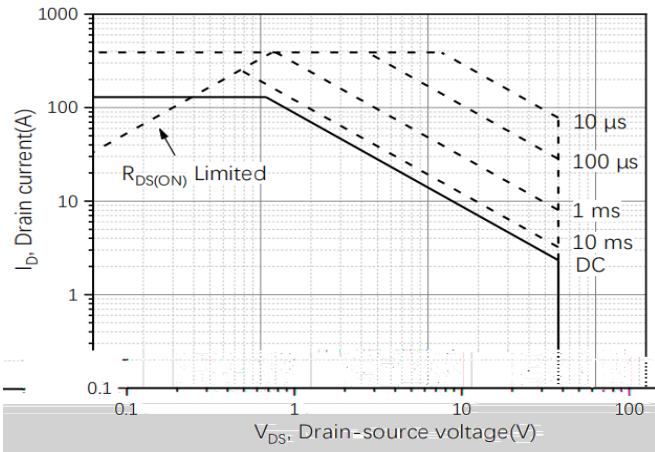


Figure 7. Safe Operation Area

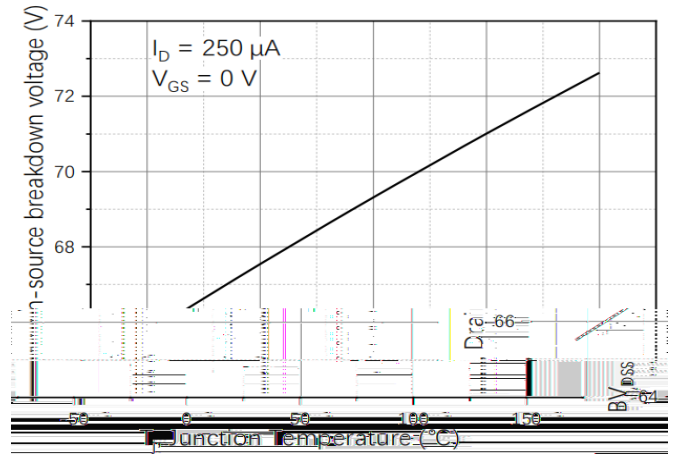


Figure 8. Drain-source breakdown voltage

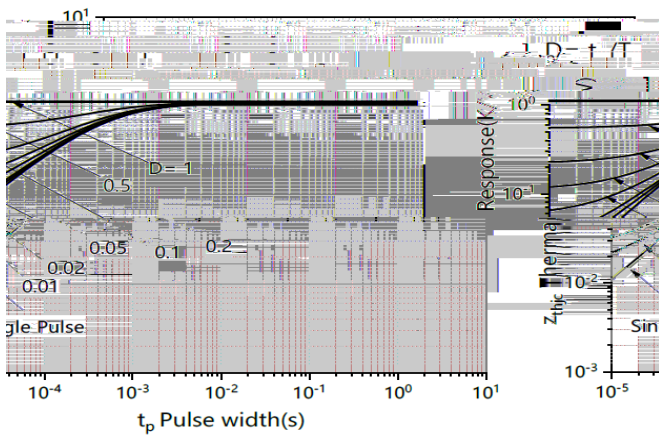


Figure 9. Transient thermal impedance

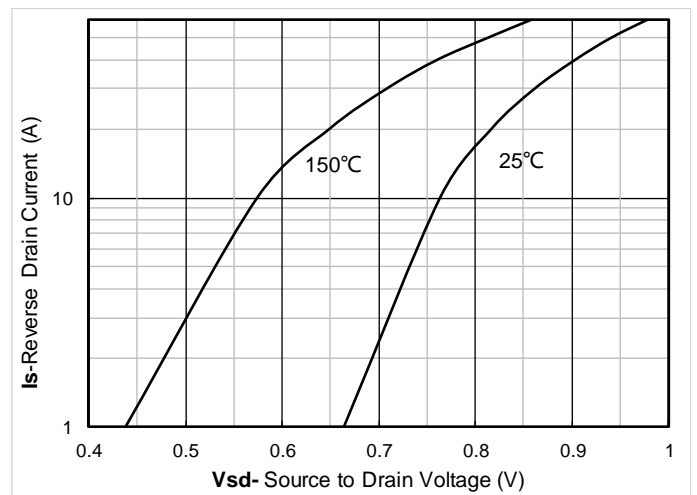


Figure 10. Forward characteristics of reverse diode

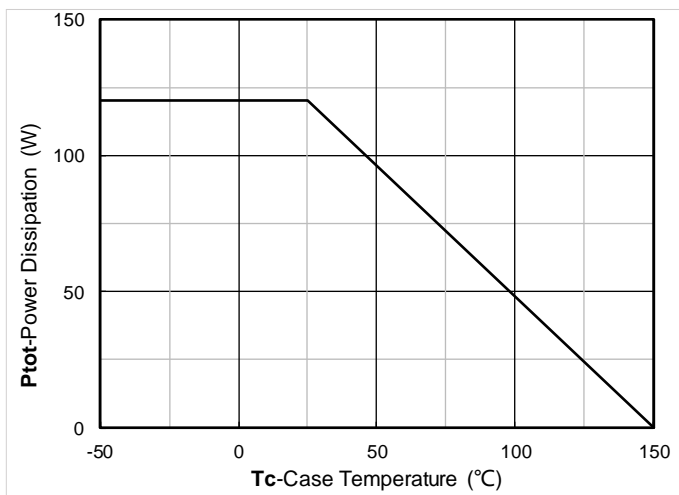


Figure 11. Power dissipation

## Test circuits and waveforms

Figure A: Gate Charge Test Circuit & Waveforms

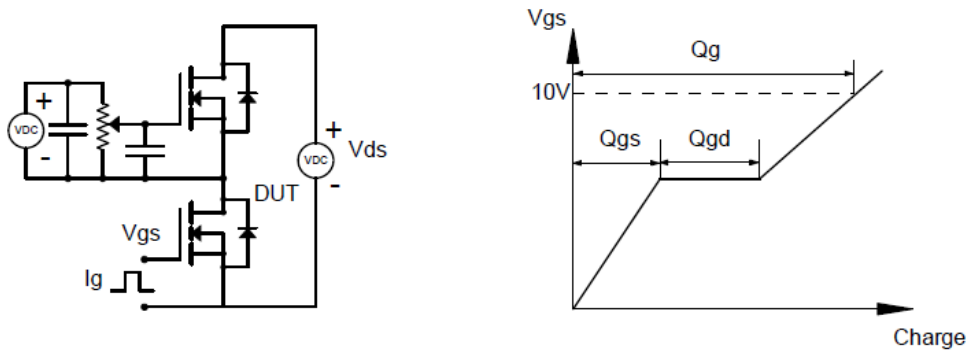


Figure B: Resistive Switching Test Circuit & Waveforms

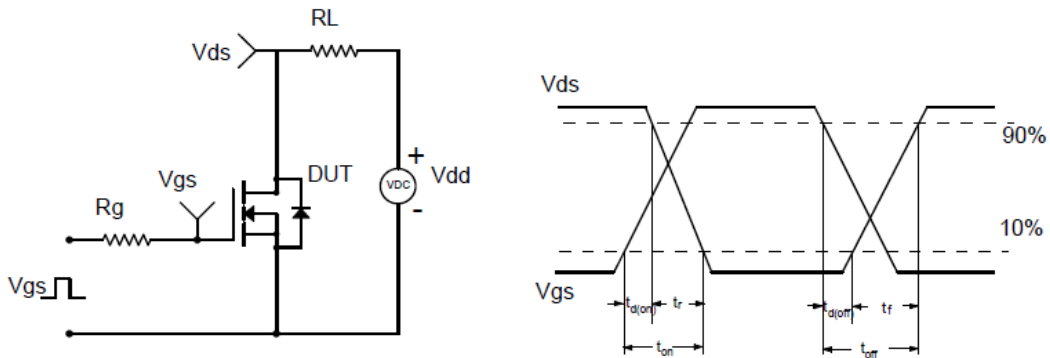


Figure C: Unclamped Inductive Switching (UIS) Test

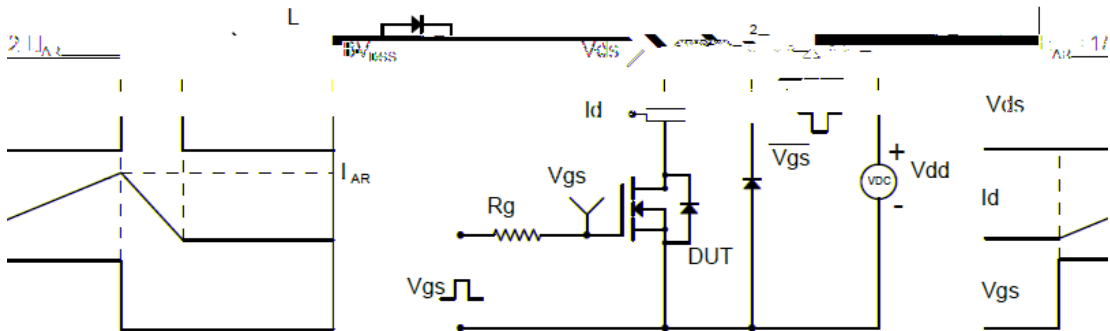
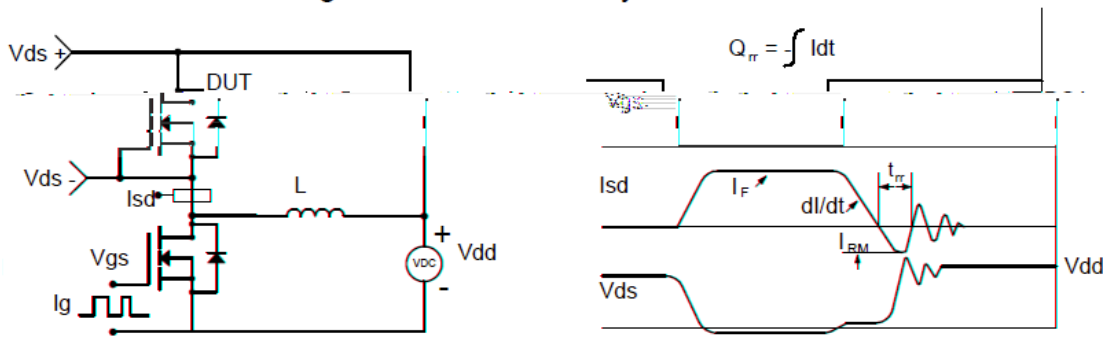


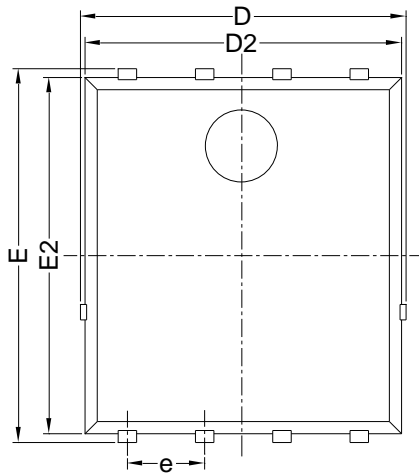
Figure D: Diode Recovery Test Circuit & Waveforms



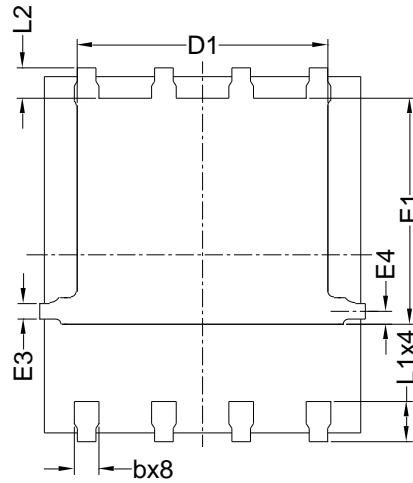


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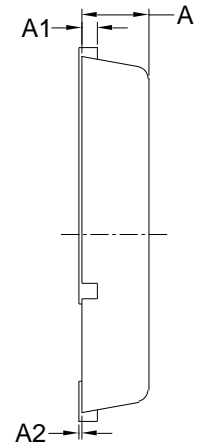
## PDFN5060-8L-B-1.1MM Package Information



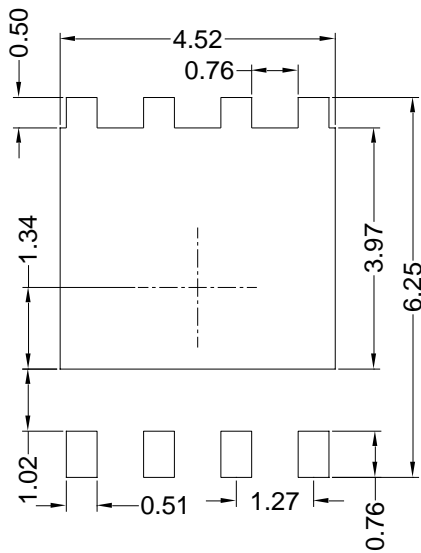
Top View  
正面视图



Bottom View  
背面视图



Side View  
侧面视图



Suggested Solder Pad Layout  
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$  mm.
3. The pad layout is for reference purposes only.



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