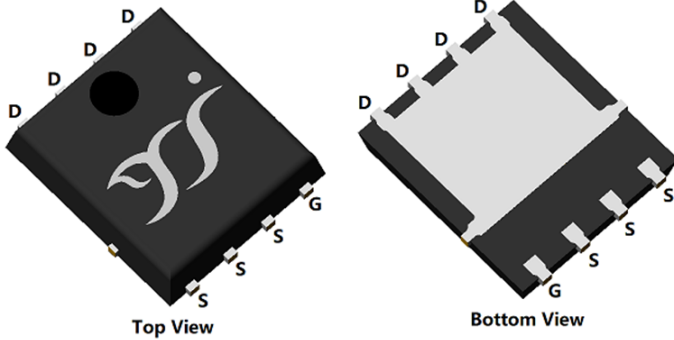


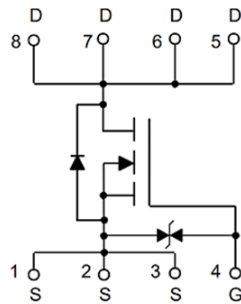
## N-Channel Enhancement Mode Field Effect Transistor



Top View

Bottom View

PDFN5060-8L



### Product Summary

$V_{DS}$	60V
$I_D$	85A
$R_{DS(ON)}$ ( at $V_{GS}=10V$ )	< 3.7 mohm
$R_{DS(ON)}$ ( at $V_{GS}=4.5V$ )	< 5.0 mohm
100% EAS Tested	
100% $\nabla V_{DS}$ Tested	
ESD Protected up to 2.0KV(HBM)	

### General Description

Split Gate Trench MOSFET technology  
 Excellent package for heat dissipation  
 High density cell design for low  $R_{DS(ON)}$   
 Moisture Sensitivity Level 1  
 Epoxy Meets UL 94 V-0 Flammability Rating  
 Halogen Free

### Applications

DC-DC Converters  
 Power management functions  
 Synchronous-rectification application

### Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	60	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current <sup>A</sup>	$I_D$	$T_C=25^\circ\text{C}$	85
		$T_C=100^\circ\text{C}$	54
Pulsed Drain Current <sup>B</sup>	$I_{DM}$	340	A
Avalanche energy	EAS	400	mJ
Total Power Dissipation <sup>C</sup>	$P_D$	$T_C=25^\circ\text{C}$	110
		$T_C=100^\circ\text{C}$	44
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 ~ +150	$^\circ\text{C}$

### Thermal resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	R	14	17	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Ambient <sup>D</sup>		Steady-State	40	
Thermal Resistance Junction-to-Case	R	0.85	1.1	

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG85G06AK	F1	YJG85G06AK	5000	10000	100000	13 reel



# YJG85G06AK

## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	A
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±10	
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250	1.0	1.6	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =20A		2.9	3.7	m
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =20A		3.8	5.0	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V		0.8	1.3	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				85	A
Gate resistance	R <sub>g</sub>	f=1MHz		2		
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, f=1MHZ		4650		pF
Output Capacitance	C <sub>oss</sub>			850		
Reverse Transfer Capacitance	C <sub>rss</sub>			65		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =25A		70.78		nC
Gate-Source Charge	Q <sub>gs</sub>			16.64		
Gate-Drain Charge	Q <sub>gd</sub>			10.62		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>r</sub> =20A, di/dt=500A/us		39.8		
Reverse Recovery Time	t <sub>rr</sub>			41.6		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =30V, I <sub>D</sub> =25A R <sub>GEN</sub> =2		15.9		ns
Turn-on Rise Time	t <sub>r</sub>			55.2		
Turn-off Delay Time	t <sub>D(off)</sub>			57.5		
Turn-off fall Time	t <sub>f</sub>			91.3		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V<sub>DD</sub>=50V, V<sub>GS</sub>=10V, L=2mH, I<sub>AS</sub>=20A.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R<sub>qJA</sub> is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25°C. The °C. The value in any given

application depends on the user's specific board design.



## Typical Performance Characteristics

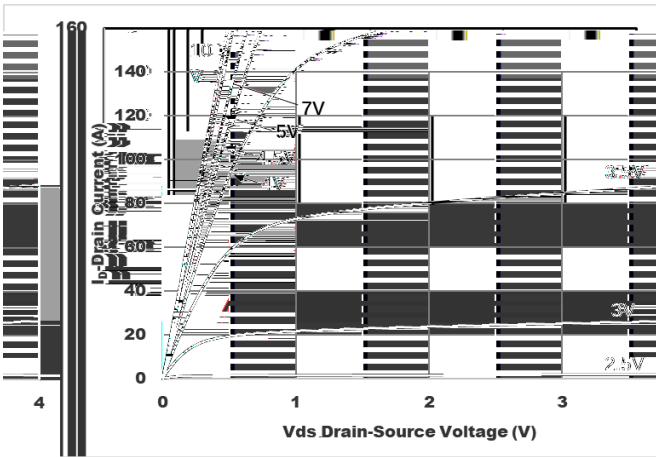


Figure1. Output Characteristics

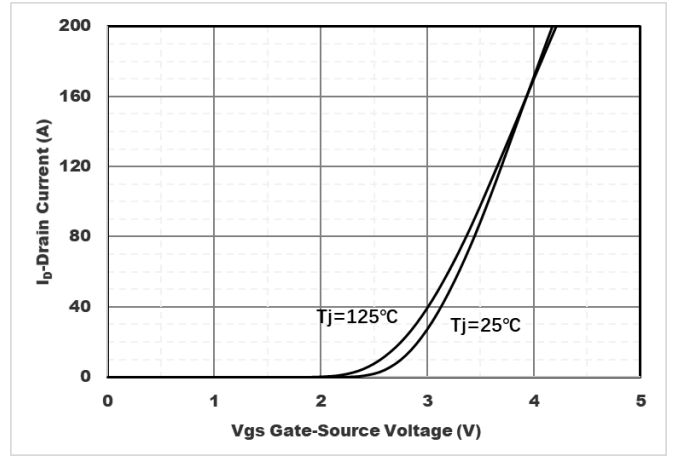


Figure2. Transfer Characteristics

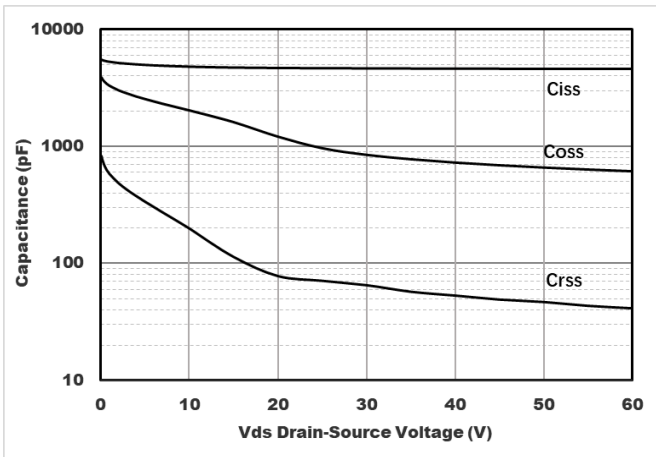


Figure3. Capacitance Characteristics

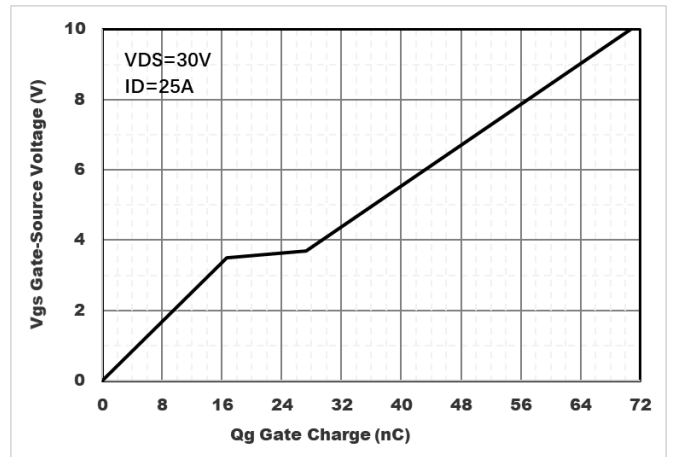


Figure4. Gate Charge

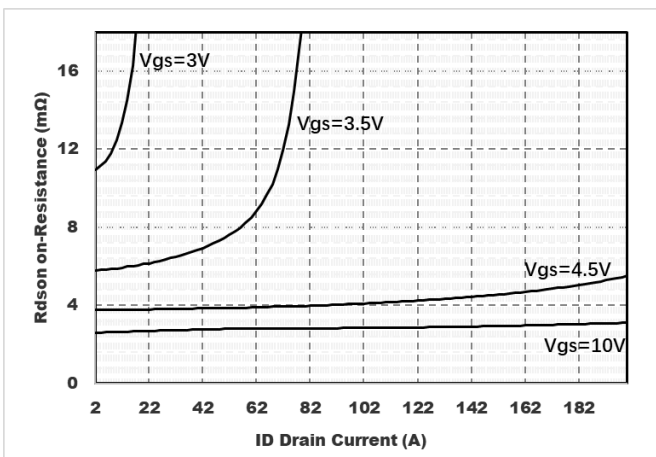


Figure5. Drain-Source on Resistance

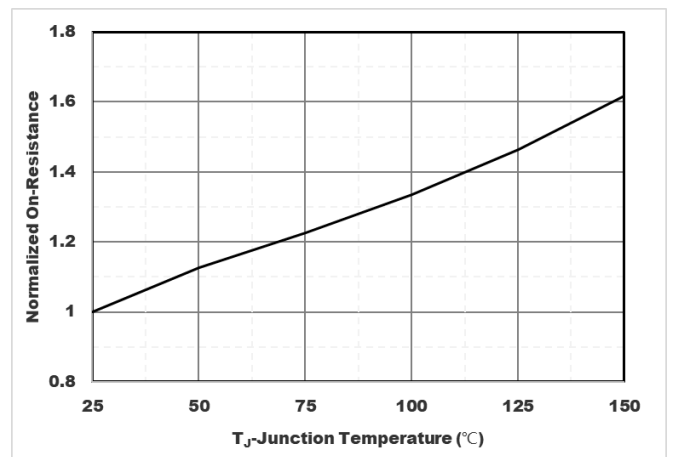


Figure6. Drain-Source on Resistance

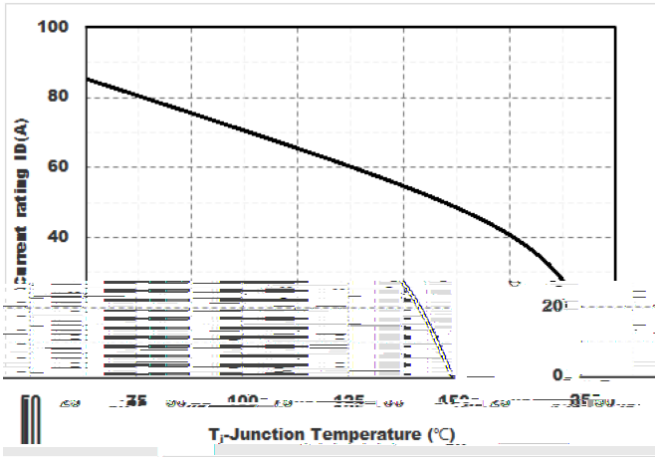


Figure7. Drain current

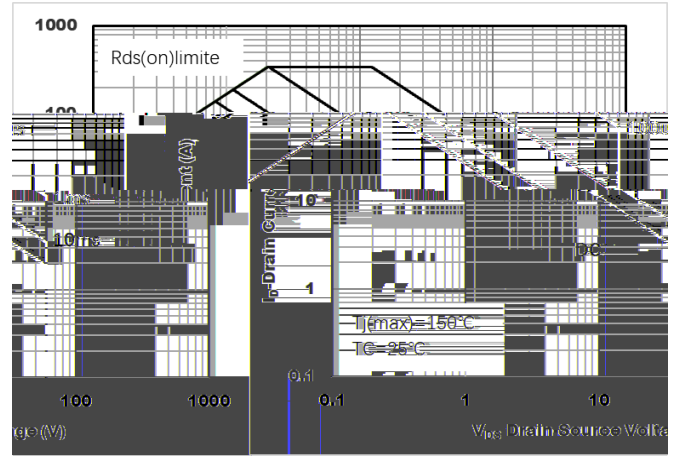


Figure8. Safe Operation Area

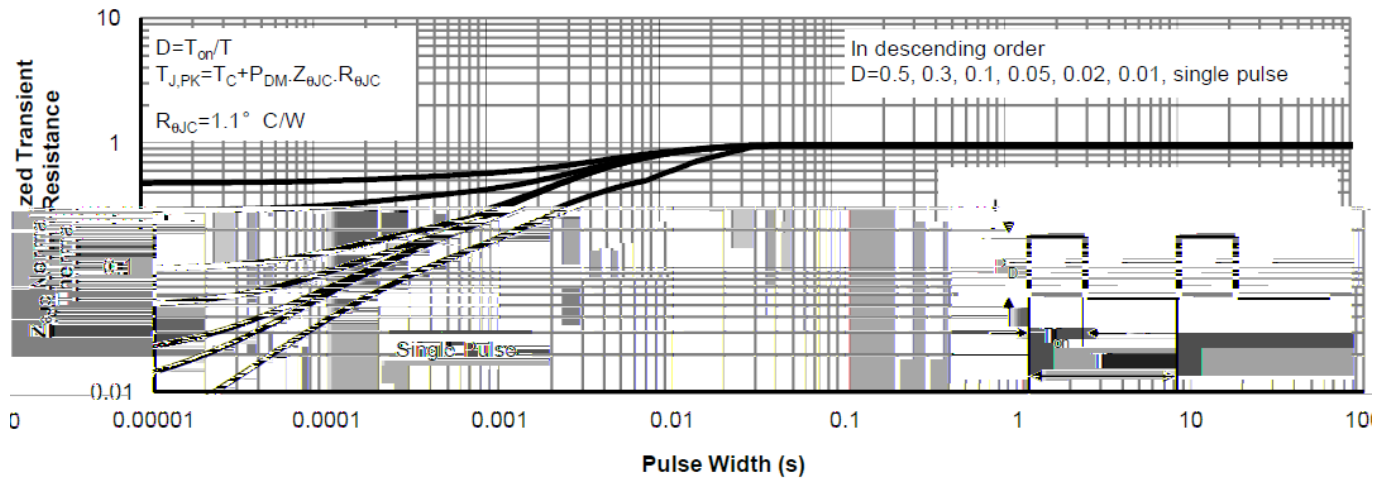
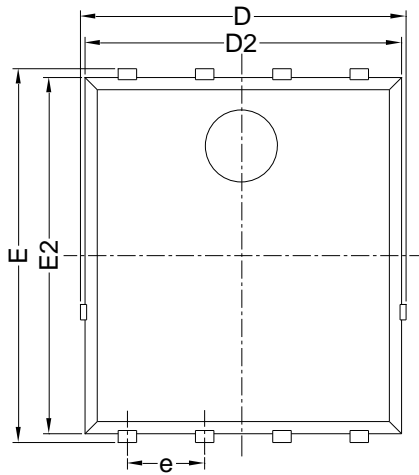


Figure9. Normalized Maximum Transient Thermal Impedance

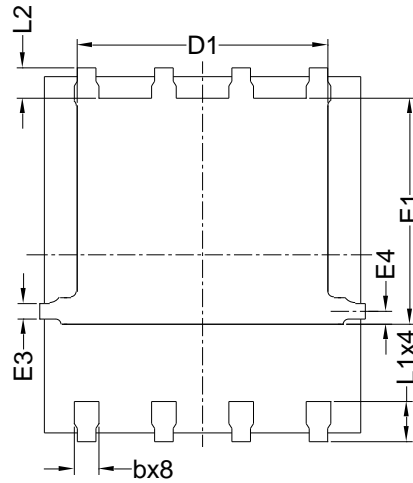


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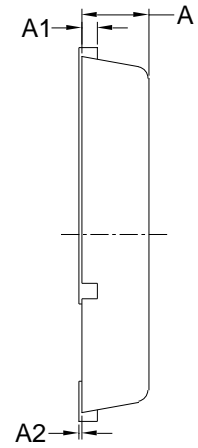
## PDFN5060-8L-B-1.1MM Package information



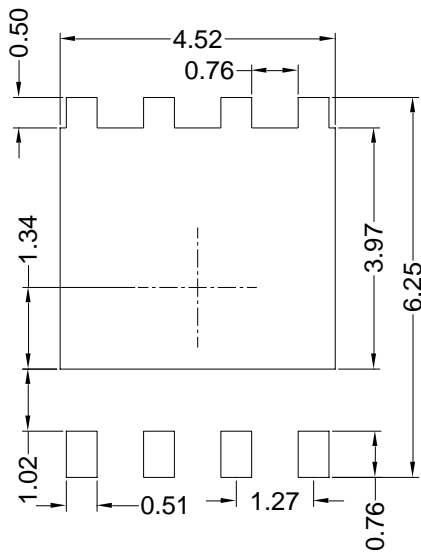
Top View  
正面视图



Bottom View  
背面视图



Side View  
侧面视图



Suggested Solder Pad Layout  
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.



# YJG85G06AK

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