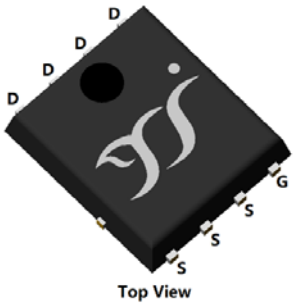
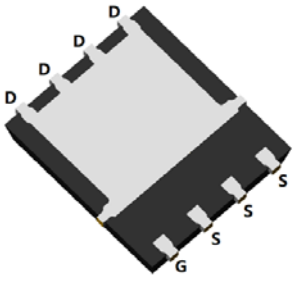
RoHS
COMPLIANT

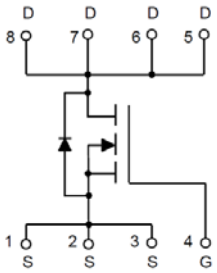


Top View



Bottom View

PDFN5060-8L



- V_{DS} 40V
- I_D 60A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜7mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Part no. with suffix "Q" means AEC-Q101 qualified

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ (T_A=25℃ unless otherwise noted)

Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	13	A
	T_A =100℃		8.5	
	T_C=25℃		60	
	T_C =100℃		38	
Pulsed Drain Current [A]		I_{DM}	180	A
Avalanche energy [B]		EAS	100	mJ
Total Power Dissipation [C]	T_A=25℃	P_D	2.5	W
	T_A =100℃		1	
	T_C=25℃		50	
	T_C =100℃		20	
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	2.5	℃/W
Thermal Resistance Junction-to-Ambient [D]		$R_{\theta JA}$	50	℃/W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ (Example)

YJG60N04AQ	F1	YJG60N04A	5000	10000	100000	13“ reel

■ (T_J=25℃ unless otherwise noted)

Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		5	7	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A, V_{GS}=0V		0.85	1.2	V
Gate resistance	R_G	f=1MHz		1.7		Ω
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1MHz		2100		pF
Output Capacitance	C_{oss}			250		
Reverse Transfer Capacitance	C_{rss}			210		
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=20V, I_D=20A	-	23	-	nC
Gate-Source Charge	Q_{gs}		-	3.5	-	
Gate-Drain Charge	Q_{gd}		-	6.5	-	
Reverse Recovery Charge	Q_{rr}	I_F=20A, di/dt=300A/us	-	10	-	nC
Reverse Recovery Time	t_{rr}		-	12	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=20V, I_D=20A R_{GEN}=3Ω	-	3.8	-	ns
Turn-on Rise Time	t_r		-	58	-	
Turn-off Delay Time	$t_{D(off)}$		-	20	-	
Turn-off fall Time	t_f		-	2.6	-	

A. Repetitive rating; pulse width limited by max. junction temperature.
B. T_J=25℃, V_{DD}=38V, V_G=10V, L=0.5mH, IAS=20A.
C. P_d is based on max. junction temperature, using junction-case thermal resistance.
D. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in the still air environment with T_A =25℃. The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

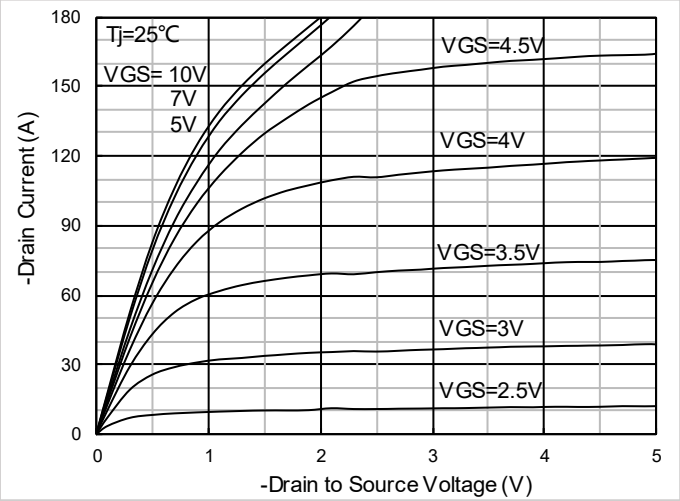


Figure 1. Output Characteristics

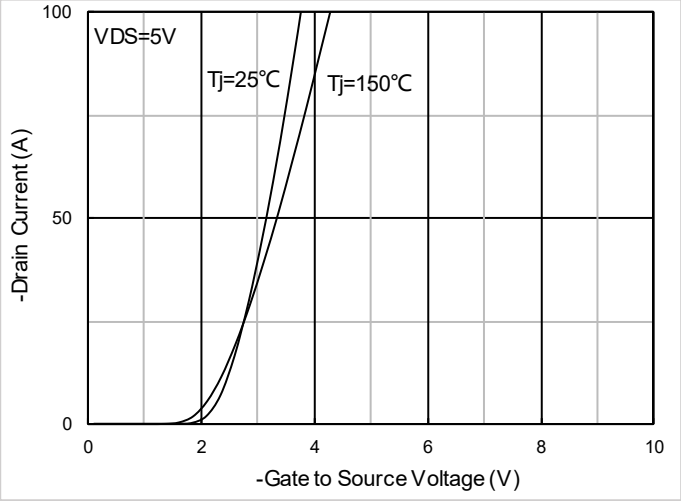


Figure 2. Transfer Characteristics

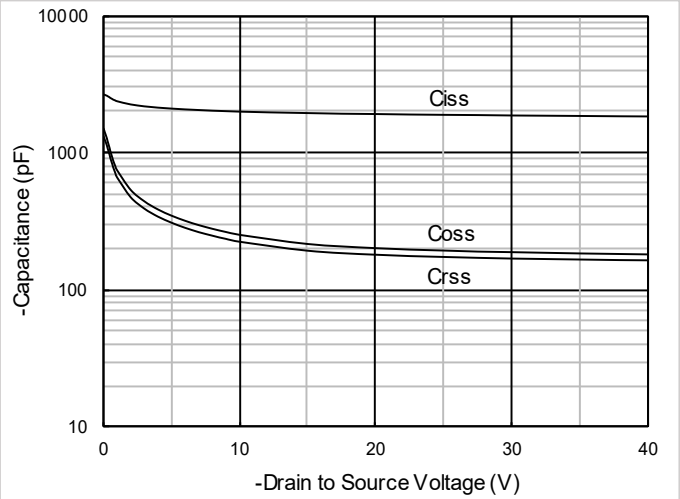


Figure 3. Capacitance Characteristics

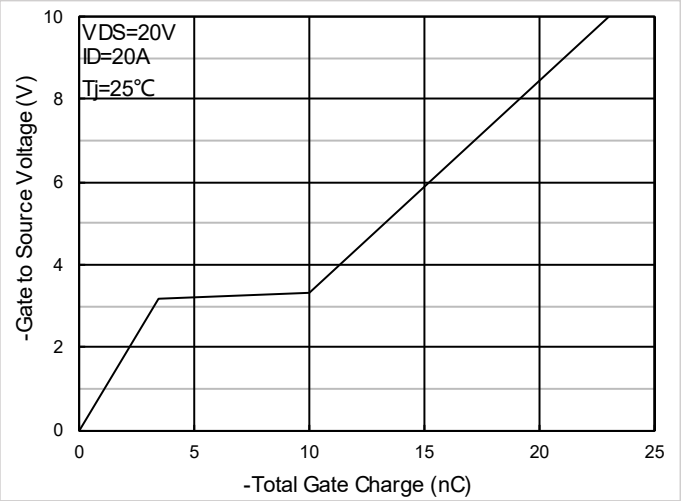


Figure 4. Gate Charge

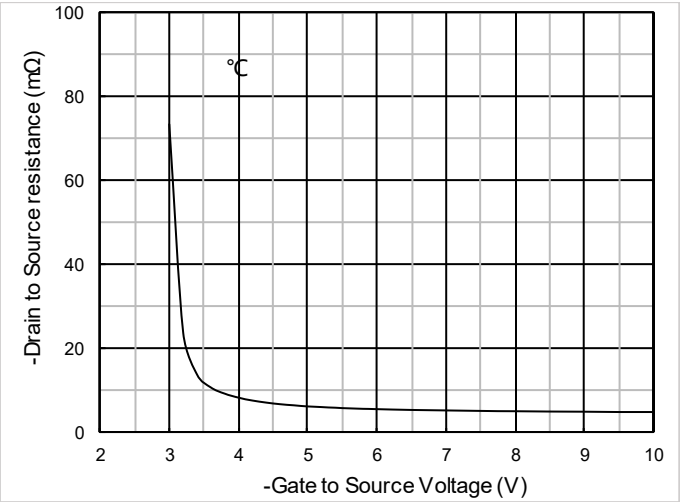


Figure 5. On-Resistance vs Gate to Source Voltage

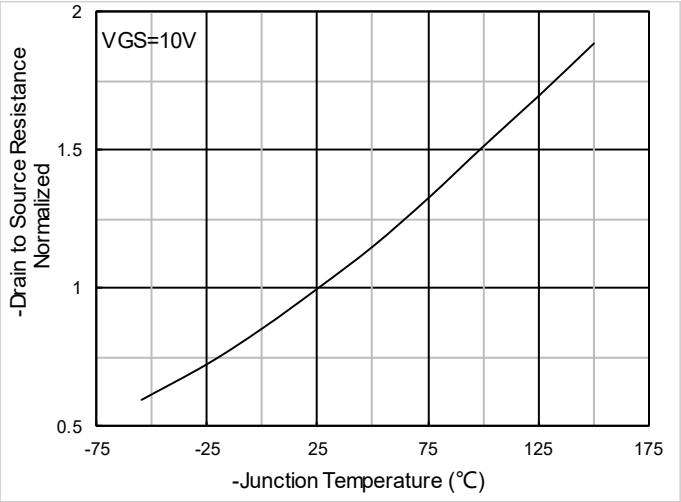


Figure 6. Normalized On-Resistance

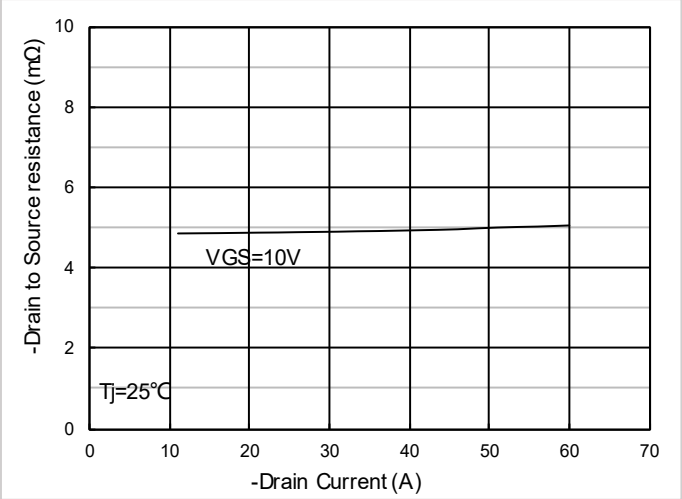


Figure 7. $R_{DS(on)}$ VS Drain Current

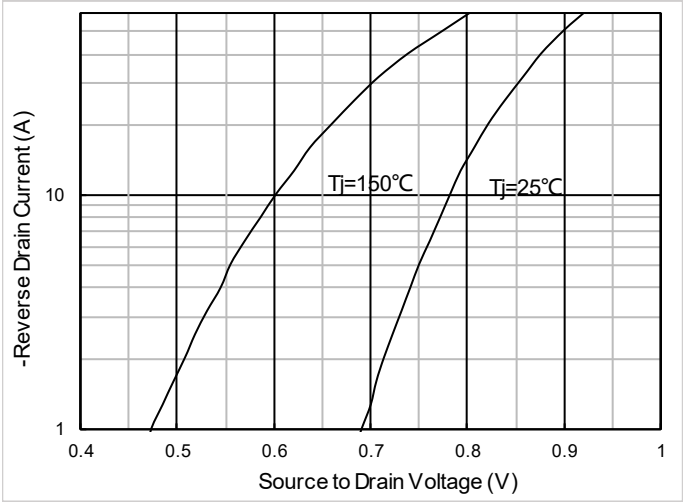


Figure 8. Forward characteristics of reverse diode

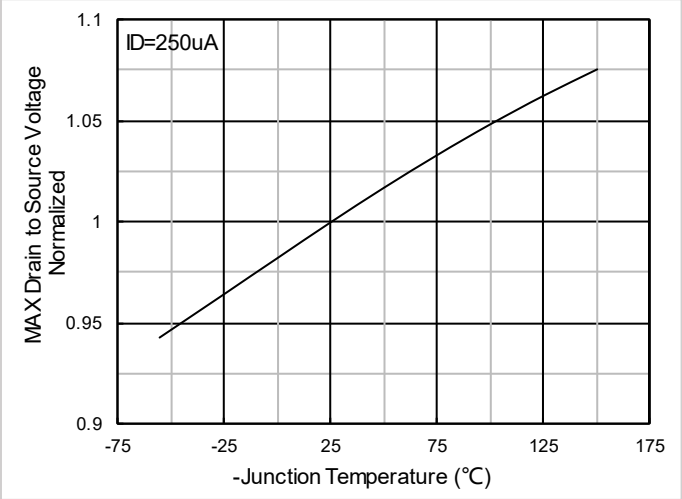


Figure 9. Normalized breakdown voltage

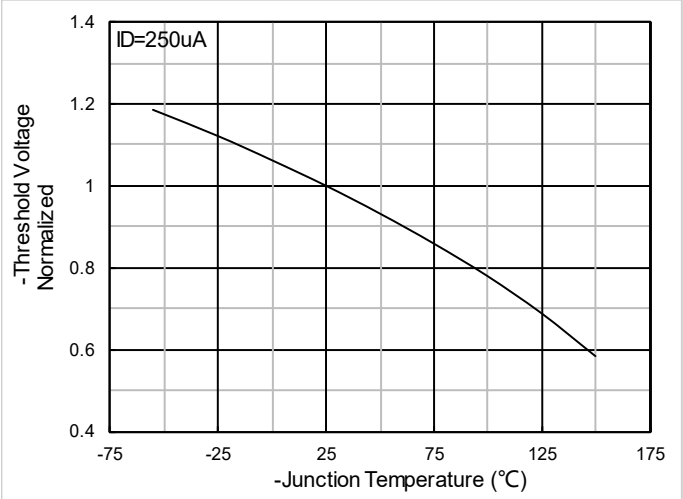


Figure 10. Normalized Threshold voltage

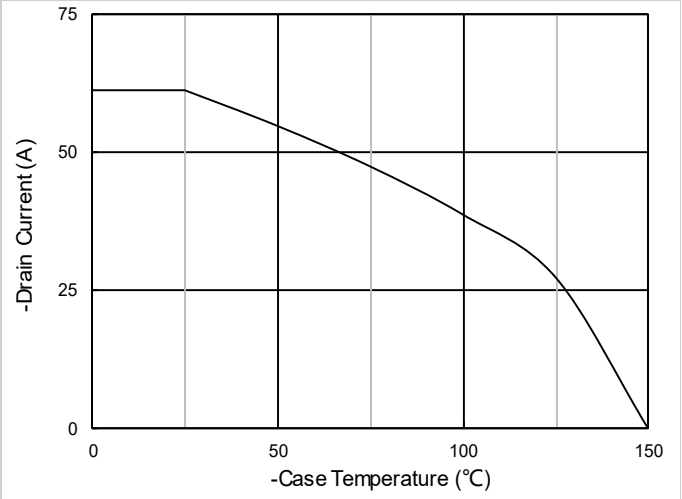


Figure 11. Current dissipation

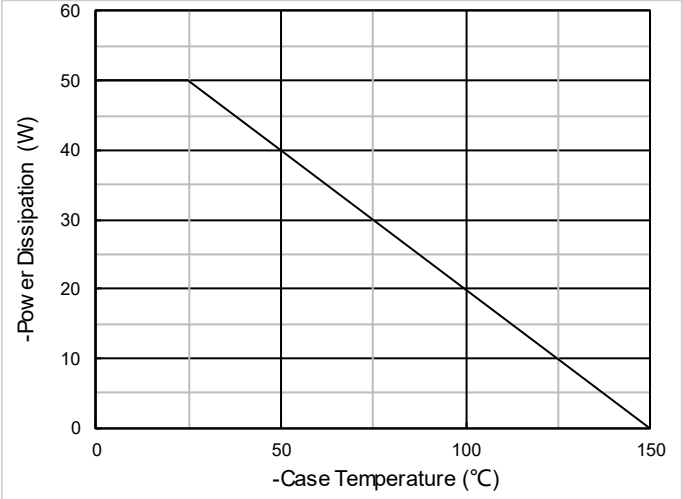


Figure 12. Power dissipation

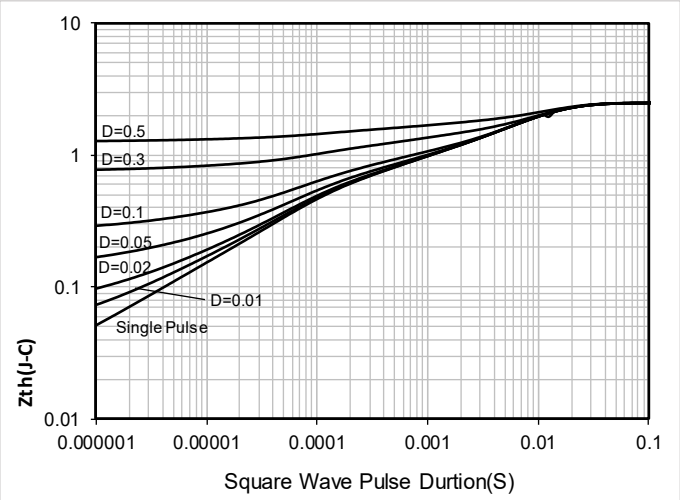


Figure 13. Maximum Transient Thermal Impedance

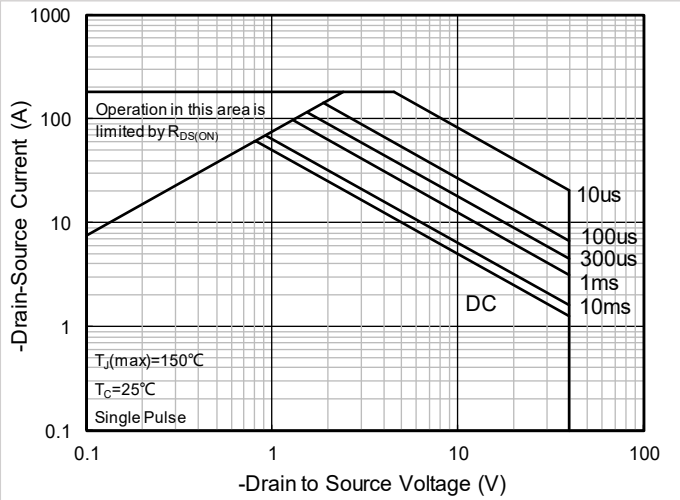
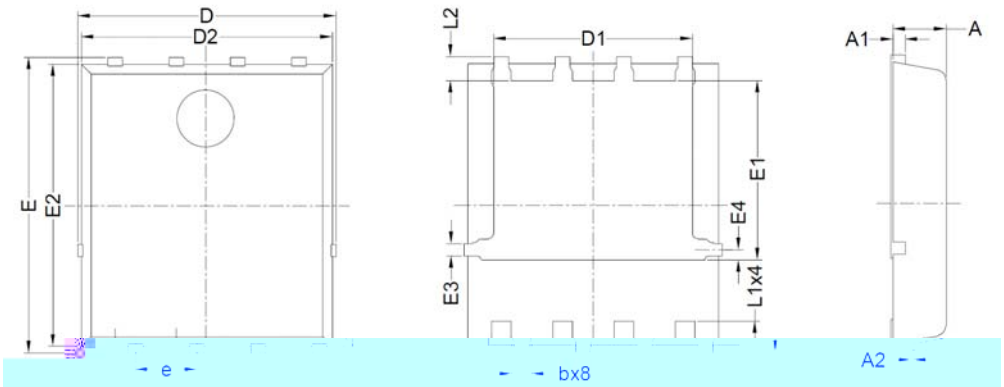
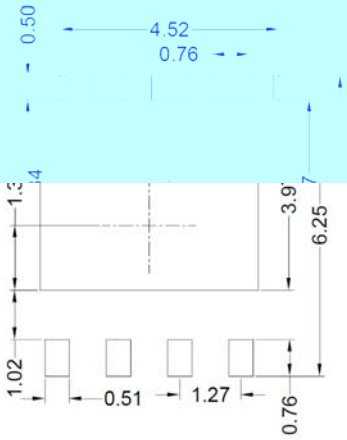


Figure 14. Safe Operation Area

■



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254 REF	
E4		0.21 REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	



Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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