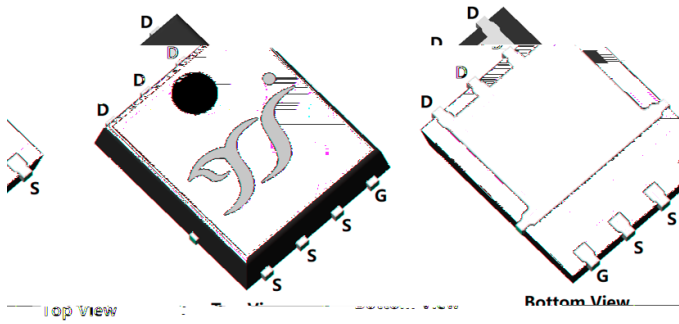


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 150V
- I_D 60A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) 19m Ω
- $R_{DS(ON)}$ (at $V_{GS}=6V$) 22m Ω

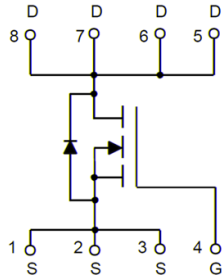
General Description

- Advanced Trench Cell Design
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

DFN5060-8L



PI

■ Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}	150	V
Gate-source Voltage	V_{GS}	± 25	V
Drain Current	I_D	$T_C=25^\circ C$	60
		$T_C=100^\circ C$	38
Pulsed Drain Current ^A	I_{DM}	120	A
Total Power Dissipation ^B	P_D	$T_C=25^\circ C$	125
		$T_C=100^\circ C$	50
Junction and Storage Temperature Range	T_J, T_{STG}	-55 +150	$^\circ C$

■ Thermal resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^C	$R_{\theta JA}$	50	60	$^\circ C/W$
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	0.8	1	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG60G15HJ	F1	YJG60G15HJ	5000	10000	100000	13" reel



YJG60G15HJ

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	150	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =150V, V _{GS} =0V	-	-	1	μA
		V _{DS} =150V, V _{GS} =0V, T _J =150°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±25V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	2	-	4	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A	-	13	19	mΩ
		V _{GS} =6V, I _D =10A	-	15	22	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V	-	-	1.3	V
Maximum Body-Diode Continuous Current	I _S		-	-	60	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =75V, V _{GS} =0V, f=1MHz	-	2100	-	pF
Output Capacitance	C _{oss}		-	160	-	
Reverse Transfer Capacitance	C _{rss}		-	5	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =75V, I _D =20A	-	25	-	nC
Gate-Source Charge	Q _{gs}		-	10	-	
Gate-Drain Charge	Q _{gd}		-	8	-	
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=100A/us	-	220	-	nC
Reverse Recovery Time	t _{rr}		-	86	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =75V, I _D =20A R _{GEN} =4.5Ω	-	15	-	ns
Turn-on Rise Time	t _r		-	34	-	
Turn-off Delay Time	t _{D(off)}		-	30	-	
Turn-off fall Time	t _f		-	26	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. P_d is based on max. junction temperature, using junction-case thermal resistance.

C. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in the still air environment with T_A=25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



Typical Electrical and Thermal Characteristics Diagrams

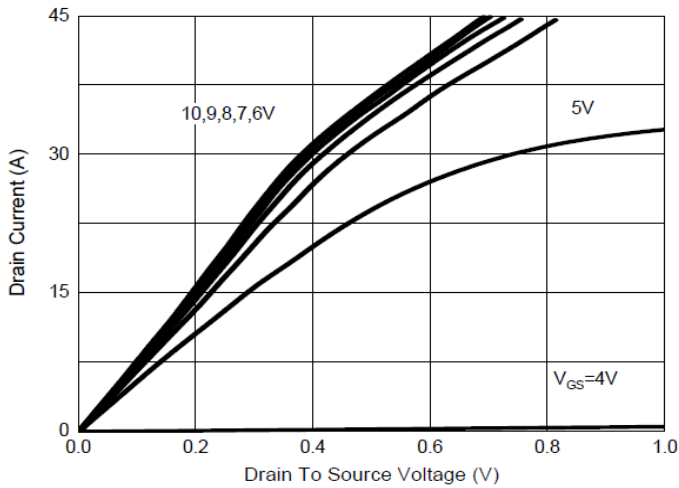


Figure 1. Output Characteristics

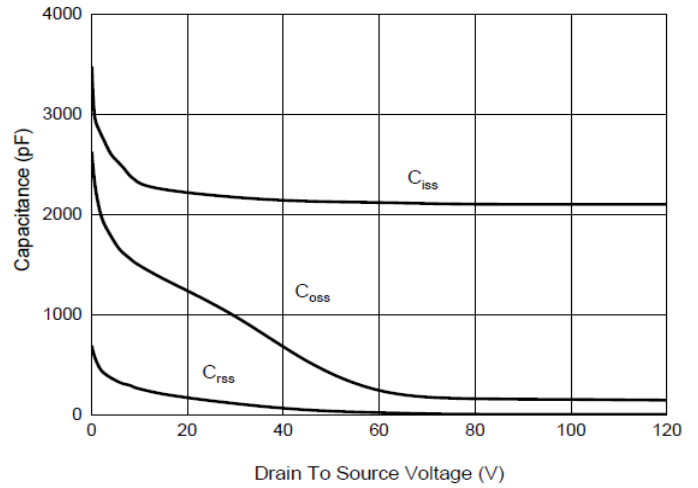


Figure 2. Capacitance Characteristics

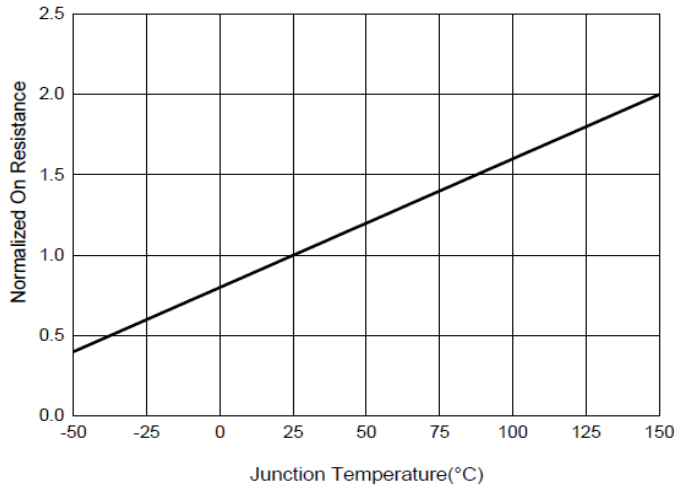


Figure 3. Normalized On-Resistance

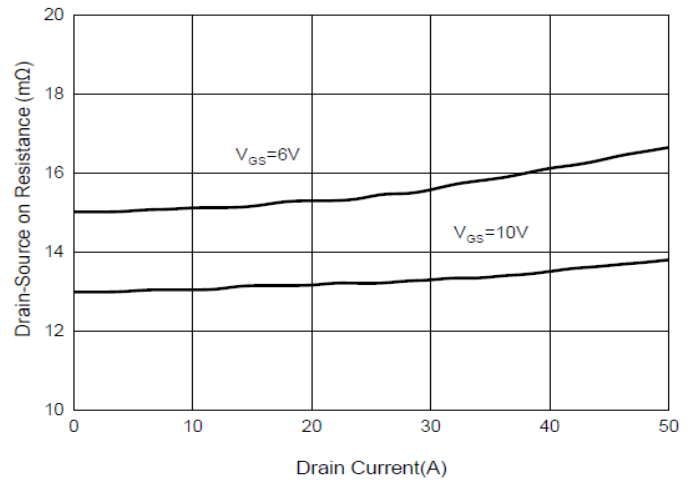


Figure 4. RDS(on) VS Drain Current

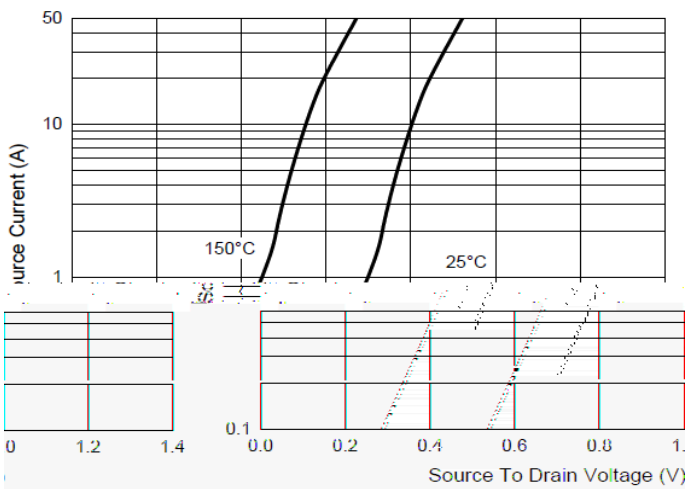


Figure 5. Forward characteristics of reverse diode

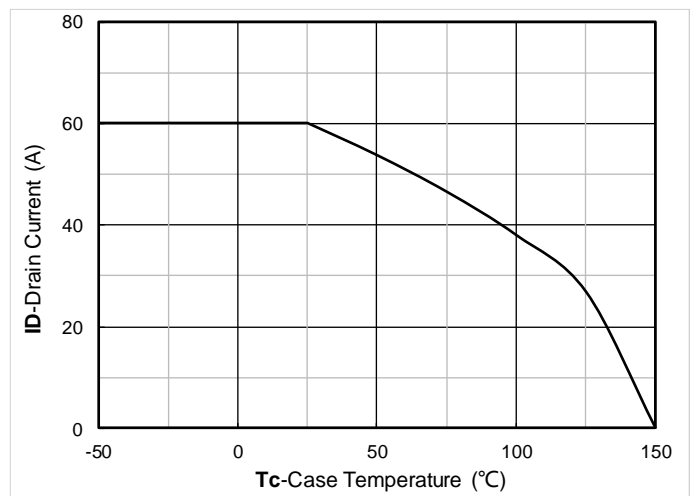


Figure 6. Power dissipation

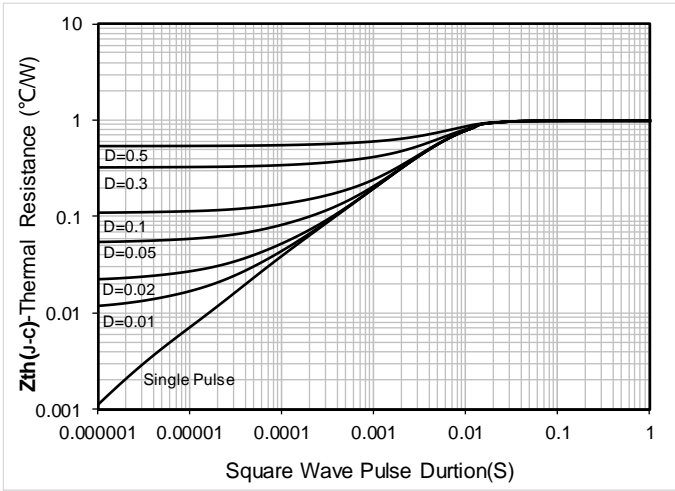


Figure 7. Maximum Transient Thermal Impedance

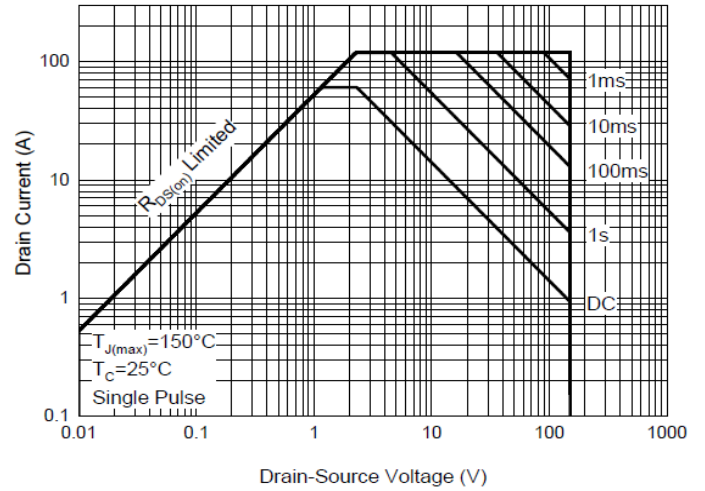


Figure 8. Safe Operation Area

■ Test Circuits & Waveforms

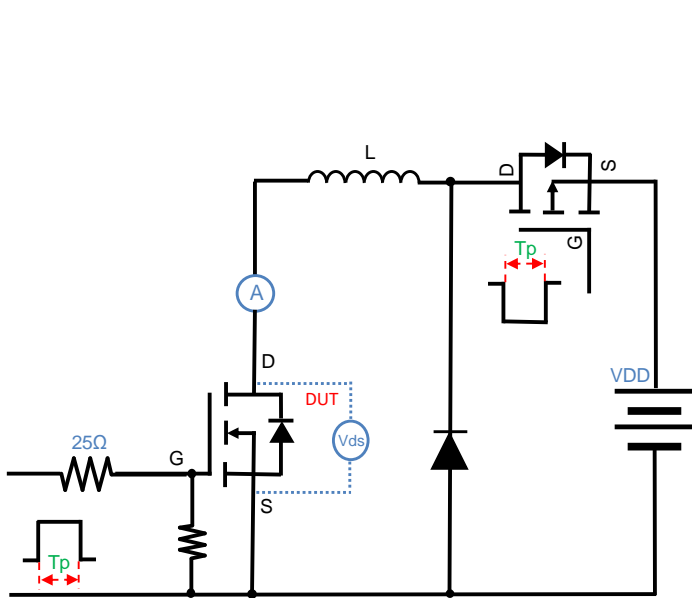
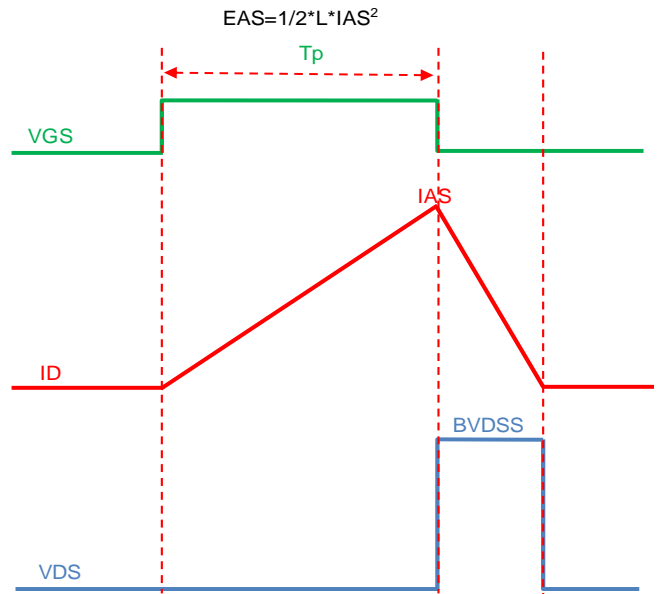


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



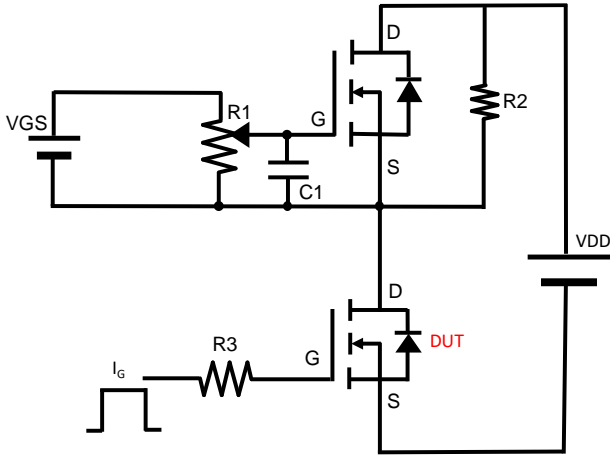


Figure B. Gate Charge Test Circuit & Waveform

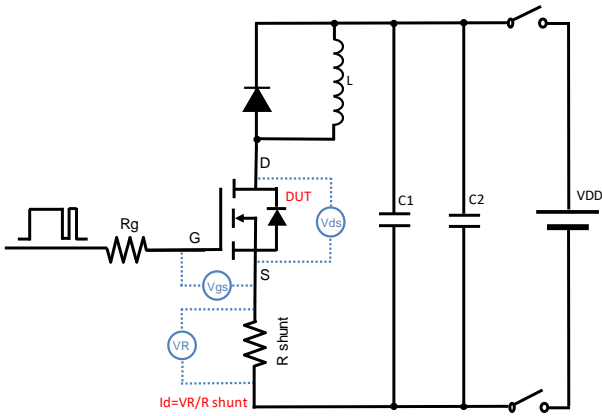


Figure C. Resistive Switching Test Circuit & Waveform

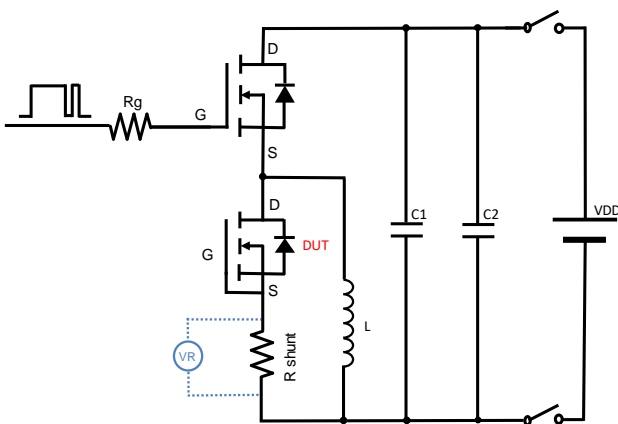
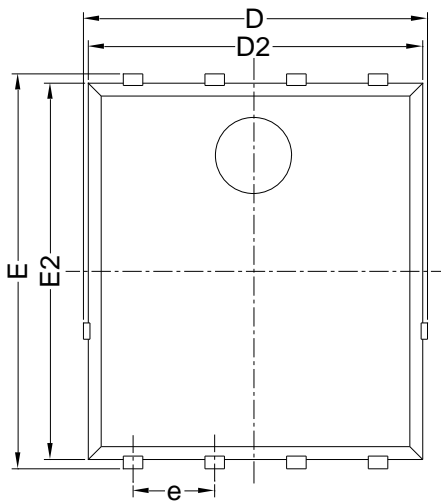


Figure D. Diode Recovery Test Circuit & Waveform

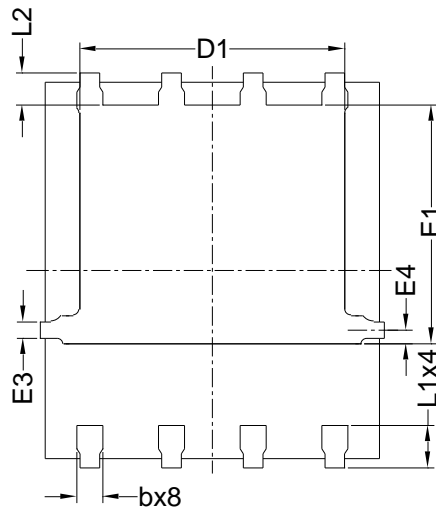


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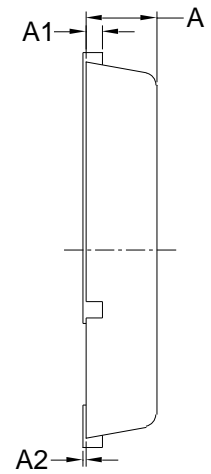
■ PDFN5060-8L-B-1.1MM Package information



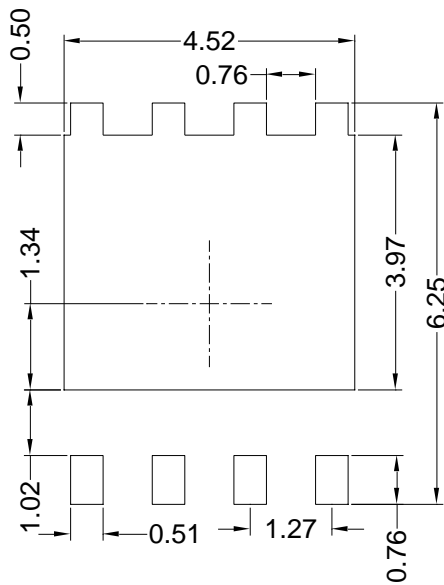
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



YJG60G15HJ

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