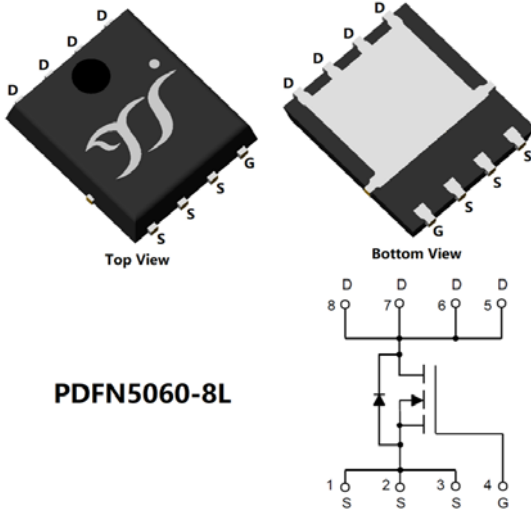


N-Channel Enhancement Mode Field Effect Transistor



PDFN5060-8L

Product Summary

- V_{DS} 100V
- I_D 60A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) 12 mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) 15 mohm
- 100% UIS Tested
- 100% ∇V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- High Frequency Switching
- Synchronous Rectification
- 12V, 24V and 48V Automotive systems

■ Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ C$	I_D	60	A
	$T_C=125^\circ C$		28	
Pulsed Drain Current ^A		I_{DM}	240	A
Avalanche energy ^B		EAS	200	mJ
Total Power Dissipation ^C	$T_C=25^\circ C$	P_D	78	W
	$T_C=125^\circ C$		15	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	$^\circ C$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	$R_{\theta JA}$	92	100	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.3	1.6	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG60G10BQ	F1	YJG60G10B	5000	10000	100000	13" reel



YJG60G10BQ

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1	1.8	2.8	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		8.0	12	mΩ
		V _{GS} =4.5V, I _D =20A		9.5	15	mΩ
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V			1.3	V
Maximum Body-Diode Continuous Current	I _S				60	A
Gate resistance	R _G	f=1MHz, Open drain		1		Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHZ		2500		pF
Output Capacitance	C _{oss}			1385		
Reverse Transfer Capacitance	C _{rss}			45		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =13V, V _{DS} =50V, I _D =30A		36.0		nC
Gate-Source Charge	Q _{gs}			6.3		
Gate-Drain Charge	Q _{gd}			13.8		
Reverse Recovery Charge	Q _{rr}	V _{GS} =0V, di/dt=100A/us, I _S =30A		280		nC
Reverse Recovery Time	t _{rr}			10.5		
Turn-on Delay Time	t _{D(on)}	V _{GS} =13V, V _{DD} =50V, I _{DS} =30A R _{GEN} =2.3Ω		12		ns
Turn-on Rise Time	t _r			62		
Turn-off Delay Time	t _{D(off)}			24.5		
Turn-off fall Time	t _f			3.5		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V_{DD}=50V, R_G=25Ω, L=1mH, I_{AS}=20A

C. P_d is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on the minimum recommend pad size, in the still air environment with T_A =25 . The maximum allowed junction temperature of 150 . The value in any given application depends on the user's specific board design.



YJG60G10BQ

■ Typical Performance Characteristics

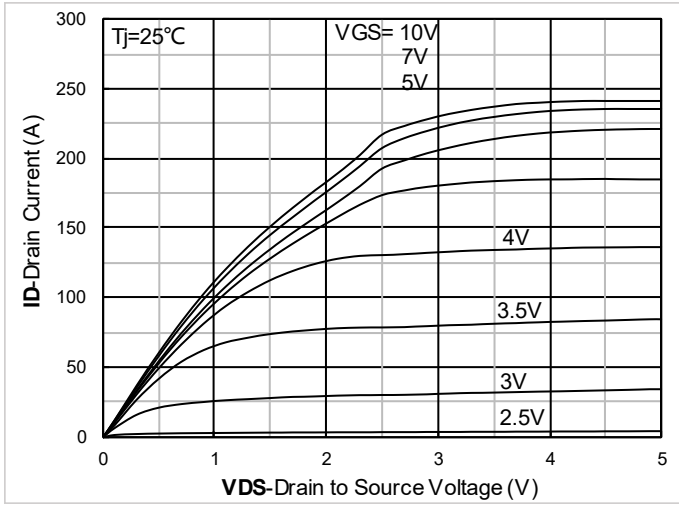


Figure 1. Output Characteristics

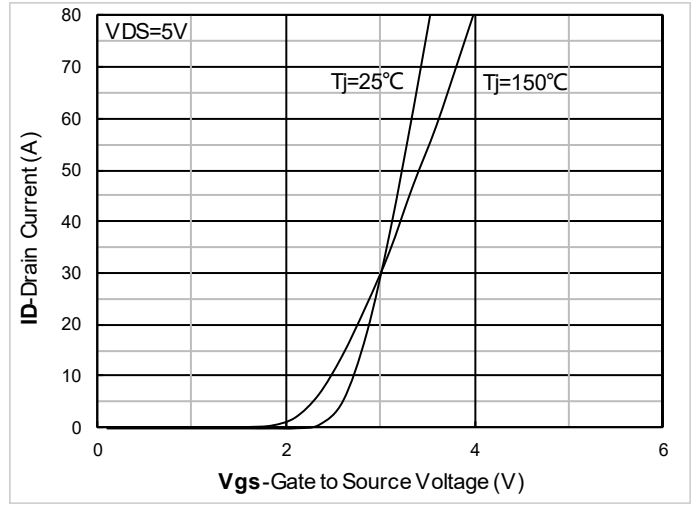


Figure 2. Transfer Characteristics

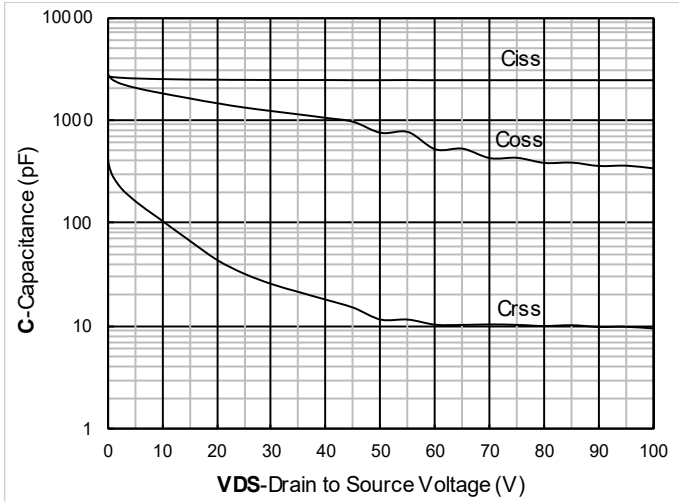


Figure 3. Capacitance Characteristics

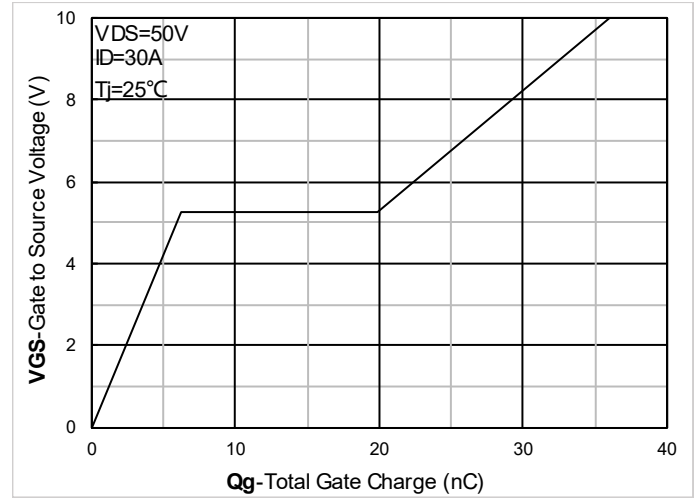


Figure 4. Gate Charge

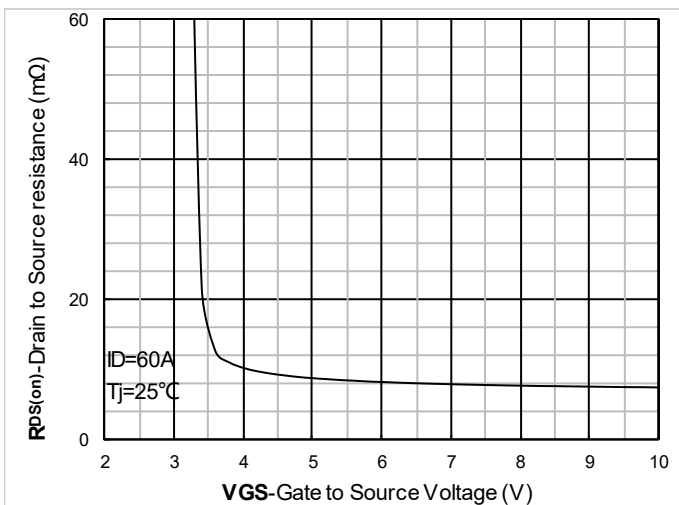


Figure 5. On-Resistance vs Gate to Source Voltage

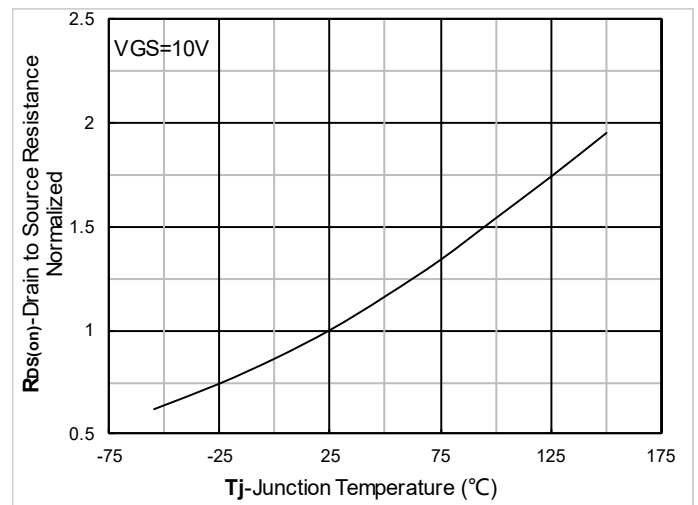


Figure 6. Normalized On-Resistance



YJG60G10BQ

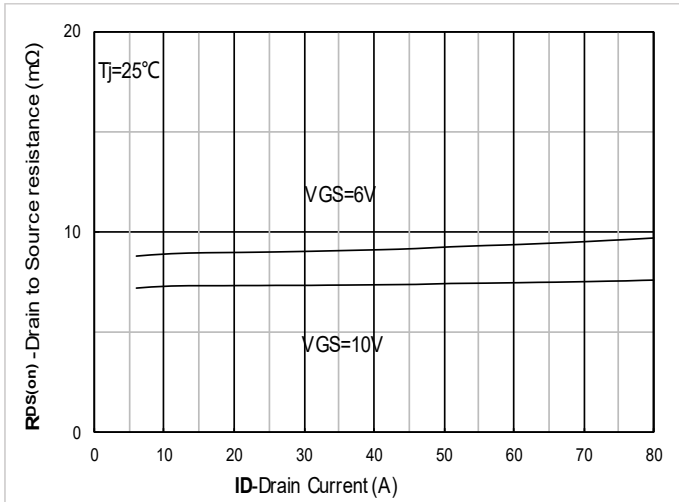


Figure 7. $R_{DS(on)}$ VS Drain Current

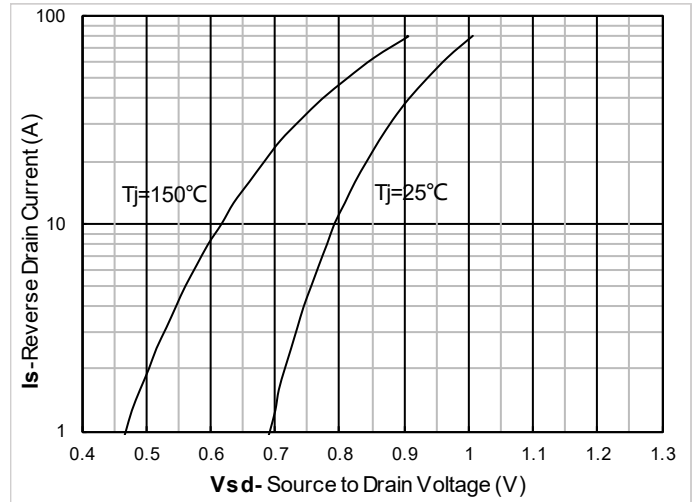


Figure 8. Forward characteristics of reverse diode

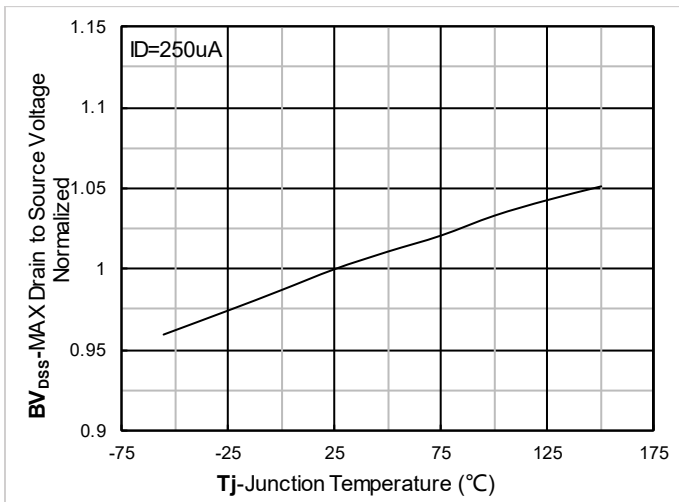


Figure 9. Normalized breakdown voltage

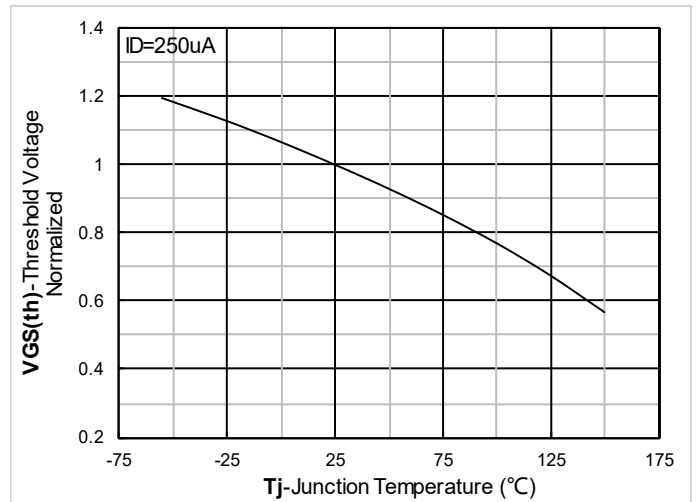


Figure 10. Normalized Threshold voltage

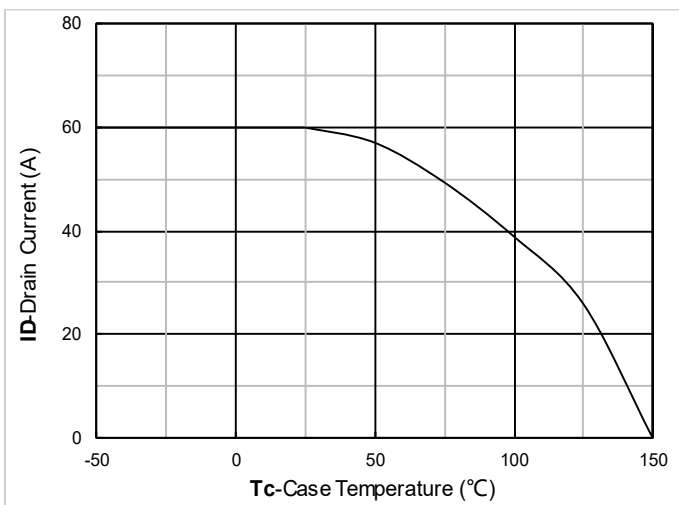


Figure 11. Current dissipation

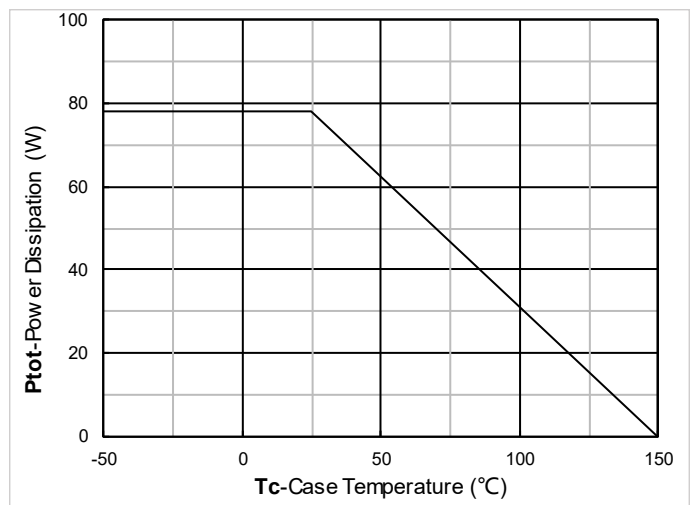


Figure 12. Power dissipation



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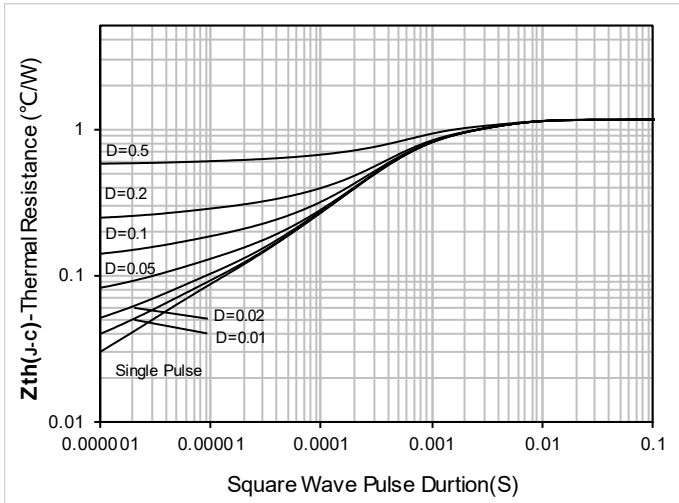


Figure 13. Maximum Transient Thermal Impedance

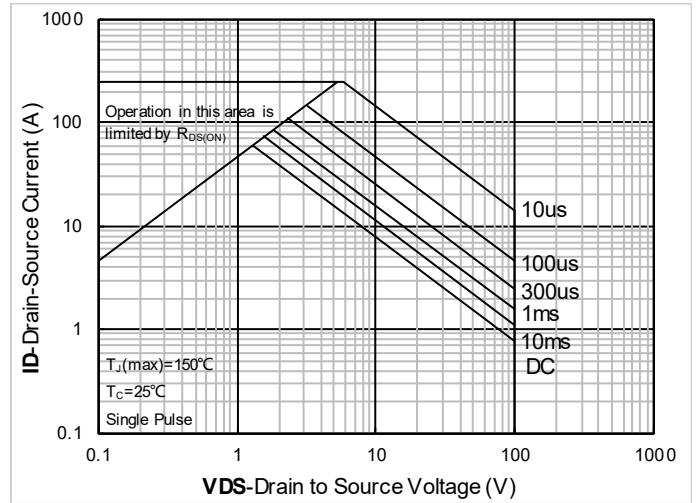


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

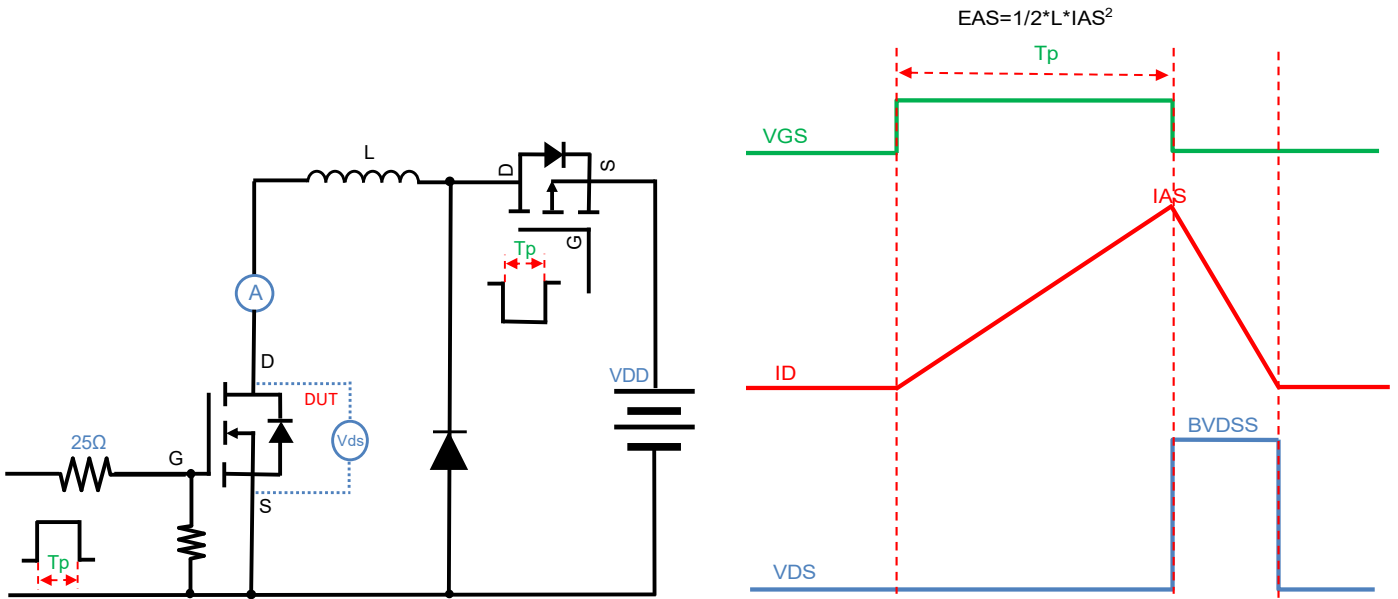


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

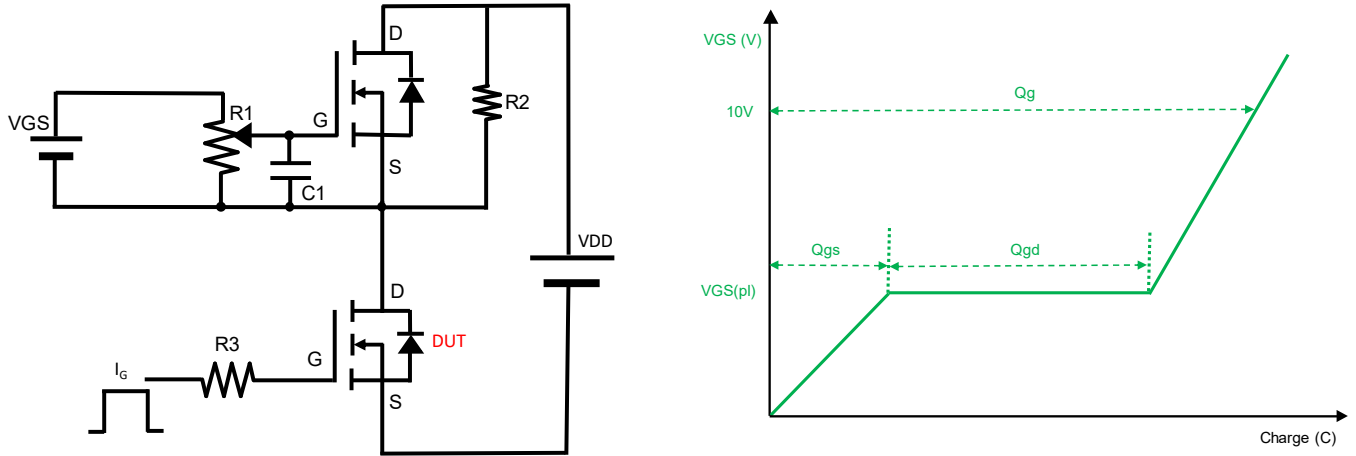


Figure B. Gate Charge Test Circuit & Waveform

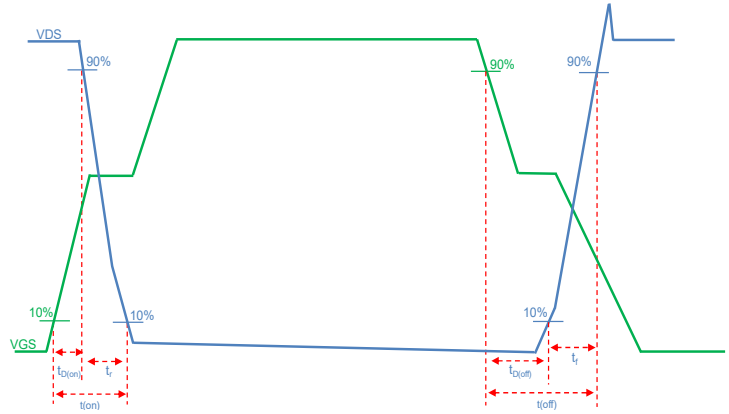
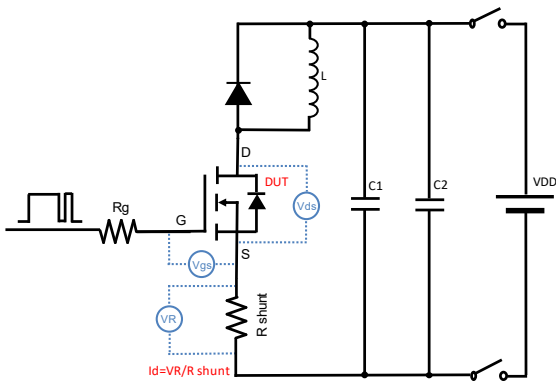


Figure C. Resistive Switching Test Circuit & Waveform

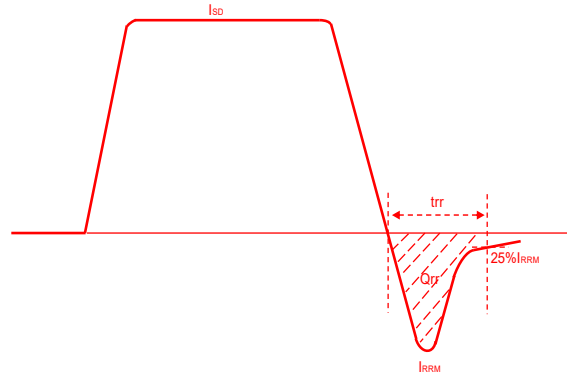
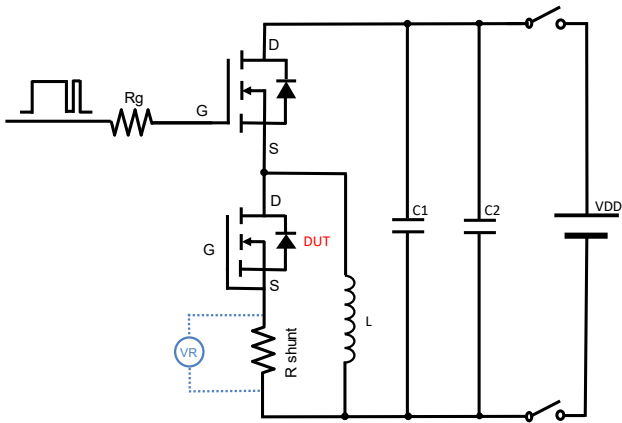
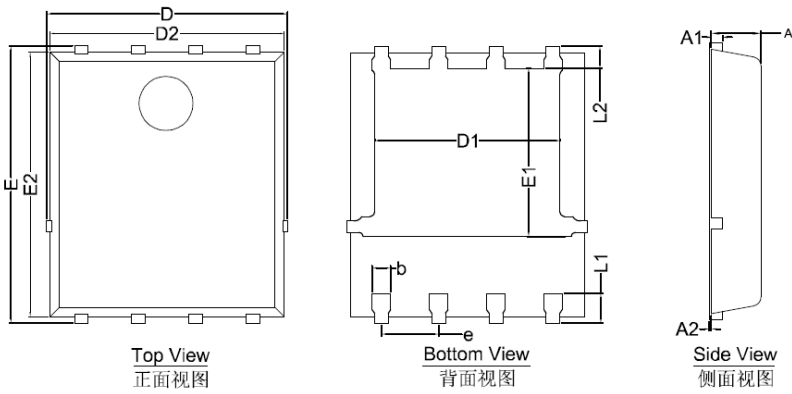


Figure D. Diode Recovery Test Circuit & Waveform

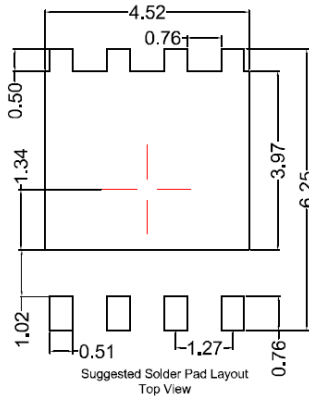


YJG60G10BQ

■ PDFN5060 Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		



Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.10\text{mm}$.
 3. The pad layout is for reference purposes only.



YJG60G10BQ

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