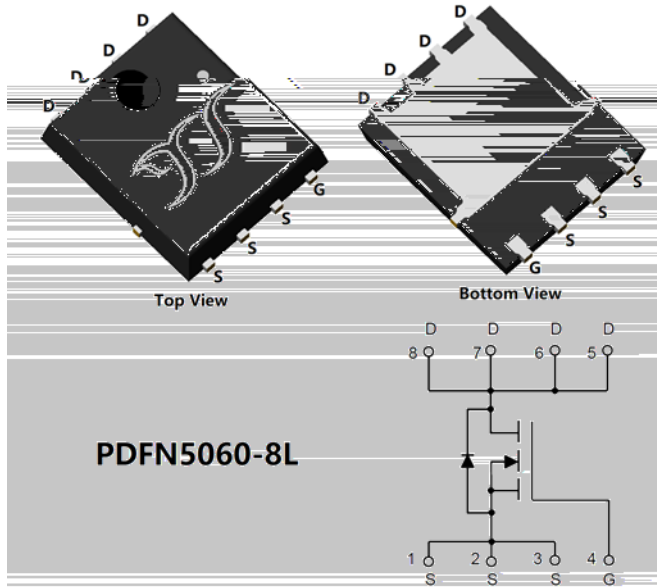


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

V_{DS}	100V
I_D	60A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	8.6 mohm
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	13 mohm
100% EAS Tested	
100% V_{DS} Tested	

General Description

Split gate trench MOSFET technology
 Excellent package for heat dissipation
 High density cell design for low $R_{DS(ON)}$
 Moisture Sensitivity Level 1
 Epoxy Meets UL 94 V-0 Flammability Rating
 Halogen Free

Applications

High Frequency Switching
 Synchronous Rectification

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	20	V
Drain Current	$T_C=25$	I_D	60	A
	$T_C=100$		38	
Pulsed Drain Current ^A		I_{DM}	240	A
Avalanche energy ^B		EAS	200	mJ
Total Power Dissipation ^C	$T_C=25$	P_D	88	W
	$T_C=100$		35.2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	t 10S	R	15	20	/W
	Steady-State		40	50	
Thermal Resistance Junction-to-Case	Steady-State	R	1.15	1.42	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG60G10B	F1	YJG60G10B	5000	10000	100000	13 reel



YJG60G10B

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = 20V, V _{DS} =0V			100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250	1.3	1.8	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		7.5	8.6	m
		V _{GS} =4.5V, I _D =20A		9.5	13	m
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V			1.3	V
Maximum Body-Diode Continuous Current	I _S				60	A
Gate resistance	R _G	f=1MHz		0.68		
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHZ		2270		pF
Output Capacitance	C _{oss}			797		
Reverse Transfer Capacitance	C _{rss}			36		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =25A		32		nC
Gate-Source Charge	Q _{gs}			11.1		
Gate-Drain Charge	Q _{gd}			4.78		
Reverse Recovery Charge	Q _{rr}	I _r =20A, di/dt=100A/us		64		
Reverse Recovery Time	t _{rr}			51.5		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _{DS} =25A R _{GEN} =2.2		9.3		ns
Turn-on Rise Time	t _r			34.8		
Turn-off Delay Time	t _{D(off)}			24.6		
Turn-off fall Time	t _f			71		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V_{DD}=50V, R_G 1mH, I_{AS}=20A

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. -4 board with 2oz. Copper, in a still air environment with TA =25 C. The C. The value in any given

application depends on the user's specific board design.



Typical Performance Characteristics

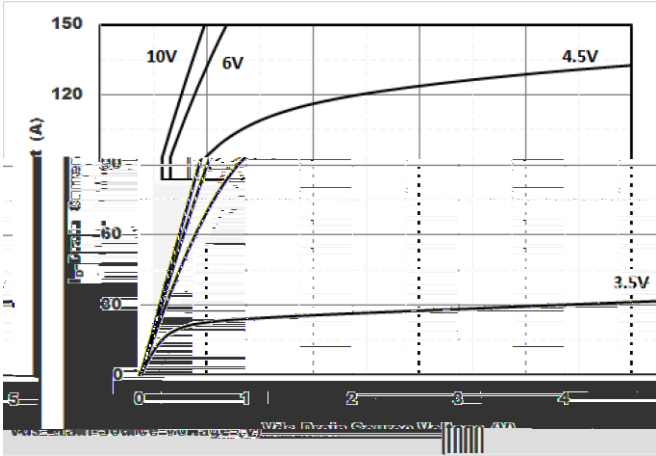


Figure1. Output Characteristics

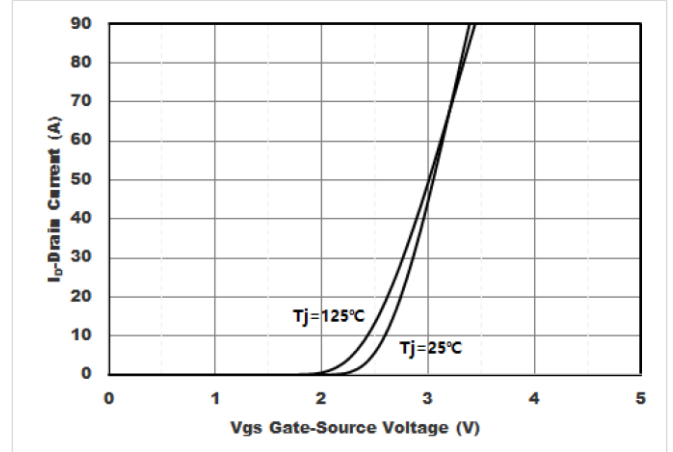


Figure2. Transfer Characteristics

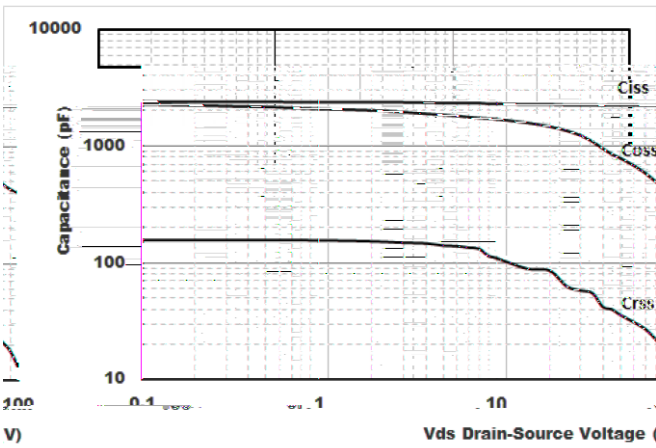


Figure3. Capacitance Characteristics

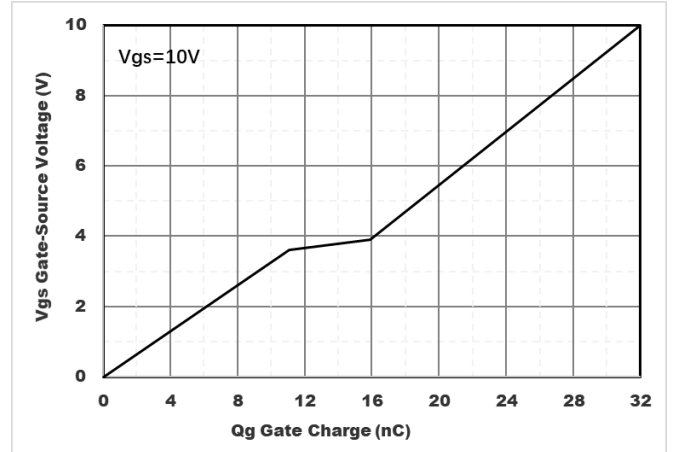


Figure4. Gate Charge

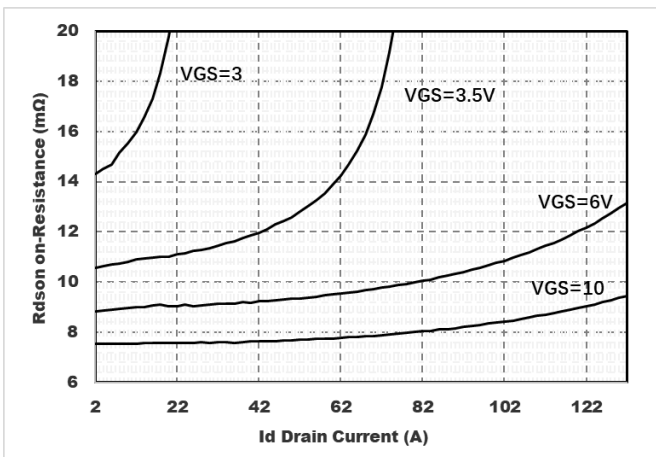


Figure5. : On-Resistance vs. Gate to Source Voltage

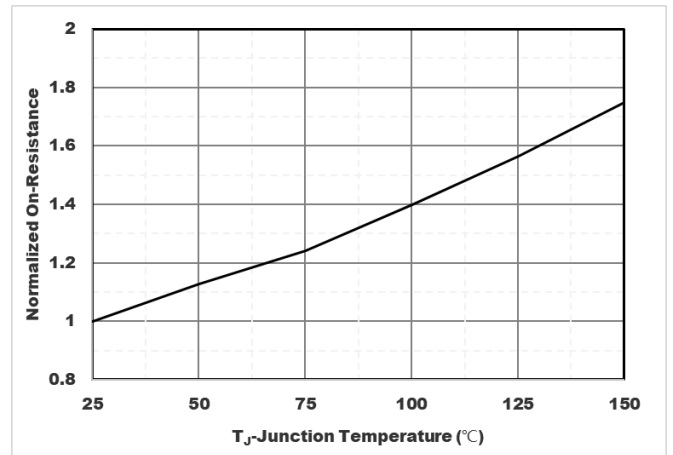


Figure6. Normalized On-Resistance



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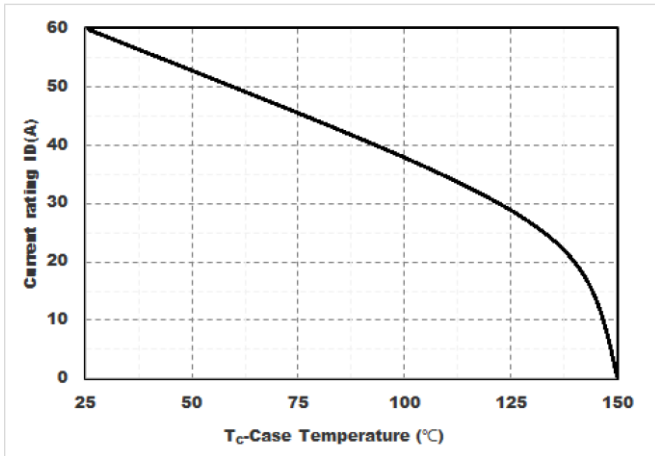


Figure7. Drain current

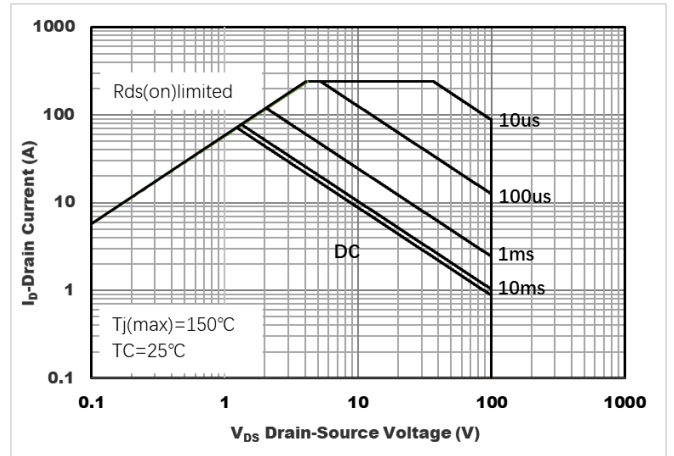


Figure8.Safe Operation Area

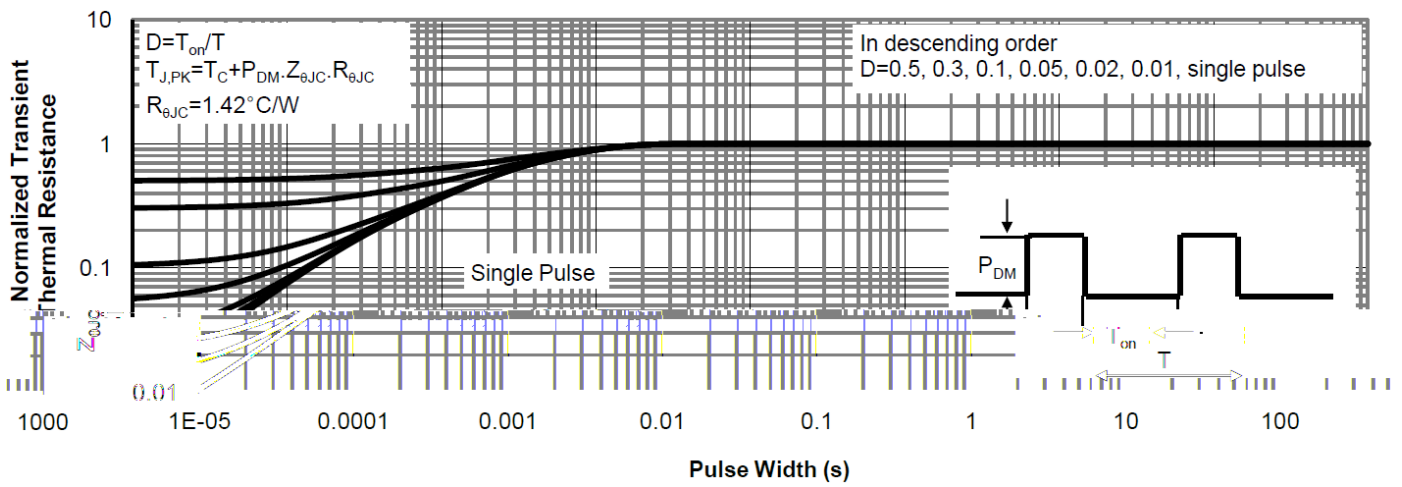
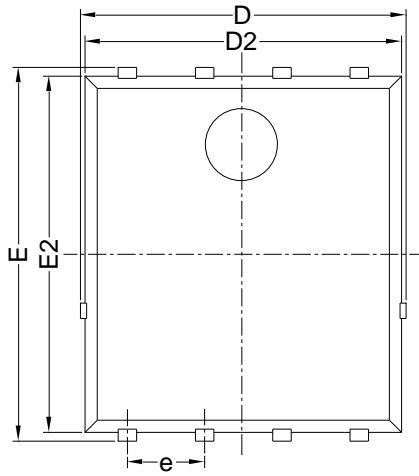


Figure9.Normalized Maximum Transient thermal impedance

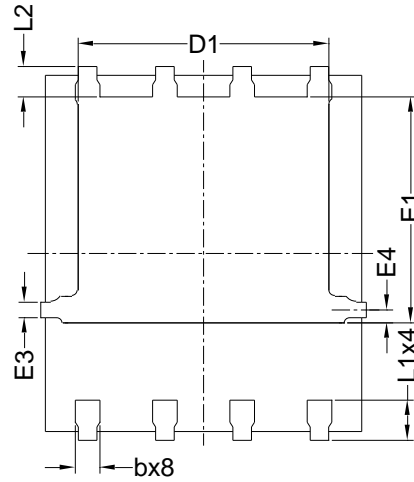


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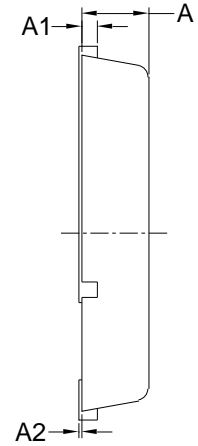
PDFN5060-8L-B-1.1MM Package information



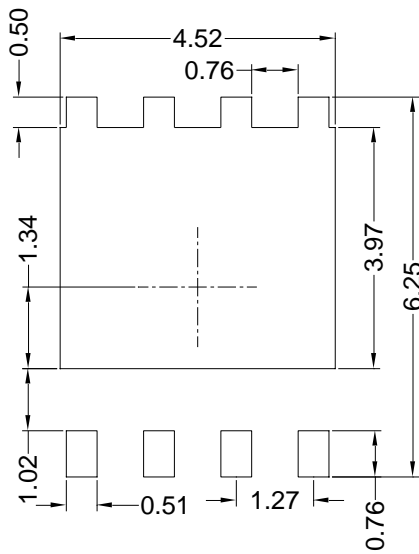
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



YJG60G10B

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