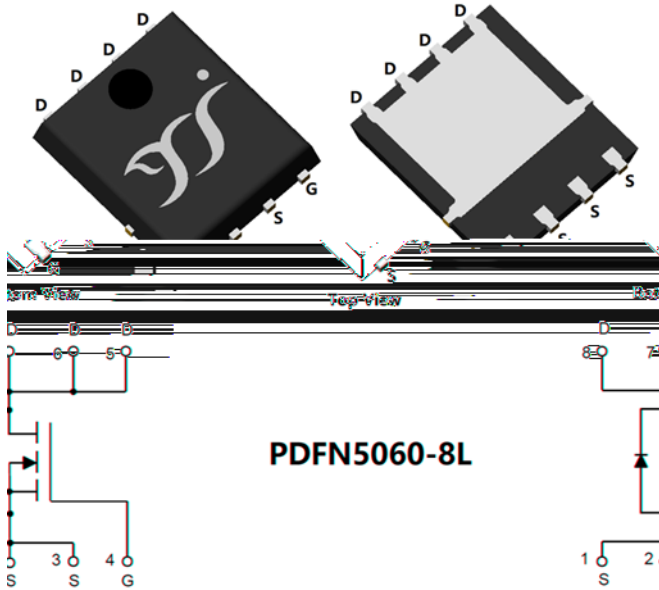


## N-Channel Enhancement Mode Field Effect Transistor



PDFN5060-8L

### Product Summary

$V_{DS}$	30V
$I_D$	50A
$r_{DS(ON)}$ (at $V_{GS}=10V$ )	<6.0mohm
$R_{DS(ON)}$ (at $V_{GS}=4.5V$ )	<8.0mohm
100% EAS Tested	
100% $\nabla V_{DS}$ Tested	

### General Description

PYNS Zb P 7A 8: 10 P NSYZWRd  
 Excellent package for heat dissipation  
 High density cell design for low  $R_{DS(ON)}$   
 Moisture Sensitivity Level 1  
 Epoxy Meets UL 94 V-0 Flammability Rating  
 Halogen Free

### Applications

High current load applications  
 Load switch  
 Hard switched and high frequency circuits  
 Uninterruptible power supply

### Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	30	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current	$I_D$	$T_C=25^\circ C$	50
		$T_C=100^\circ C$	32
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	190	A
Total Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ C$	45
		$T_C=100^\circ C$	18
Total Power Dissipation @ $T_A=25^\circ C$ <sup>C</sup>	$P_D$	6.0	W
Single Pulse Avalanche Energy <sup>D</sup>	$E_{AS}$	98	mJ
Thermal Resistance Junction-to-Case	$R_{JC}$	2.8	$^\circ C/W$
Thermal Resistance Junction-to-Ambient	$R_{JA}$	21	$^\circ C/W$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ C$

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG50N03B	F1	YJG50N03B	5000	10000	100000	13 reel



# YJG50N03B

## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250 ,	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V			1	,
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20V, V <sub>DS</sub> =0V			± 100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250 ,	1	1.5	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		3.9	6.0	X
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =15A		6.0	8.0	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V		0.85	1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				80	A
Gate Resistance	R <sub>g</sub>	f =1 MHz		2.3		Ω
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHZ		2191		pF
Output Capacitance	C <sub>oss</sub>			300		
Reverse Transfer Capacitance	C <sub>rss</sub>			247		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		46.3		nC
Gate-Source Charge	Q <sub>gs</sub>			8.8		
Gate-Drain Charge	Q <sub>gd</sub>			9.2		
Reverse Recovery Chrage	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=100A/us		1.6		ns
Reverse Recovery Time	t <sub>rr</sub>			11		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =15V, R <sub>L</sub> =0.75 R <sub>GEN</sub> =3		11		ns
Turn-on Rise Time	t <sub>r</sub>			80		
Turn-off Delay Time	t <sub>D(off)</sub>			39		
Turn-off fall Time	t <sub>f</sub>			92		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. The value of R<sub>JA</sub> is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25°C.

D. T<sub>J</sub>=25°C, V<sub>DD</sub>=25V, V<sub>G</sub>=10V, L=1.0mH, I<sub>AS</sub>=14A.



## Typical Performance Characteristics

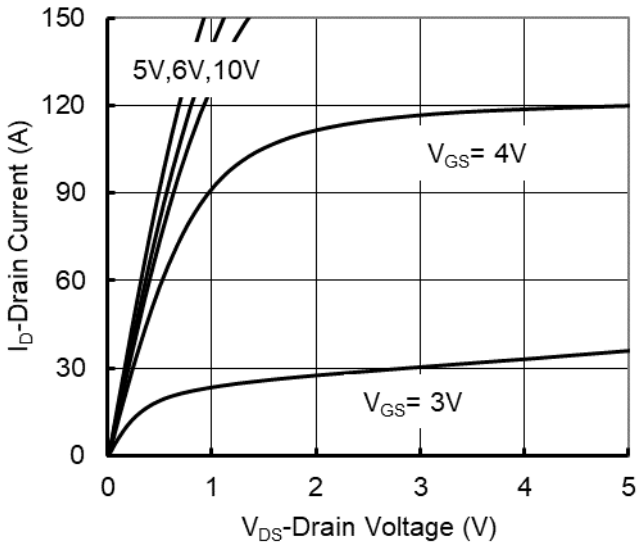


Figure 1. Output Characteristics

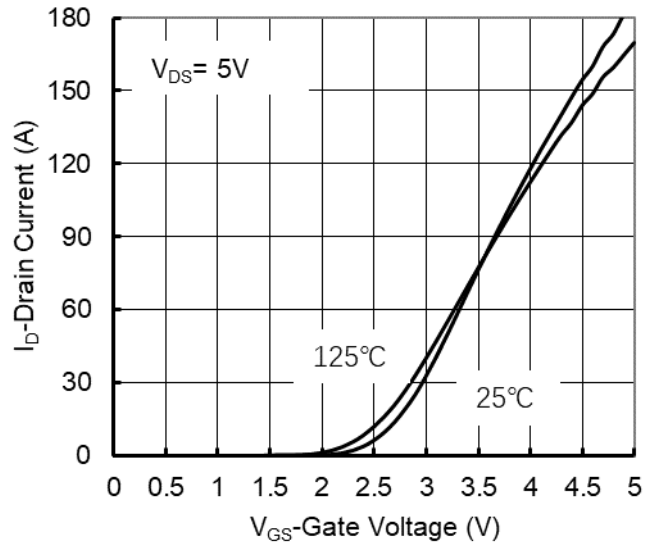


Figure 2. Transfer Characteristics

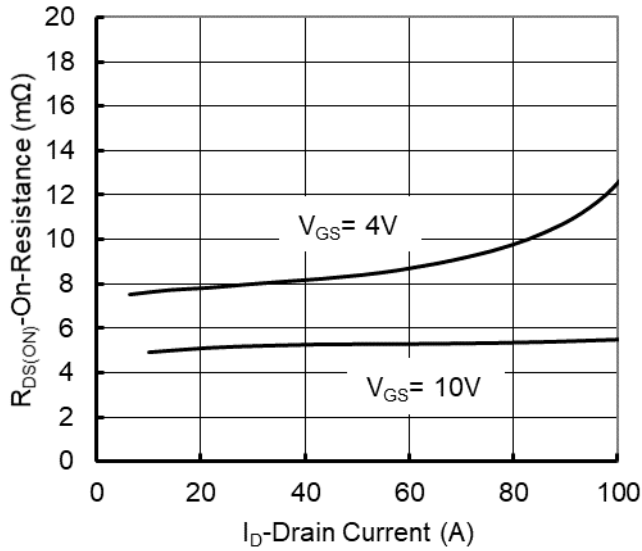


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

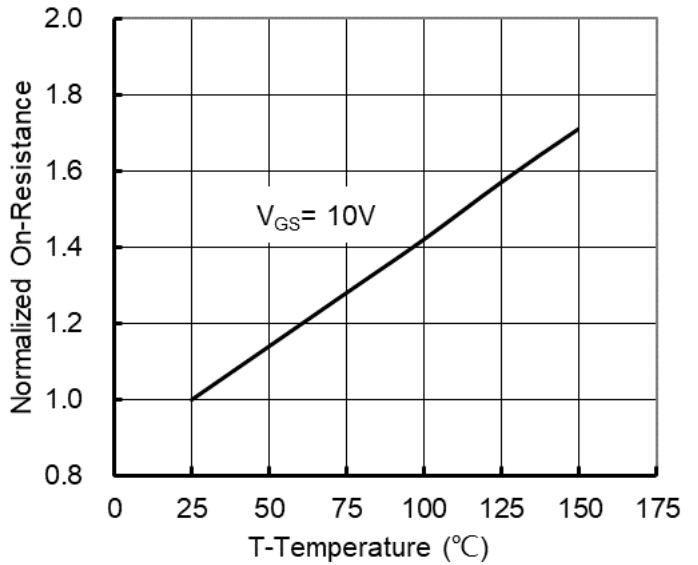


Figure 4. On-Resistance vs. Junction Temperature

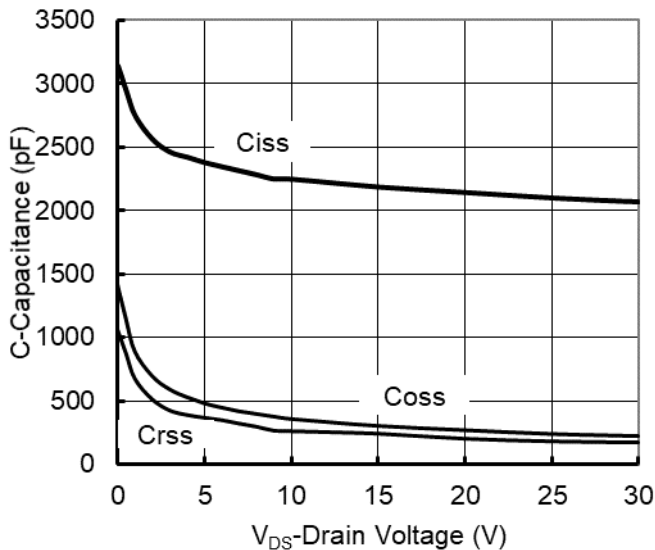


Figure 5. Capacitance Characteristics

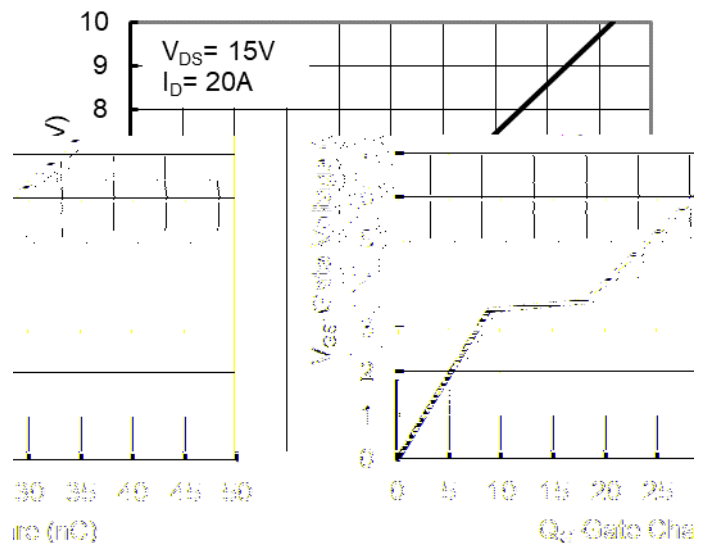


Figure 6. Gate Charge



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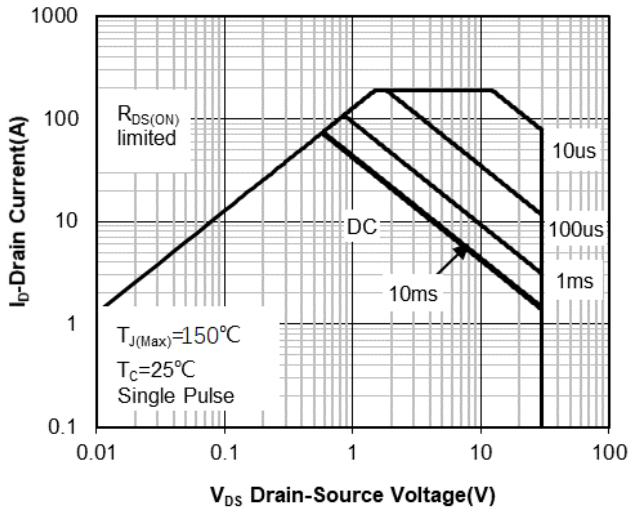


Figure 7. Safe Operation Area

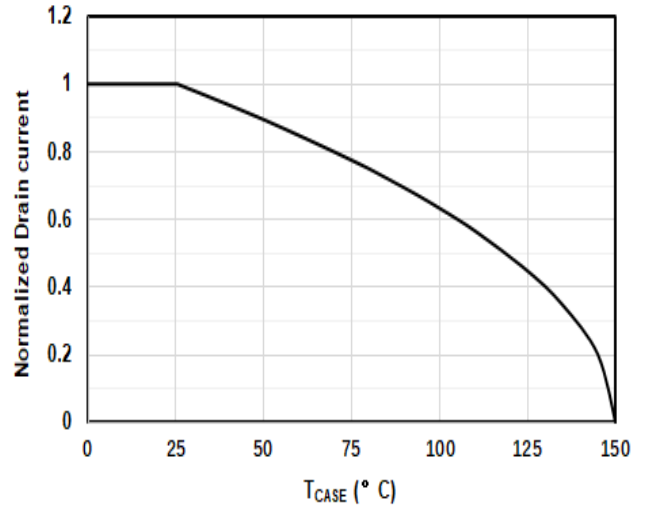


Figure 8. Maximum Continuous Drain Current vs Case Temperature

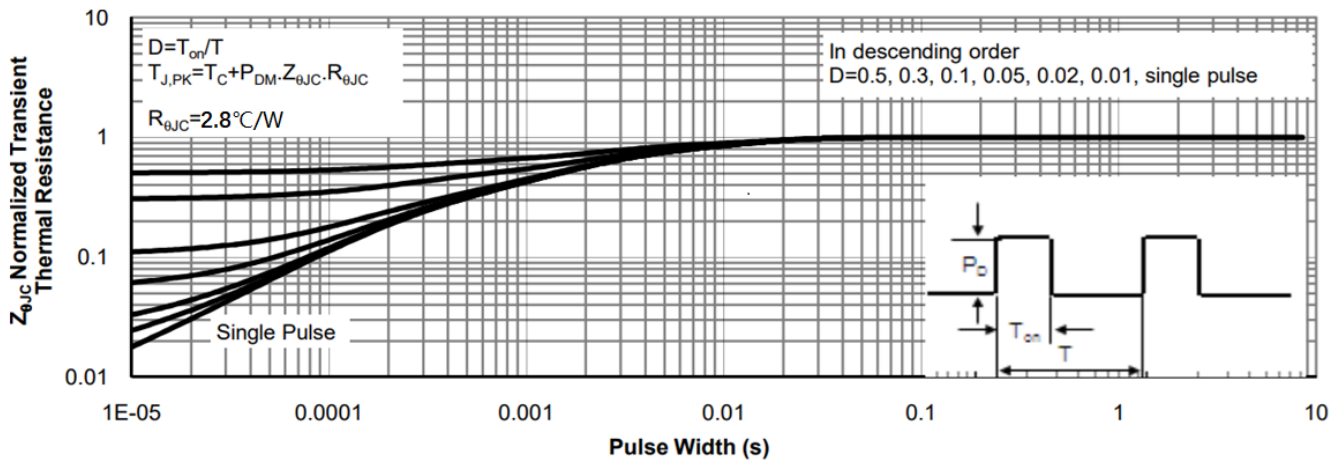
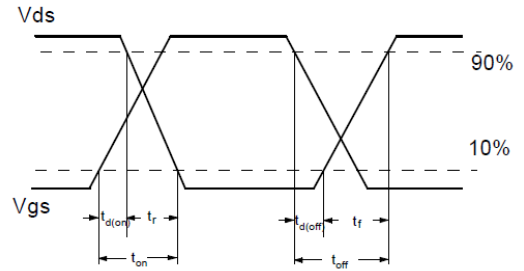
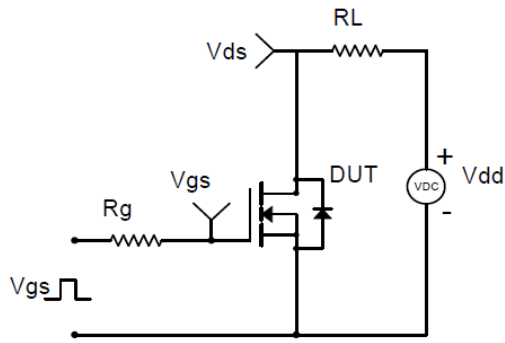
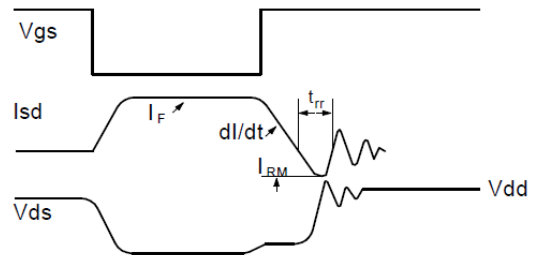
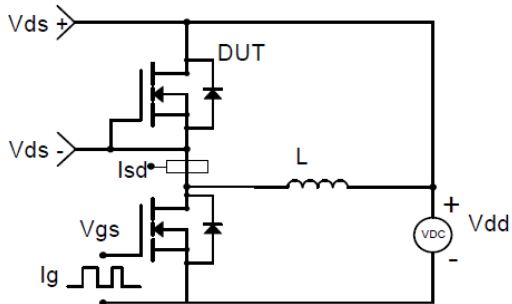


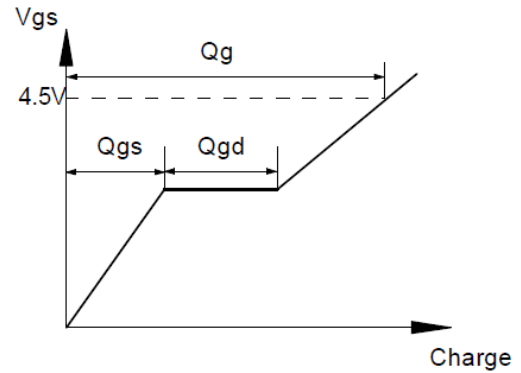
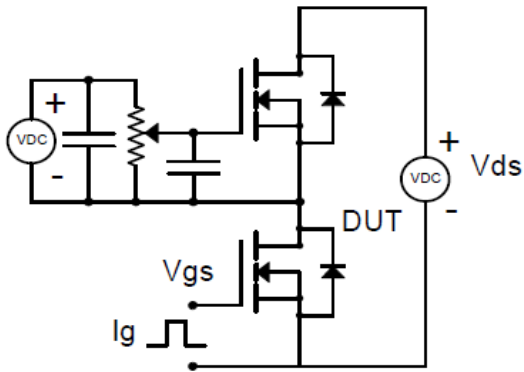
Figure 9. Normalized Maximum Transient Thermal Impedance



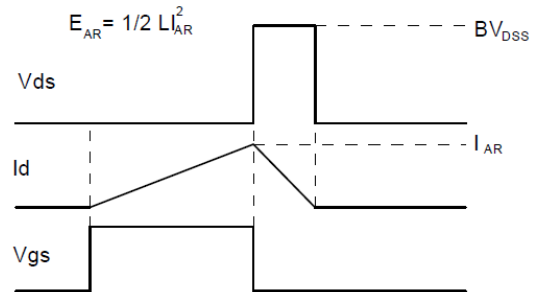
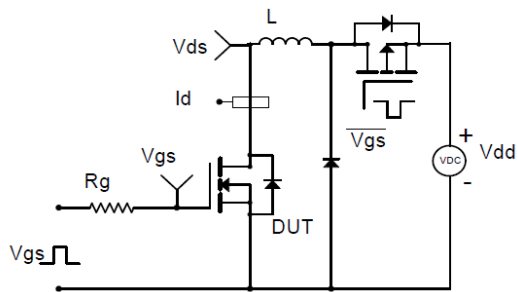
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

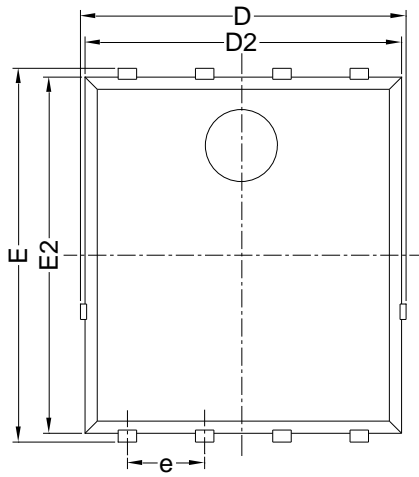


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

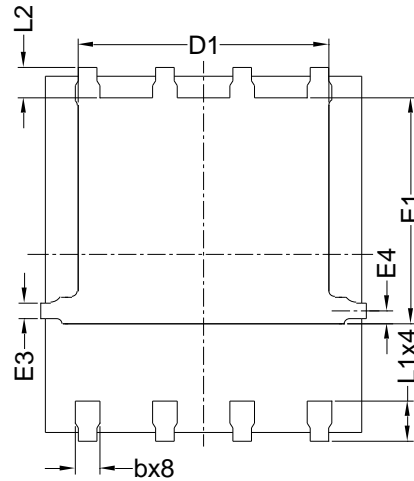


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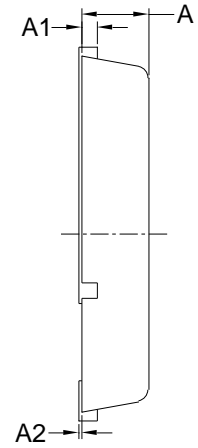
## PDFN5060-8L-B-1.1MM Package Information



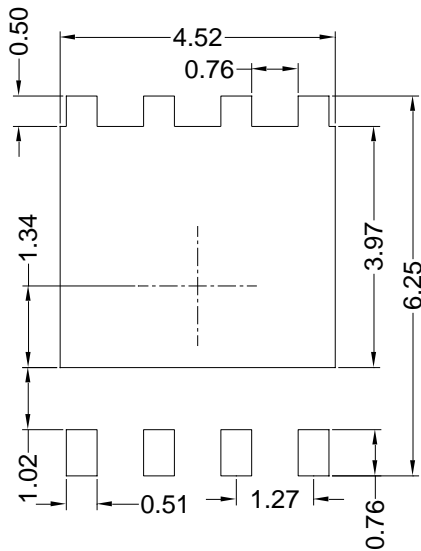
Top View  
正面视图



Bottom View  
背面视图



Side View  
侧面视图



Suggested Solder Pad Layout  
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.



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