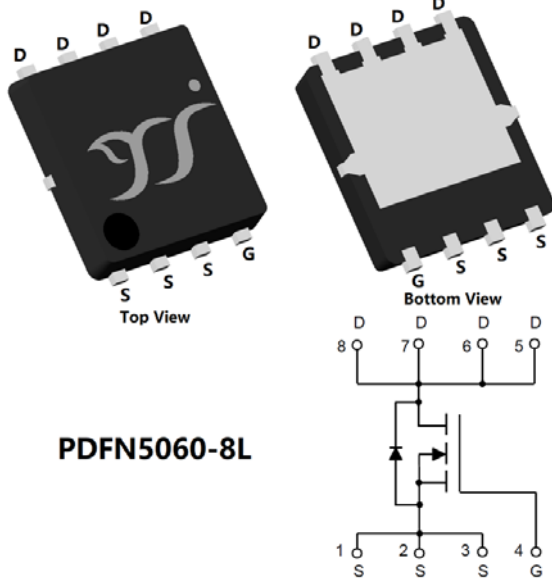


## N-Channel Enhancement Mode Field Effect Transistor



PDFN5060-8L

### Product Summary

- $V_{DS}$  40V
- $I_D$  320A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ ) 1.1m $\Omega$
- 100% EAS Tested
- 100%  $V_{DS}$  Tested

### General Description

- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Part no. with suffix "Q" means AEC-Q101 qualified

### Applications

- Power switching application
- Uninterruptible power supply
- DC-DC converter

### ■ Absolute Maximum Ratings ( $T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	40	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_C=25^\circ C$	$I_D$	320	A
	$T_C=100^\circ C$		225	
	$T_A=25^\circ C$		50	
	$T_A=100^\circ C$		36	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	900	A
Avalanche energy <sup>B</sup>		EAS	540	mJ
Total Power Dissipation <sup>C</sup>	$T_C=25^\circ C$	$P_D$	192	W
	$T_C=100^\circ C$		96	
	$T_A=25^\circ C$		5	
	$T_A=100^\circ C$		2.5	
Thermal Resistance Junction-to-Case <sup>D</sup>		$R_{\theta JC}$	0.78	$^\circ C/W$
Thermal Resistance Junction-to-Case		$R_{\theta JA}$	30	$^\circ C/W$
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 +175	$^\circ C$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG320G04HJRQ	F1	G320G04HJR	5000	10000	100000	13" reel



# YJG320G04HJRQ

## ■ Electrical Characteristics (T<sub>J</sub>=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	40			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =1mA	2	2.5	4	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =75A		0.85	1.1	mΩ
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V		0.8	1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz		2.8		Ω
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		7000		pF
Output Capacitance	C <sub>oss</sub>			2000		
Reverse Transfer Capacitance	C <sub>rss</sub>			320		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =50A	-	88	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	29	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	10	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =50A, di/dt=100A/us	-	63	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	58	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =20V, I <sub>D</sub> =50A R <sub>GEN</sub> =2.5Ω	-	17	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	12	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	56	-	
Turn-off fall Time	t <sub>f</sub>		-	25	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T<sub>J</sub>=25°C, V<sub>DD</sub>=30V, V<sub>G</sub>=10V, R<sub>G</sub>=25Ω, L=3mH, I<sub>AS</sub>=19A.

C. P<sub>q</sub> is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

D. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in the still air environment with T<sub>A</sub>=25°C.

The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design.



# YJG320G04HJRQ

## Typical Electrical and Thermal Characteristics Diagrams

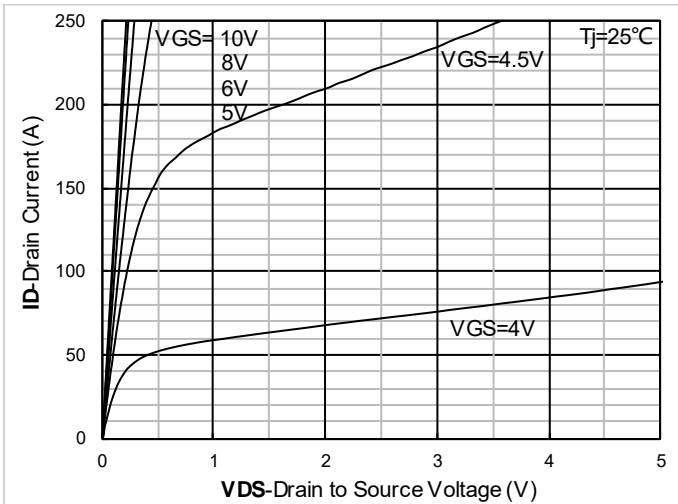


Figure 1. Output Characteristics

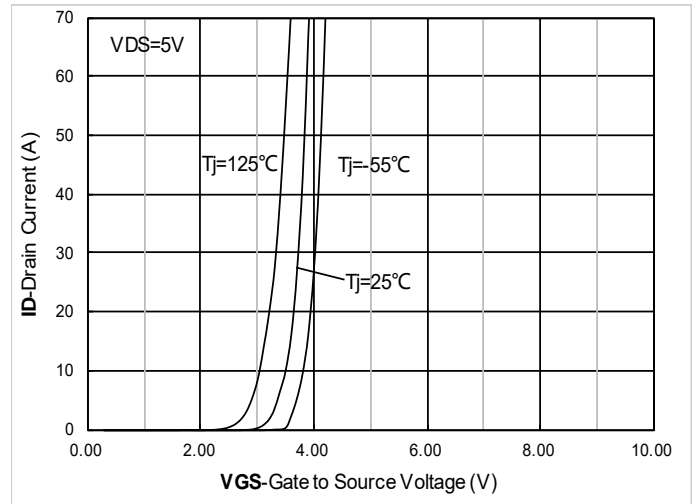


Figure 2. Transfer Characteristics

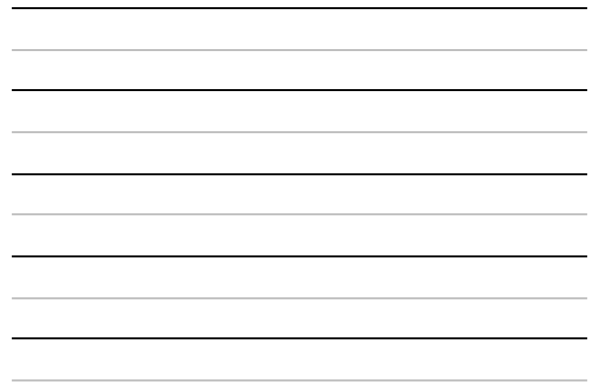


Figure 3. Capacitance Characteristics

Figure 4. Gate Charge

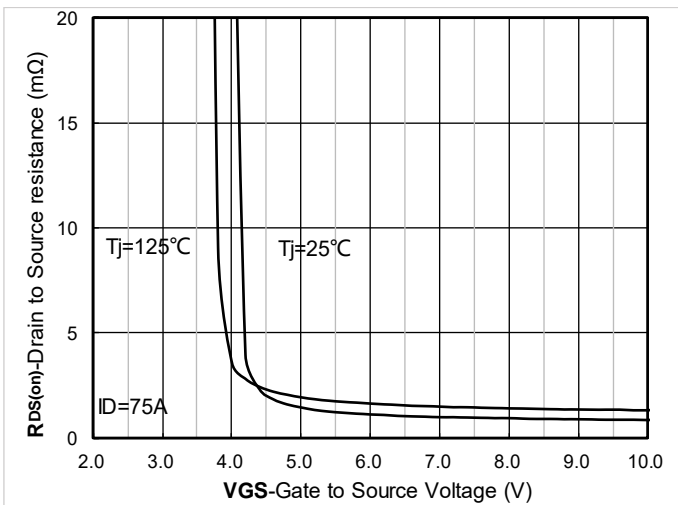


Figure 5. On-Resistance vs Gate to Source Voltage

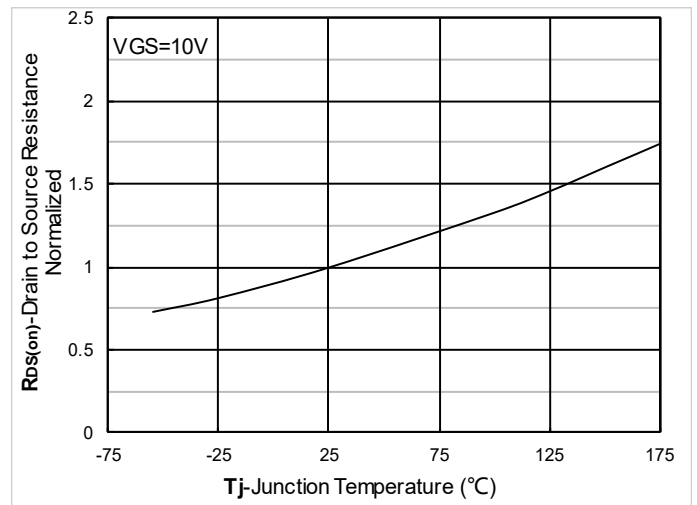


Figure 6. Normalized On-Resistance



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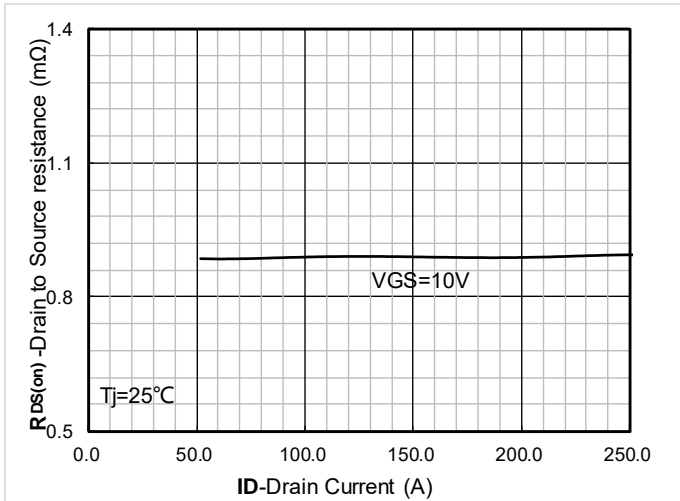


Figure 7.  $R_{DS(on)}$  VS Drain Current

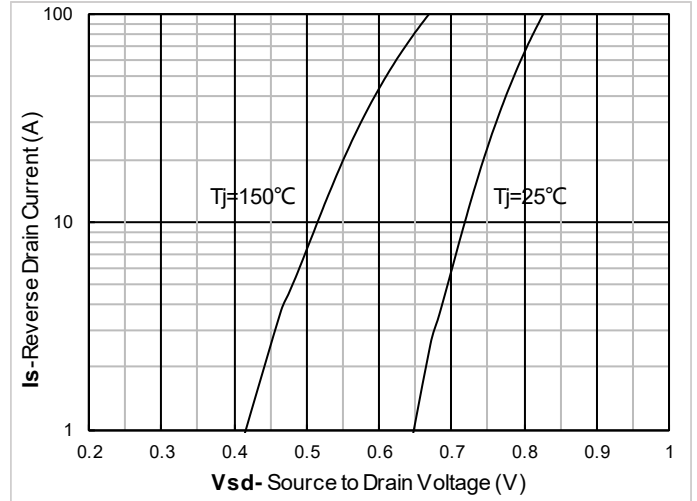


Figure 8. Forward characteristics of reverse diode

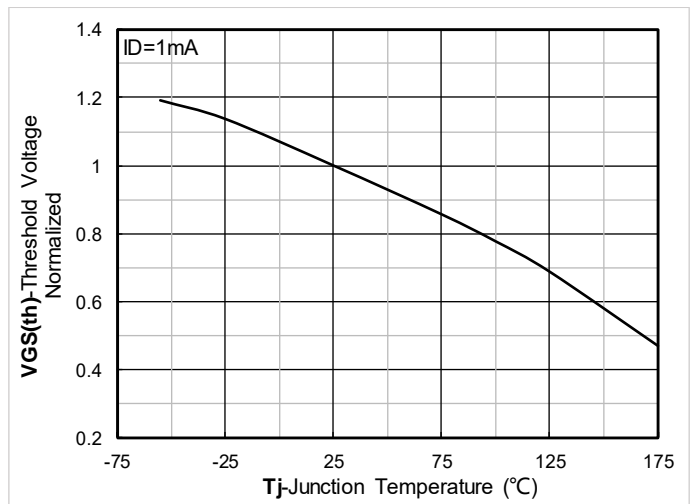


Figure 9. Normalized breakdown voltage

Figure 10. Normalized Threshold voltage

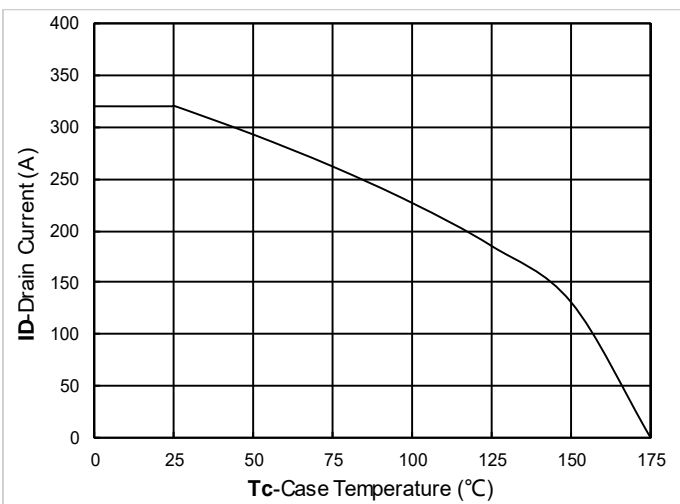


Figure 10. Current dissipation

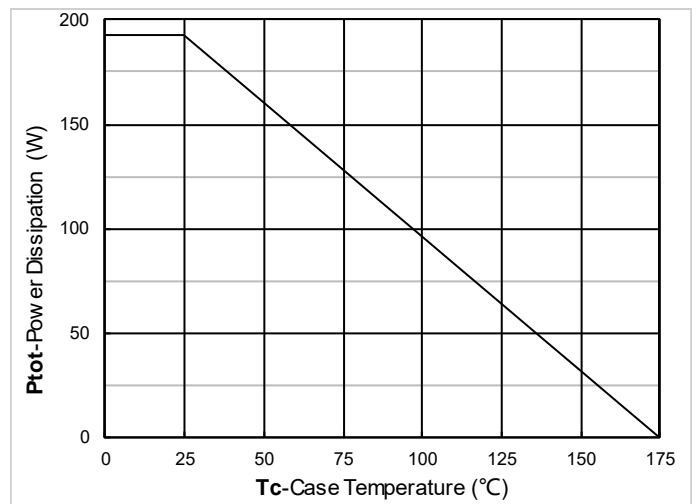


Figure 12. Power dissipation



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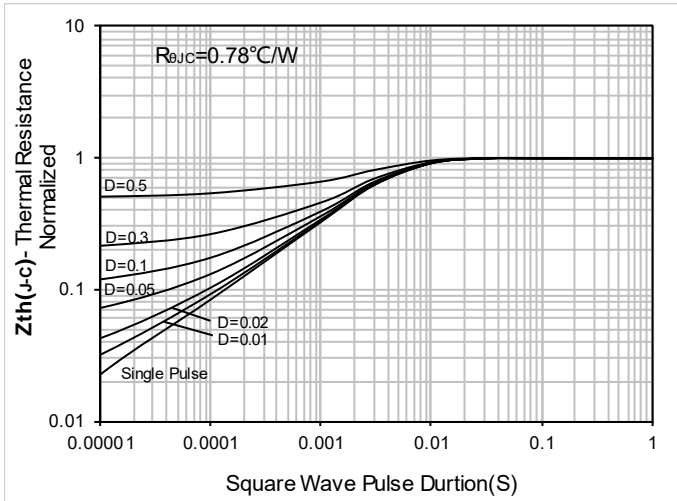


Figure 13. Maximum Transient Thermal Impedance

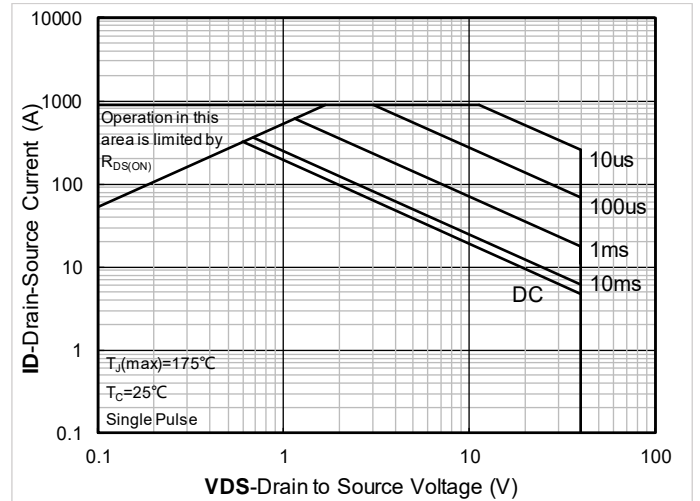
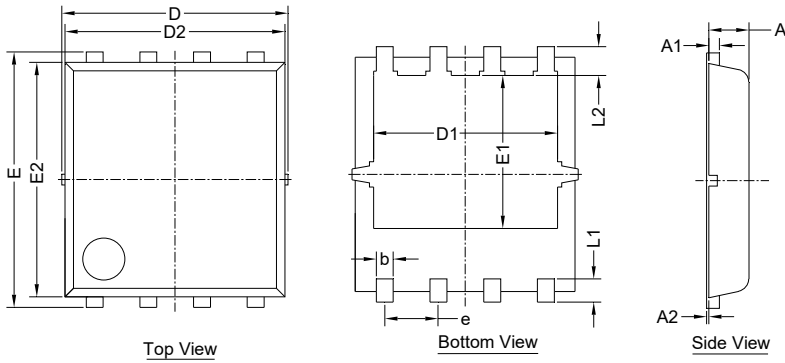


Figure 14. Safe Operation Area

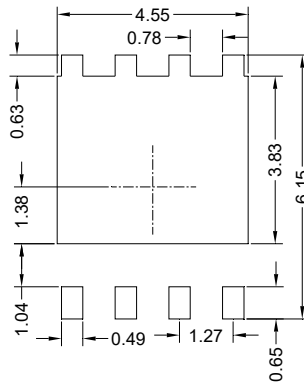


# YJG320G04HJRQ

## ■ PDFN5060-8L-0.95MM Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.05	6.15
A	0.85	0.95	1.05
A1	0.203 BSC		
A2			0.08
D1	4.25	4.35	4.45
E1	3.525	3.625	3.725
D2		5.20	
E2		5.55	
L1	0.45	0.55	0.65
L2	0.68 BSC		
b	0.3	0.4	0.5
e	1.27 BSC		



Suggested Solder Pad Layout  
Top View

**Note:**

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10\text{mm}$ .
3. The pad layout is for reference purposes only.

## ■ Marking Information





## YJG320G04HJRQ

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