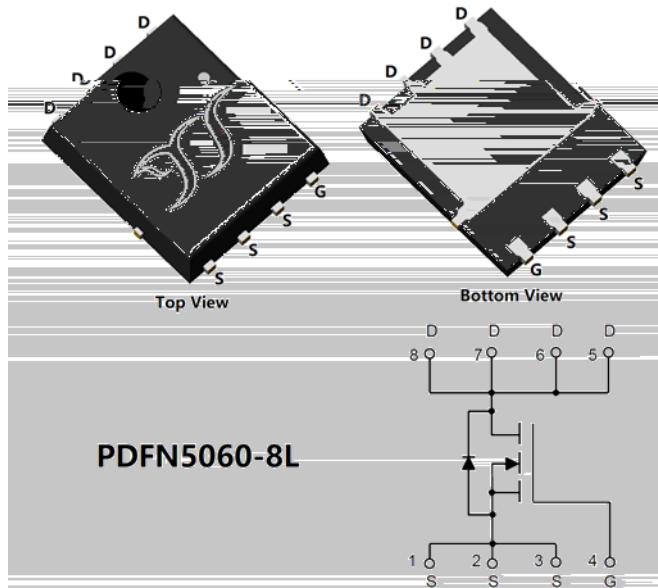


## N-Channel Enhancement Mode Field Effect Transistor



### Product Summary

$A_{DS}$	60V
$I_D$	30A
$r_{DS(ON)}$ (at $V_{GS}=10V$ )	<20mohm
$R_{DS(ON)}$ (at $V_{GS}=4.5V$ )	<23mohm
100% EAS Tested	
100% $\nabla V_{DS}$ Tested	

### General Description

PYNS Zb P MV MOSFET technology  
 High density cell design for Low  $R_{DS(ON)}$   
 High Speed switching  
 Moisture Sensitivity Level 1  
 Epoxy Meets UL 94 V-0 Flammability Rating  
 Halogen Free

### Applications

DC-DC Converters  
 Power management functions  
 Backlighting

### Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	60	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current	$I_D$	$T_C=25^\circ C$	30
		$T_C=100^\circ C$	19
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	130	A
Total Power Dissipation @ $T_C=25^\circ C$	$P_D$	45	W
Single Pulse Avalanche Energy <sup>B</sup>	$E_{AS}$	100	mJ
Thermal Resistance Junction-to-Case	$R_{JC}$	2.8	$^\circ C/W$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ C$

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG30N06A	F1	YJG30N06A	5000	10000	100000	13 reel



# YJG30N06A

## Electrical Characteristics ( $T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250$ ,	60			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$			1	,
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$			$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250$ ,	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=15A$		16	20	m
		$V_{GS}=4.5V, I_D=10A$		17.5	23	
Diode Forward Voltage	$V_{SD}$	$I_S=10A, V_{GS}=0V$		0.85	1.2	V
Maximum Body-Diode Continuous Current	$I_S$				30	A
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=30V, V_{GS}=0V, f=1\text{MHZ}$		2027		pF
Output Capacitance	$C_{oss}$			132		
Reverse Transfer Capacitance	$C_{rss}$			116		
<b>Switching Parameters</b>						
Total Gate Charge	$Q_g$	$V_{GS}=10V, V_{DS}=30V, I_D=10A$		51		nC
Gate-Source Charge	$Q_{gs}$			8.1		
Gate-Drain Charge	$Q_{gd}$			11.4		
Reverse Recovery Charge	$Q_{rr}$	$I_F=20A, di/dt=500A/us$		11.4		ns
Reverse Recovery Time	$t_{rr}$			22		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=30V, I_D=2A, R_{GEN}=3$		11		ns
Turn-on Rise Time	$t_r$			21		
Turn-off Delay Time	$t_{D(off)}$			40		
Turn-off fall Time	$t_f$			23		

A. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ .

B.  $R_{JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{JC}$  is guaranteed by design, while  $R_{JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



Typical Performance Characteristics

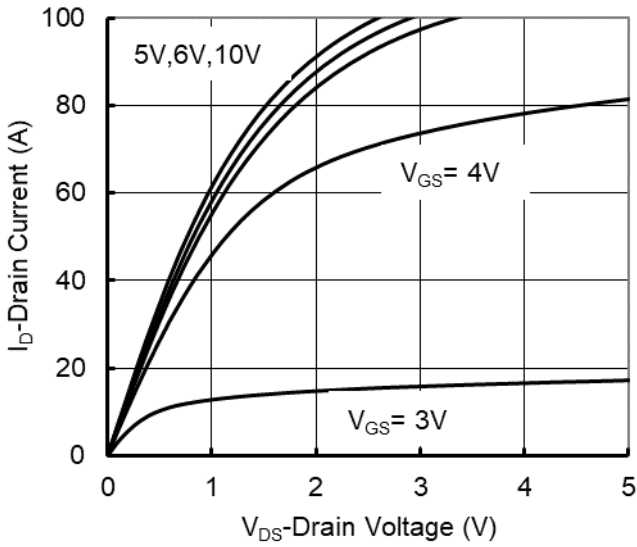


Figure 1. Output Characteristics

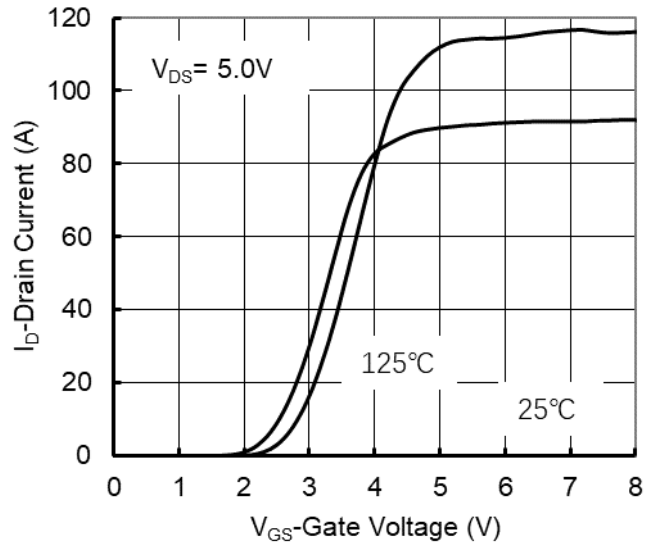


Figure 2. Transfer Characteristics

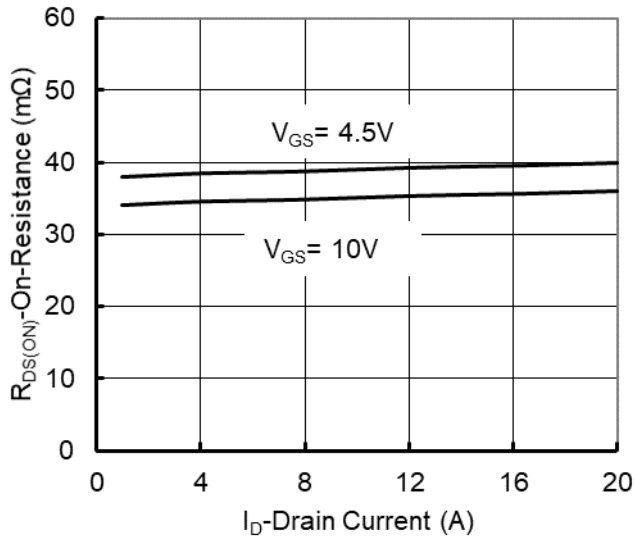


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

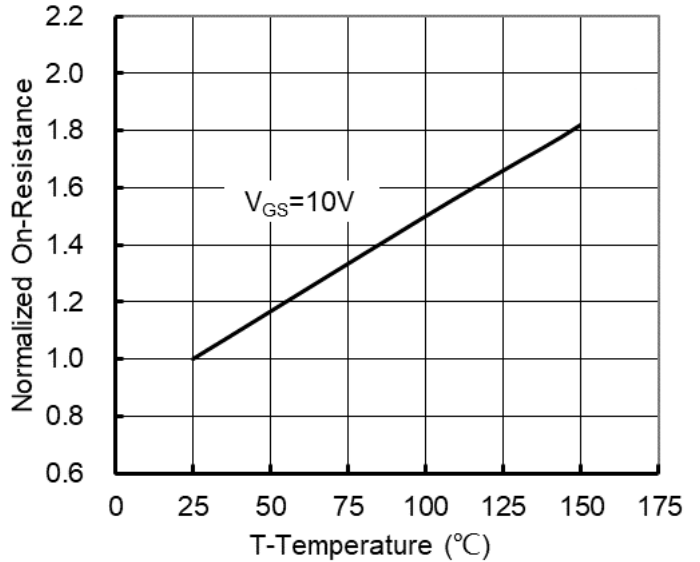


Figure 4. On-Resistance vs. Junction Temperature

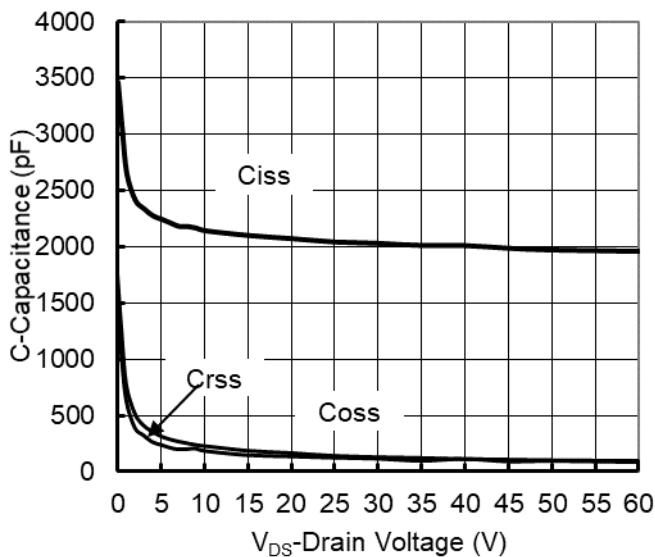


Figure 5. Capacitance Characteristics

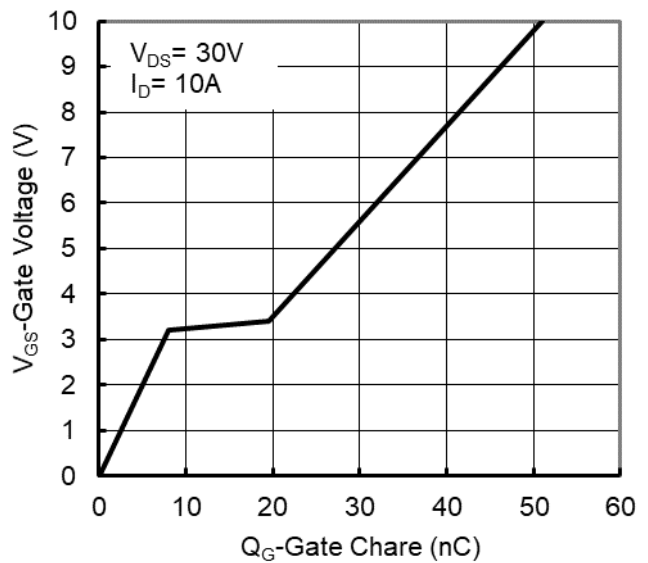


Figure 6. Gate Charge

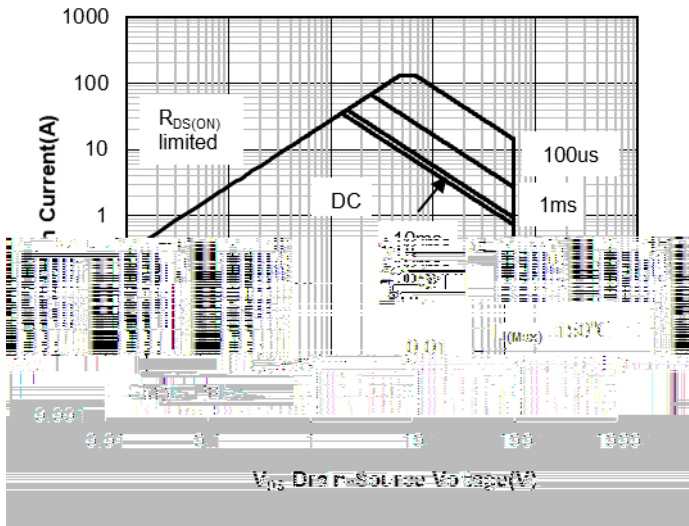


Figure 7. Safe Operation Area

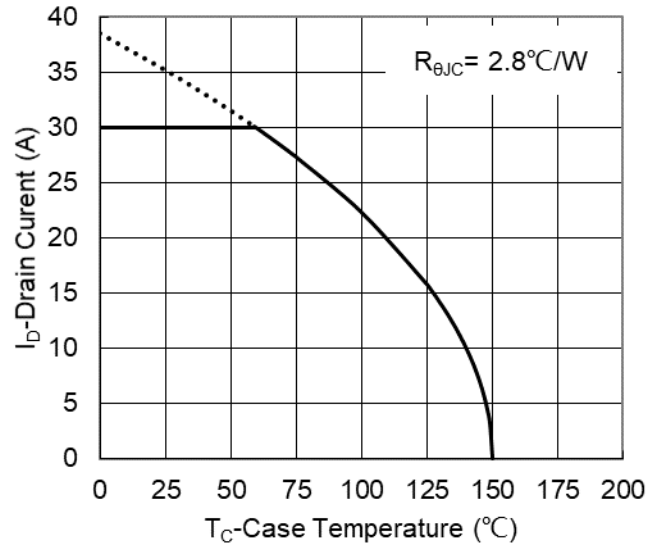


Figure 8. Maximum Continuous Drain Current vs Case Temperature

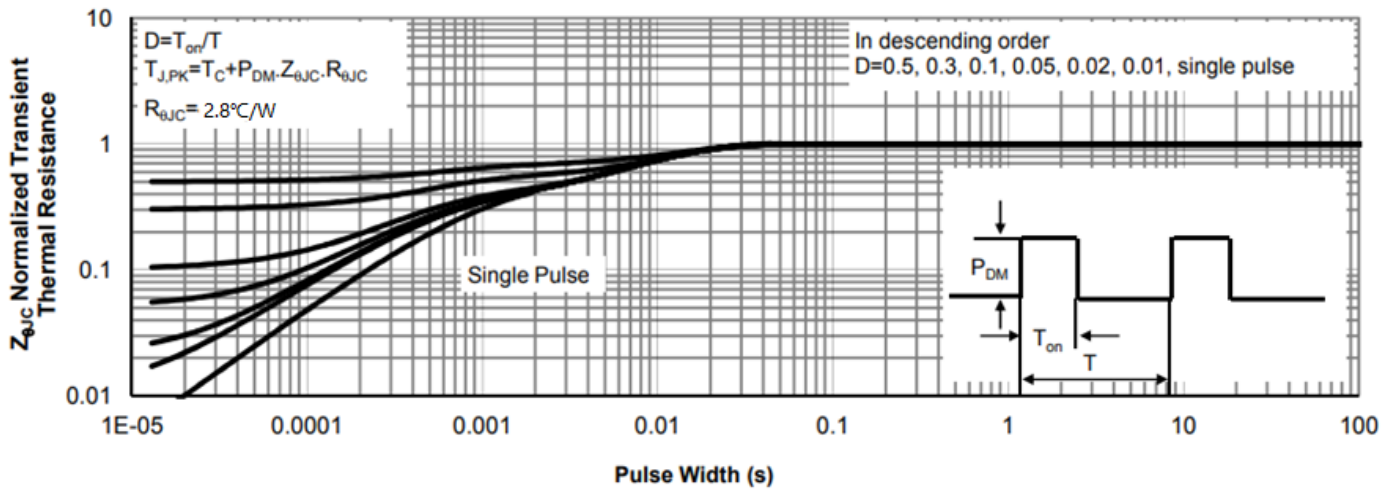
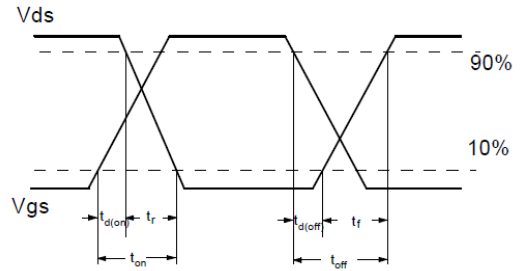
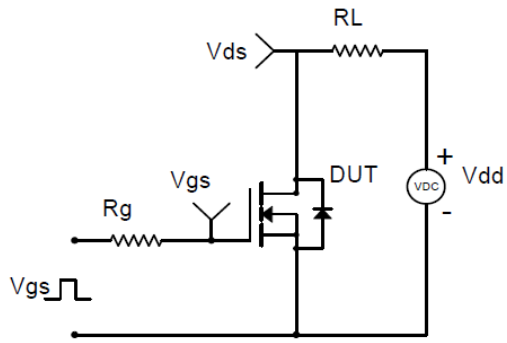
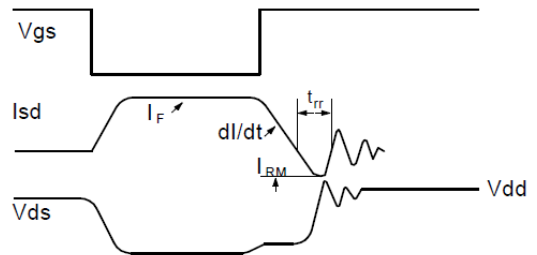
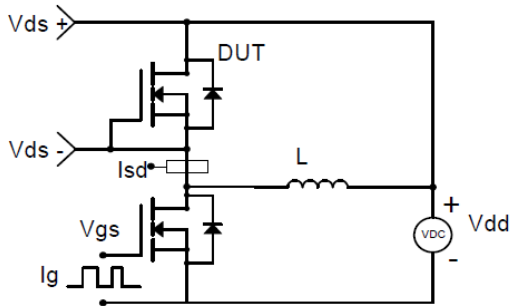


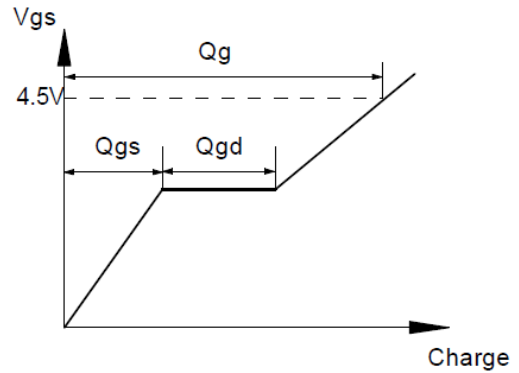
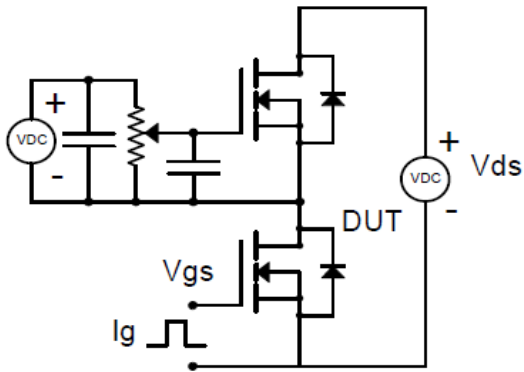
Figure 9. Normalized Maximum Transient Thermal Impedance



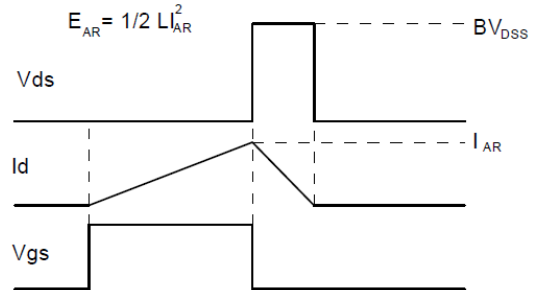
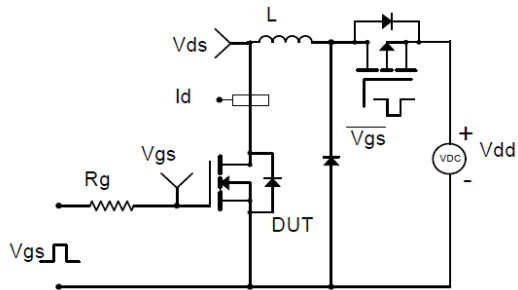
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

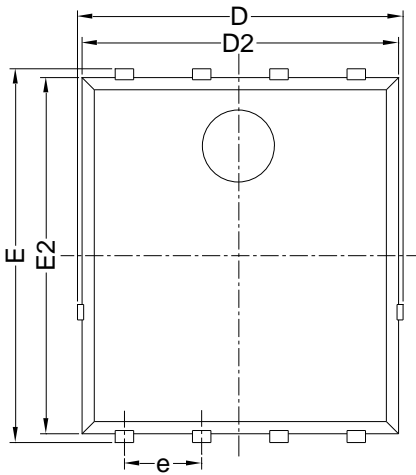


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

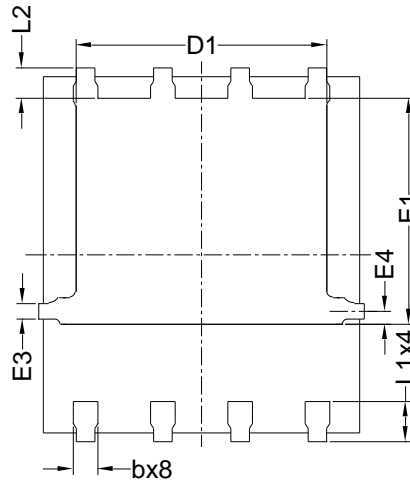


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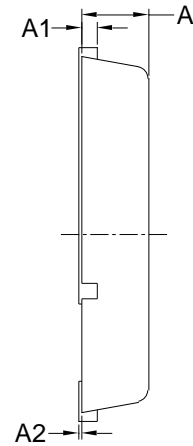
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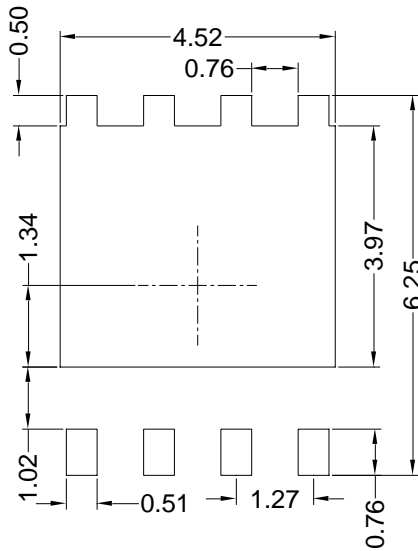
Top View  
正面视图



Bottom View  
背面视图



Side View  
侧面视图



Suggested Solder Pad Layout  
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.



# YJG30N06A

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