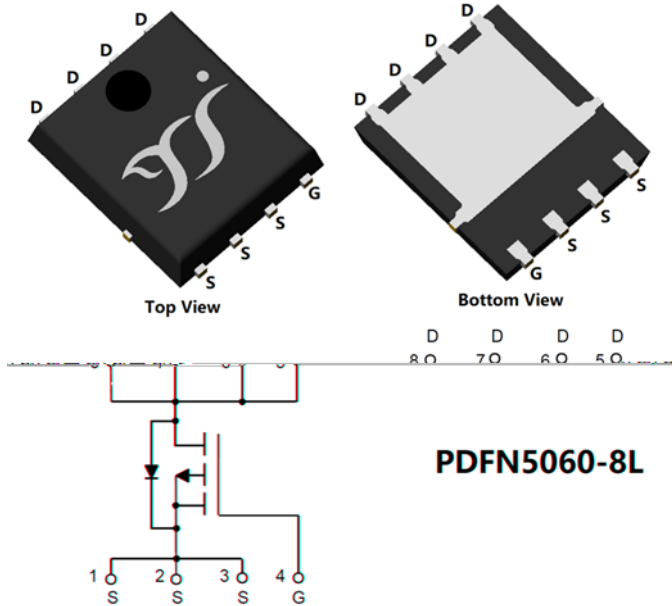


## P-Channel Enhancement Mode Field Effect Transistor



**PDFN5060-8L**

### Product Summary

$V_{DS}$	-60V
$I_D$	-25A
$R_{DS(ON)}$ ( at $V_{GS}=-10V$ )	<50 mohm
$R_{DS(ON)}$ ( at $V_{GS}=-4.5V$ )	<65 mohm
100% EAS Tested	
100% $\nabla V_{DS}$ Tested	

### General Description

- Split gate trench MOSFET technology
- Low  $R_{DS(on)}$  & FOM
- Low  $C_{rss}$
- Extremely low switching loss
- Excellent stability and uniformity
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- Automotive Systems
- Industrial DC/DC Conversion Circuits

### Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	-60	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_C=25^\circ C$	$I_D$	-25	A
	$T_C=100^\circ C$		-16	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	-75	A
Avalanche energy <sup>B</sup>		EAS	81	mJ
Total Power Dissipation <sup>C</sup>	$T_C=25^\circ C$	$P_D$	60	W
	$T_C=100^\circ C$		24	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ C$

### Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	$t \leq 10S$	R	15	20	$^\circ C/W$
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State		40	50	
Thermal Resistance Junction-to-Case	Steady-State	R	1.7	2.1	

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG25GP06A	F1	YJG25GP06A	5000	10000	100000	13 reel



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## Electrical Characteristics ( $T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250$	-60			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-60V, V_{GS}=0V$	$T_J=25^\circ\text{C}$		-1	
			$T_J=55^\circ\text{C}$		-5	
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$			$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250$	-1.3	-1.8	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-20A$		38	50	m
		$V_{GS}=-4.5V, I_D=-10A$		48	65	
Gate Resistance	$R_g$	$f=1\text{MHz}$		12		
Diode Forward Voltage	$V_{SD}$	$I_S=-20A, V_{GS}=0V$		-0.95	-1.3	V
Maximum Body-Diode Continuous Current	$I_S$				-25	A
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=-30V, V_{GS}=0V, f=1\text{MHz}$		1100		pF
Output Capacitance	$C_{oss}$			350		
Reverse Transfer Capacitance	$C_{rss}$			28		
<b>Switching Parameters</b>						
Total Gate Charge	$Q_{g(-10V)}$	$V_{GS}=-10V, V_{DS}=-30V, I_D=-20A$		18.7		nC
Total Gate Charge	$Q_{g(-4.5V)}$			8.8		
Gate-Source Charge	$Q_{gs}$			4.7		
Gate-Drain Charge	$Q_{gd}$			3.0		
Reverse Recovery Charge	$Q_{rr}$	$I_F=-20A, di/dt=100A/\mu s$		8.2		ns
Reverse Recovery Time	$t_{rr}$			20.2		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=-10V, V_{DD}=-30V, R_L=2.5$ $R_{GEN}=6$		7.5		ns
Turn-on Rise Time	$t_r$			39.5		
Turn-off Delay Time	$t_{D(off)}$			43.6		
Turn-off fall Time	$t_f$			55.1		

A. Repetitive rating; pulse width limited by max. junction temperature.

B.  $V_{DD}=50V, R_G=0.5m\Omega, I_{AS}=18A$ .

C.  $P_d$  is based on max. junction temperature, using junction-case thermal resistance.

D. The value of  $R_{qJA}$  is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The  $P_{\text{Power}}$  application depends on the user's specific board design.  $^\circ\text{C}$ . The value in any given



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## ■ Typical Performance Characteristics

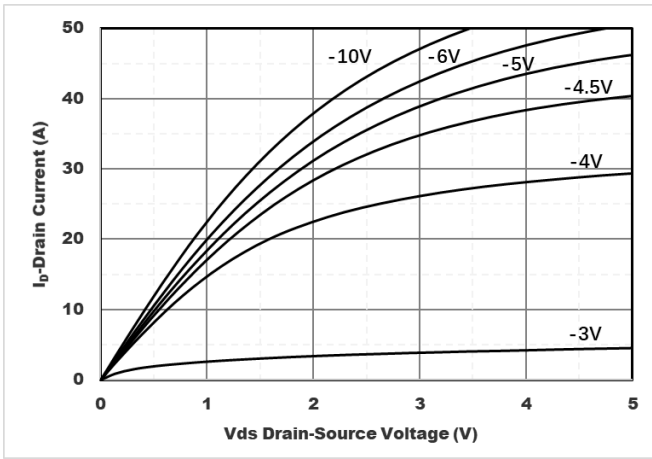


Figure1. Output Characteristics

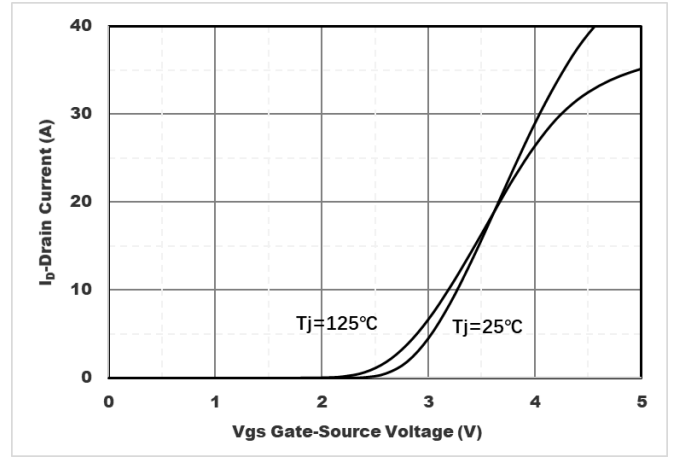


Figure2. Transfer Characteristics

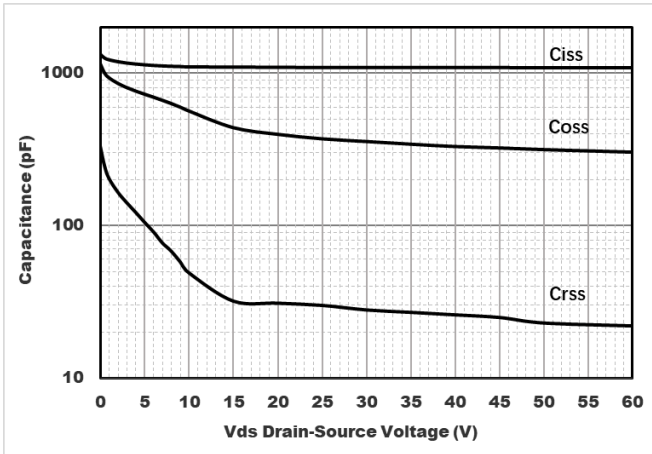


Figure3. Capacitance Characteristics

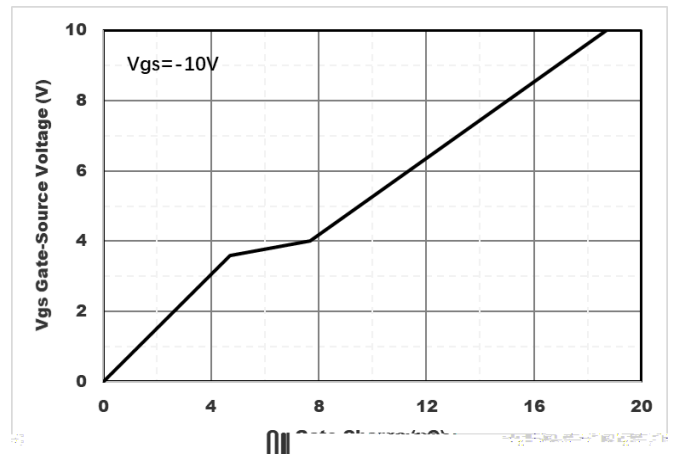


Figure4. Gate Charge

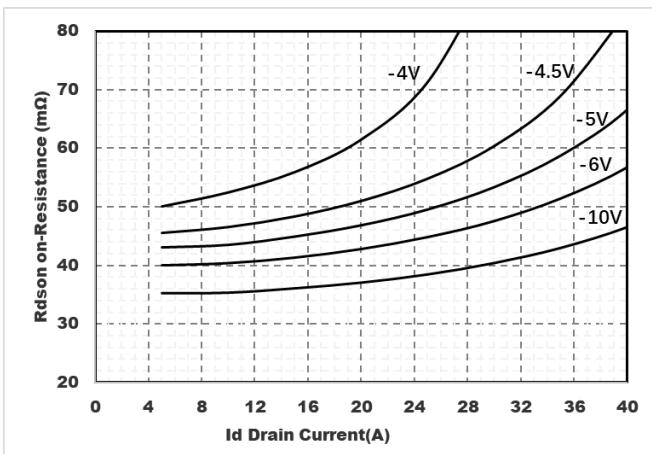


Figure5. : On-Resistance vs. Gate to Source Voltage

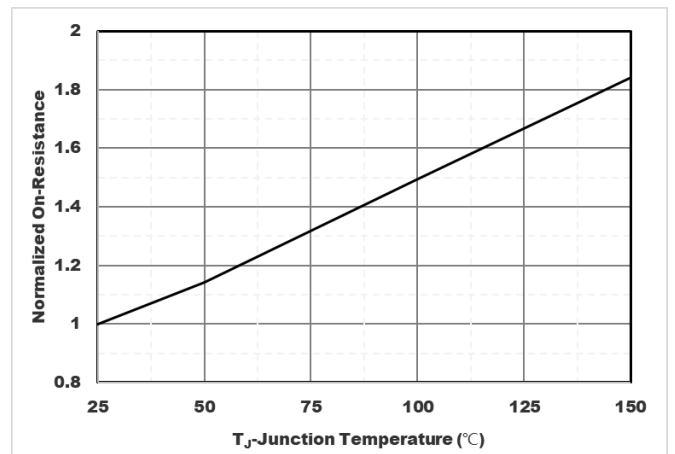


Figure6. Normalized On-Resistance



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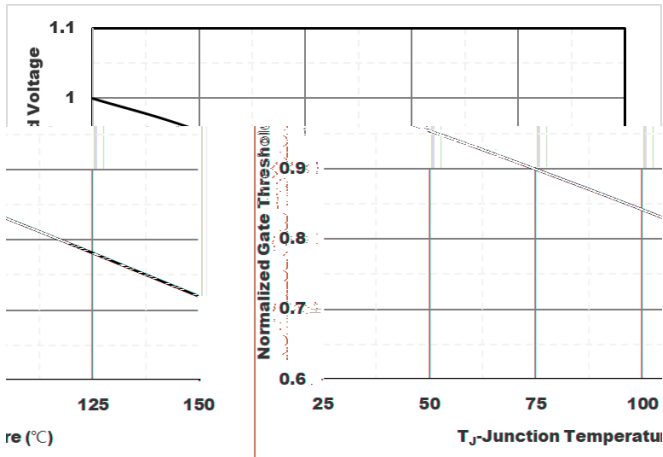


Figure7. Normalized Gate Threshold Voltage

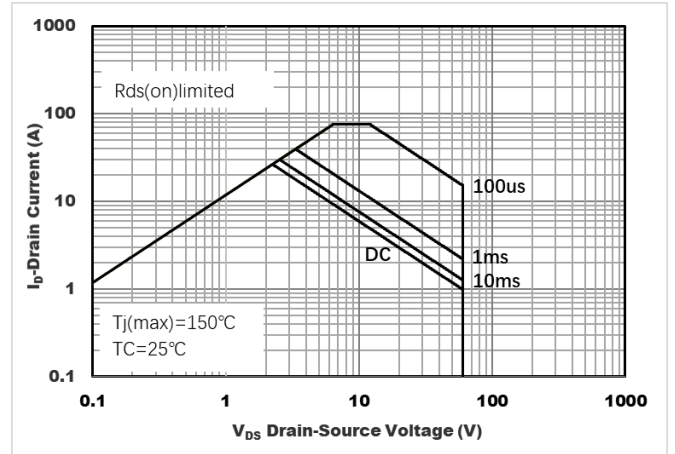


Figure8.Safe Operation Area

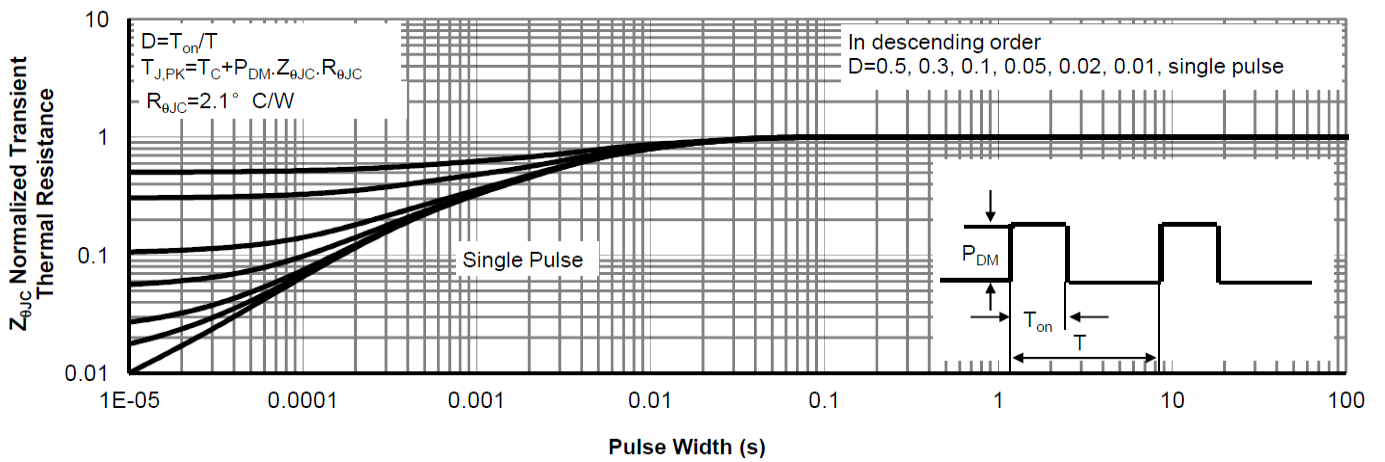
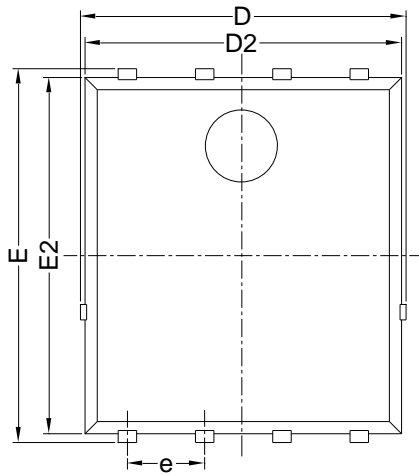


Figure9.Normalized Maximum Transient thermal impedance

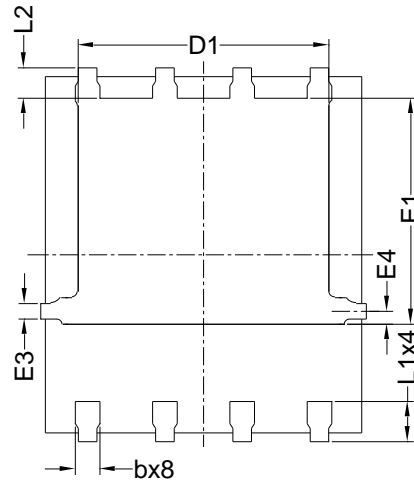


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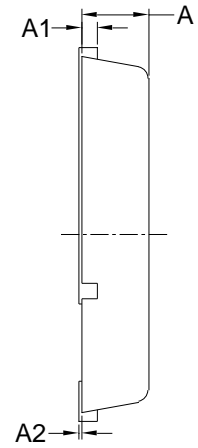
## PDFN5060-8L-B-1.1MM Package information



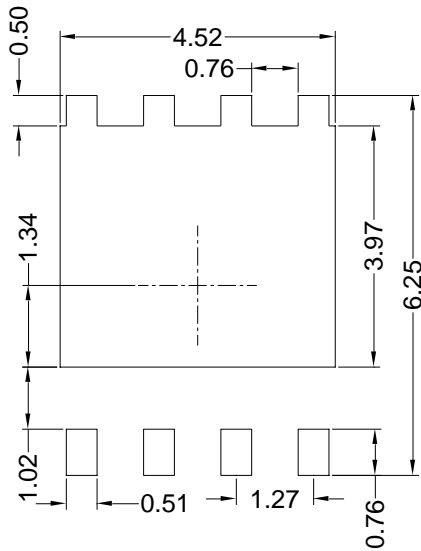
Top View  
正面视图



Bottom View  
背面视图



Side View  
侧面视图



Suggested Solder Pad Layout  
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.



## YJG25GP06A

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