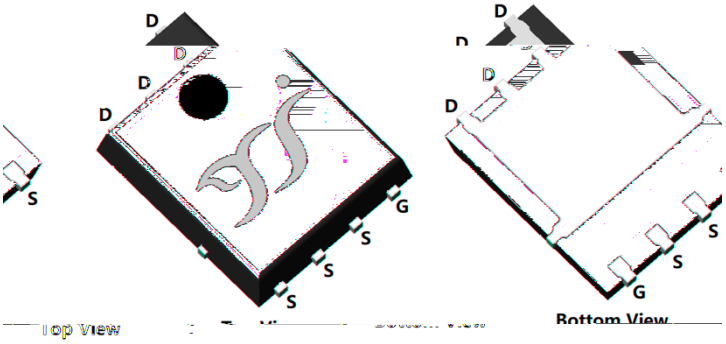
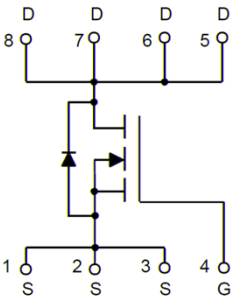
RoHS COMPLIANT

N-Channel Enhancement Mode Field Effect Transistor



DFN5060-8L



Product Summary

C_{DS}	100V
6	18A
$_{DS(ON)}$(at V_{GS}= 10V)	＜60mohm
$_{DS(ON)}$(at V_{GS}= 4.5V)	＜70mohm

100% EAS Tested
100% ▽V_{DS} Tested

General Description

A R PU = R MV MOSFET technology
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Moisture Sensitivity Level 1
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

DC-DC Converters
Power management functions
Backlighting

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	3.5	A
	T_A=100℃		2	
	T_C=25℃		18	
	T_C =100℃		11.4	
Pulsed Drain Current [A]		I_{DM}	75	A
Total Power Dissipation[B]	T_A=25℃	P_D	2	W
	T_A=100℃		0.8	
	T_C=25℃		45	
	T_C =100℃		18	
Single Pulse Avalanche Energy [C]		E_{AS}	12.5	mJ
Thermal Resistance Junction-to-Case		R $_{JC}$	2.8	℃/ W
Thermal Resistance Junction-to-Ambient [D]		R $_{7.}$	60	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG18N10A	F1	YJG18N10A	5000	10000	100000	13 reel

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250 .	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V			1	.
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250 .	1.1	1.8	3.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=8A		49	60	m
		V_{GS}= 4.5V, I_D=8A		52	70	
Diode Forward Voltage	V_{SD}	I_S=18A,V_{GS}=0V		0.8	1.2	V
Gate resistance	R_G	f=1MHz, Open drain	-	1.2	-	
Maximum Body-Diode Continuous Current	I_S				18	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHZ		2071		pF
Output Capacitance	C_{oss}			73		
Reverse Transfer Capacitance	C_{rss}			54		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=10A		51.4		nC
Gate-Source Charge	Q_{gs}			9.1		
Gate-Drain Charge	Q_{gd}			11.5		
Reverse Recovery Chrage	Q_{rr}	I_F=10A, di/dt=100A/us		35.3		
Reverse Recovery Time	t_{rr}			38		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=50V, I_D=2A R_{GEN}=3		10		
Turn-on Rise Time	t_r			19		
Turn-off Delay Time	$t_{D(off)}$			42		
Turn-off fall Time	t_f			26		

A. Repetitive rating; pulse width limited by max. junction temperature.
B. P_d is based on max. junction temperature, using junction-case thermal resistance.
C. Tj=25℃, VDD=50V, VGS=10V, L=1mH, IAS=5A.
D. The NYR S 7. V ZRN RQ YaUaURQR VPRZ aRQ V 3 -4 board with 2oz. Copper, in the still air environment with TA =25℃. The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

Typical Performance Characteristics

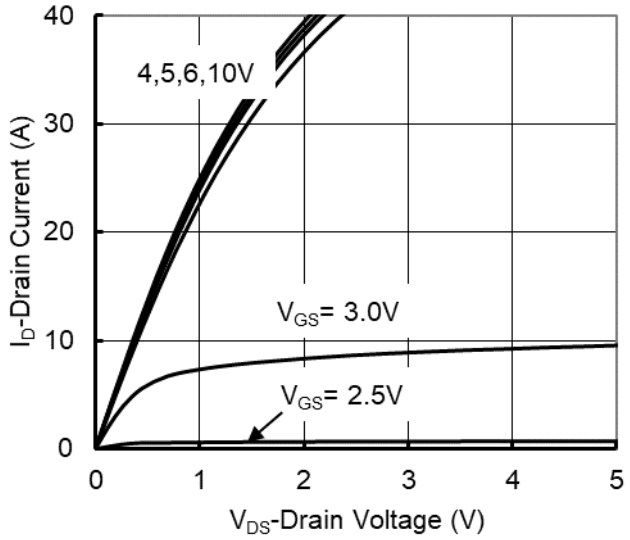


Figure 1. Output Characteristics

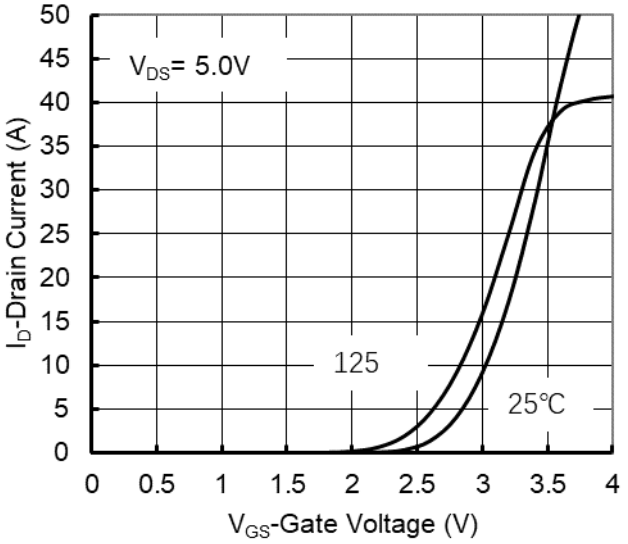


Figure 2. Transfer Characteristics

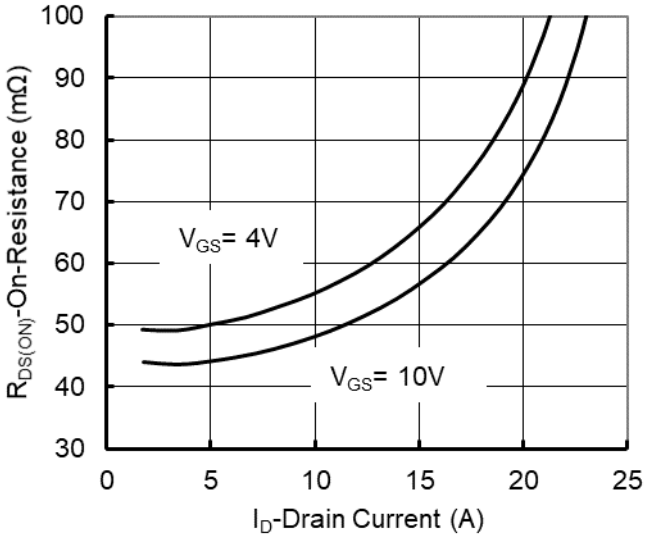


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

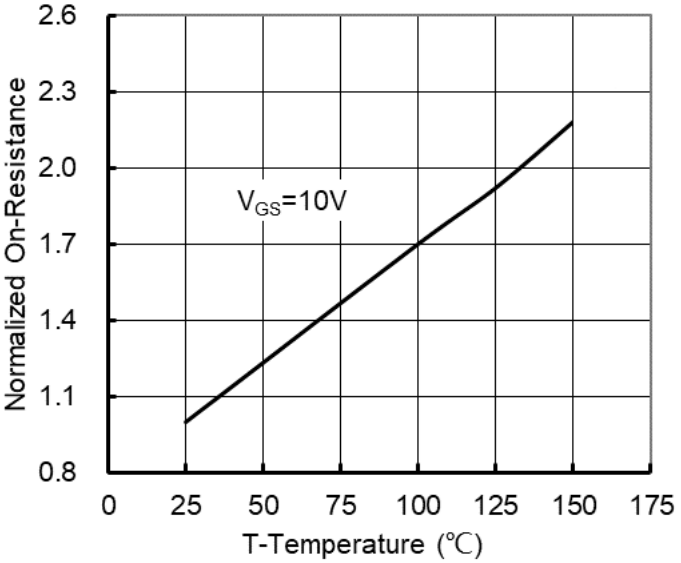


Figure 4. On-Resistance vs. Junction Temperature

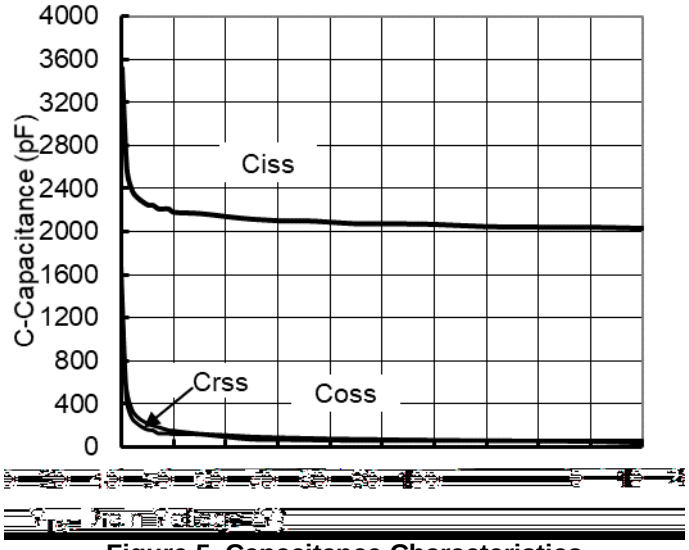


Figure 5. Capacitance Characteristics

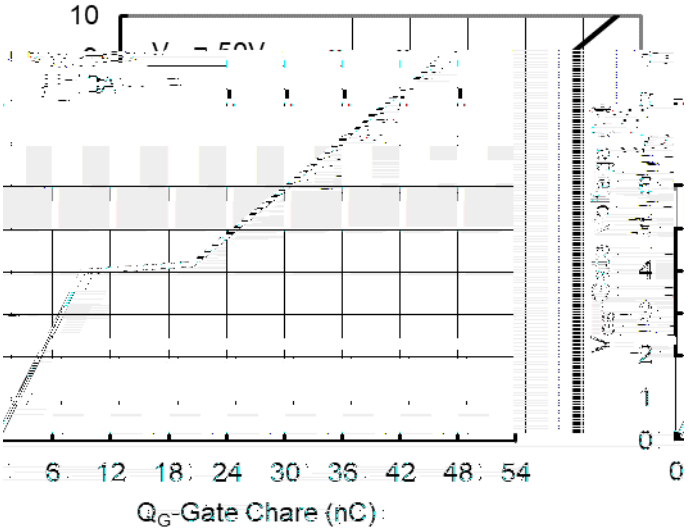


Figure 6. Gate Charge

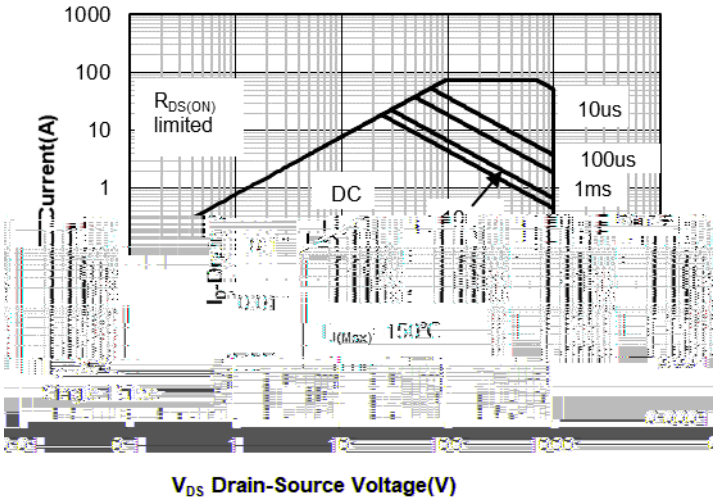


Figure 7. Safe Operation Area

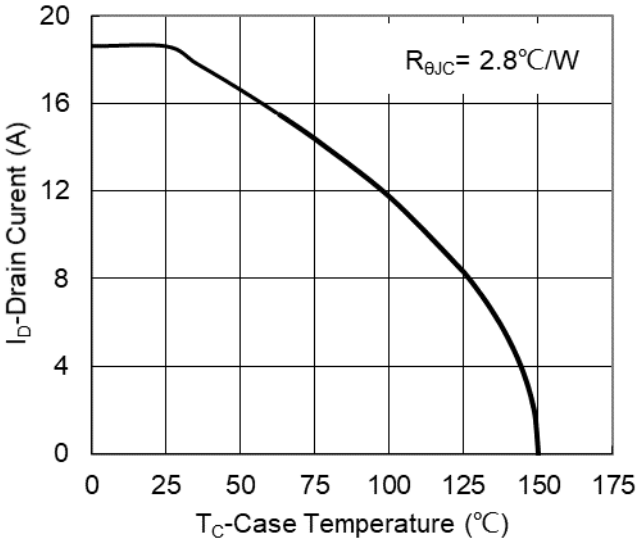


Figure 8. Maximum Continuous Drain Current vs Case Temperature

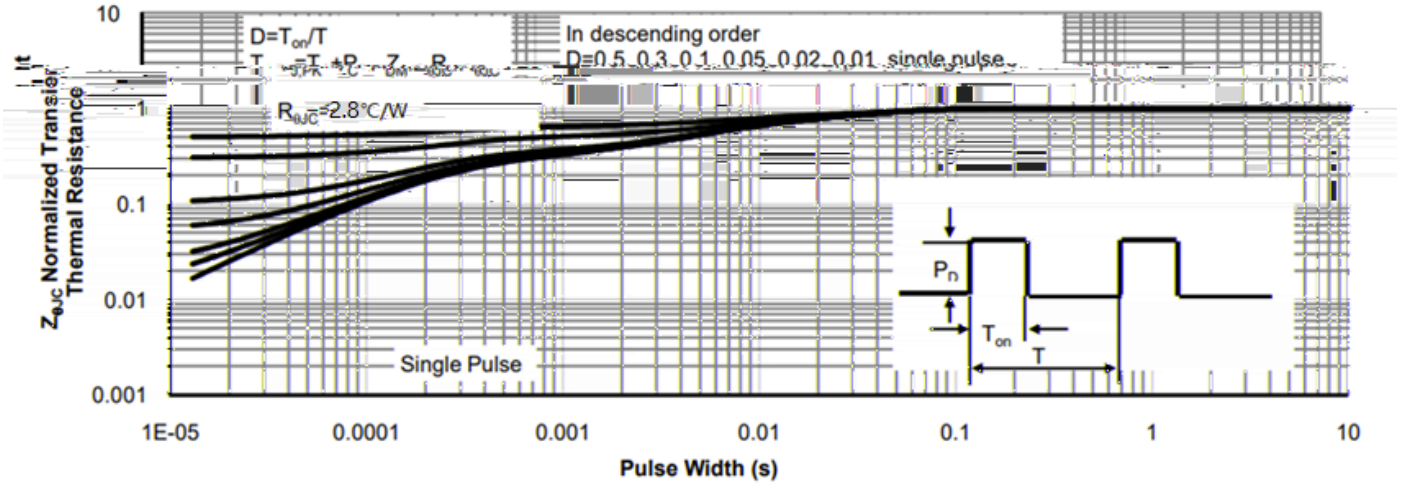
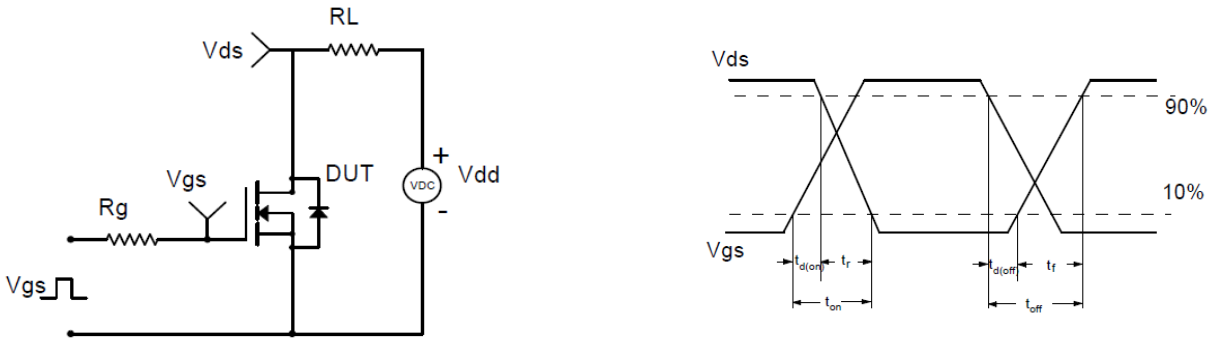
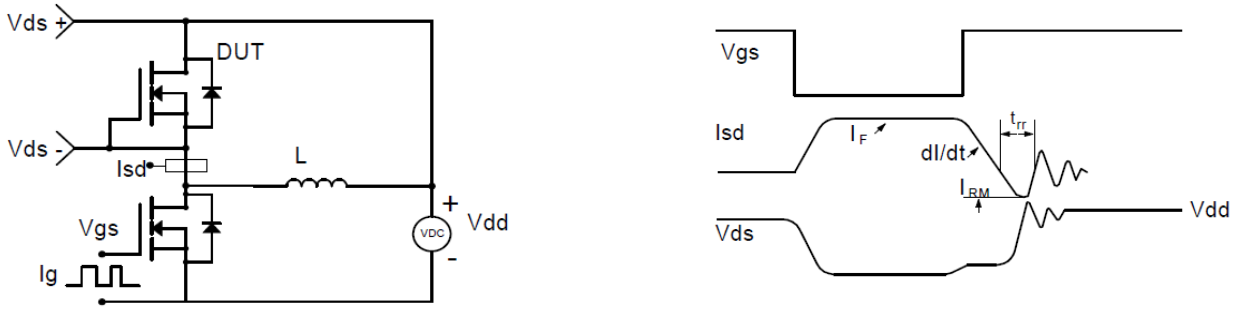


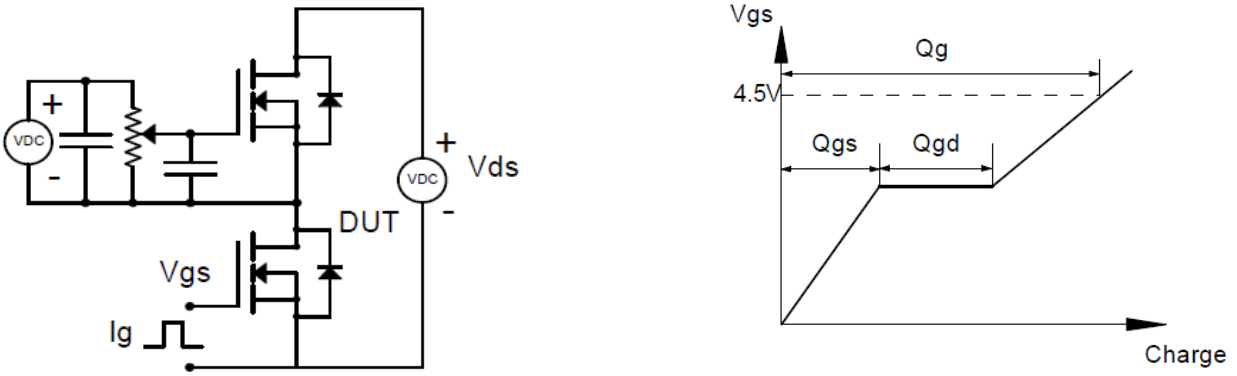
Figure 9. Normalized Maximum Transient Thermal Impedance



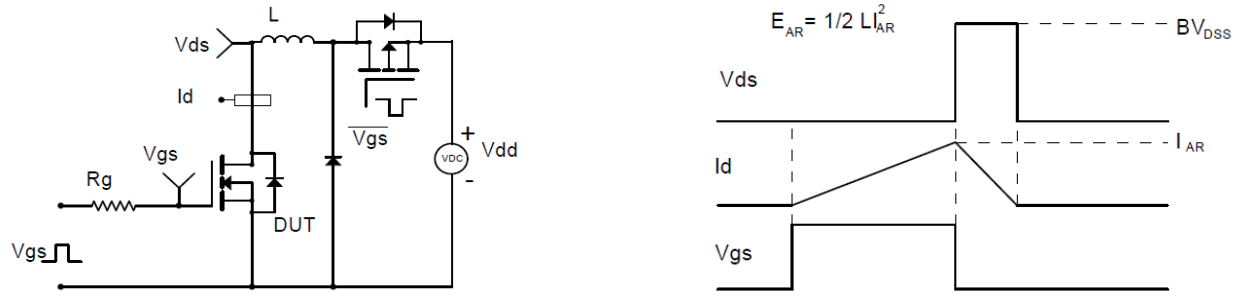
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

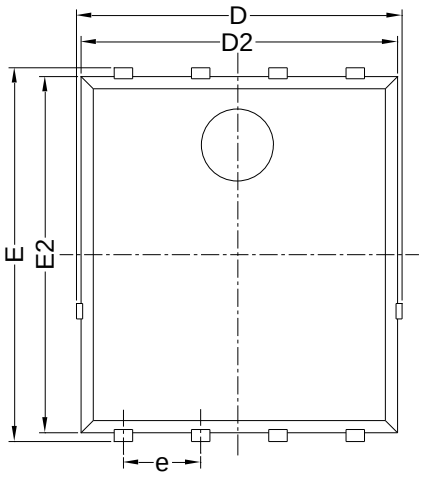


Gate Charge Test Circuit & Waveform

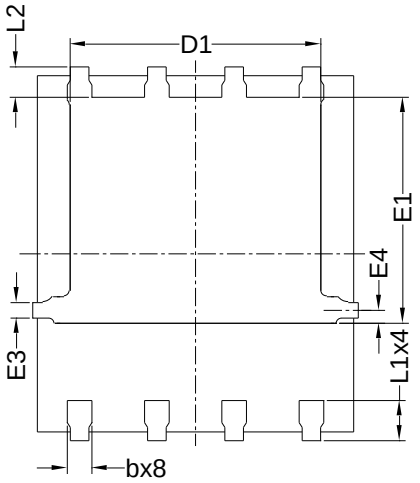


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

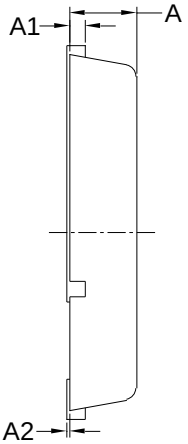
PDFN5060-8L-B-1.1MM Package Information



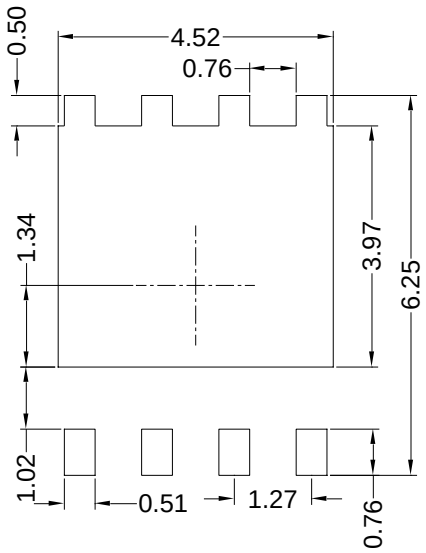
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254 REF	
E4		0.21 REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

Disclaimer

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