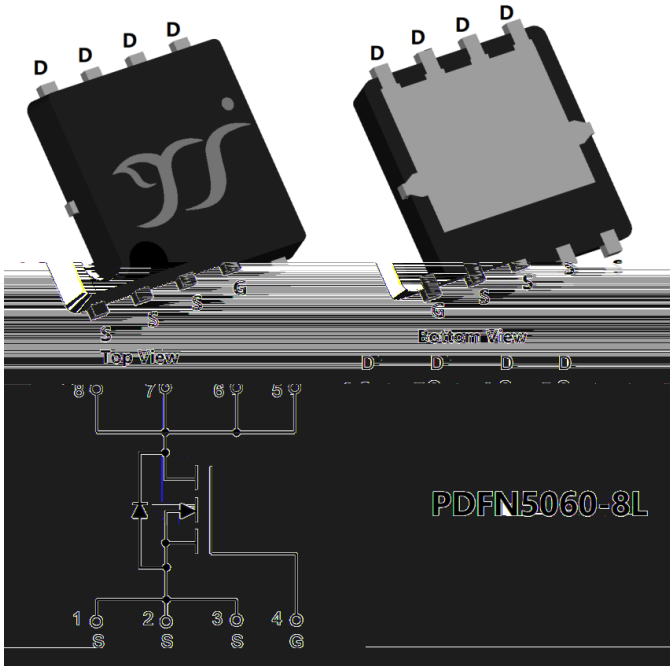


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 80V
- I_D 110A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<3.9m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=6V$) $<6m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	80	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	17	A
	$T_A=100^\circ C$		10	
	$T_C=25^\circ C$		110	
	$T_C=100^\circ C$		69	
Pulsed Drain Current ^A		I_{DM}	400	A
Avalanche energy ^B		EAS	937	mJ
Total Power Dissipation ^C	$T_A=25^\circ C$	P_D	2.5	W
	$T_A=100^\circ C$		1	
	$T_C=25^\circ C$		125	
	$T_C=100^\circ C$		50	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	$R_{\theta JA}$	40	50	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.8	1	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG110G08HR	F1	G110G08HR	5000	10000	100000	13" reel



YJG110G08HR

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	80	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V	-	-	1	μA
		V _{DS} =80V, V _{GS} =0V, T _J =150°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	2	3	4	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =55A	-	2.9	3.9	mΩ
		V _{GS} =10V, I _D =20A	-	2.9	3.9	
		V _{GS} =6V, I _D =20A	-	4.5	6	
Diode Forward Voltage	V _{SD}	I _S =55A, V _{GS} =0V	-	0.9	1.2	V
Gate resistance	R _G	f=1MHz, Open drain	-	2	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	110	A
Dynamic Parameters						
Input Capacitance	C _{iss}		-	5290	-	
Output Capacitance	C _{oss}	V _{DS} =40V, V _{GS} =0V, f=1MHz	-	870		pF



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Typical Electrical and Thermal Characteristics Diagrams

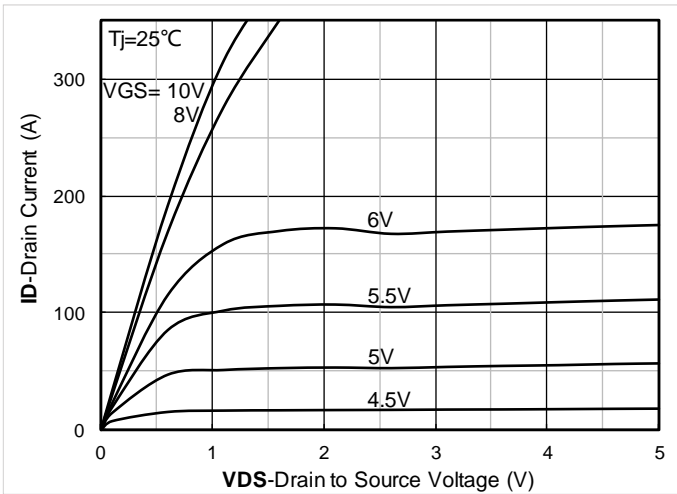


Figure 1. Output Characteristics

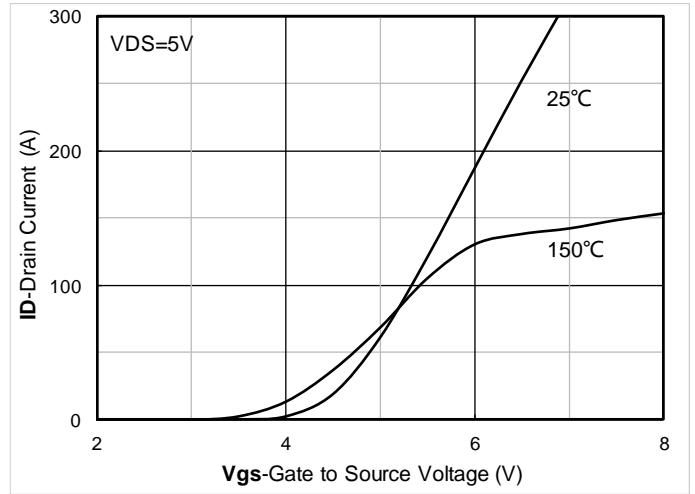


Figure 2. Transfer Characteristics

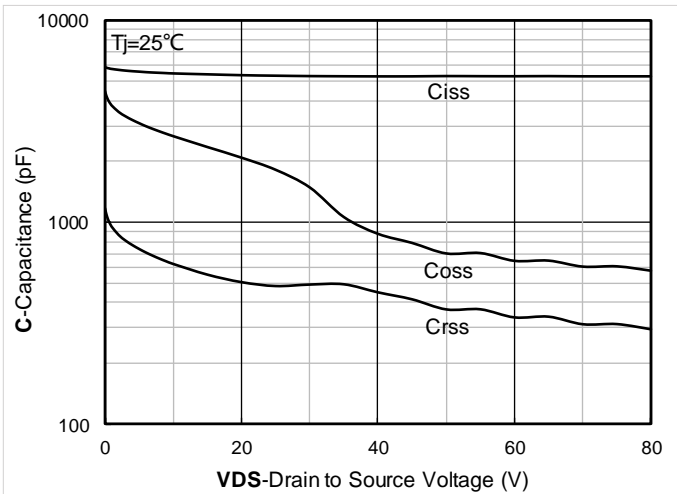


Figure 3. Capacitance Characteristics

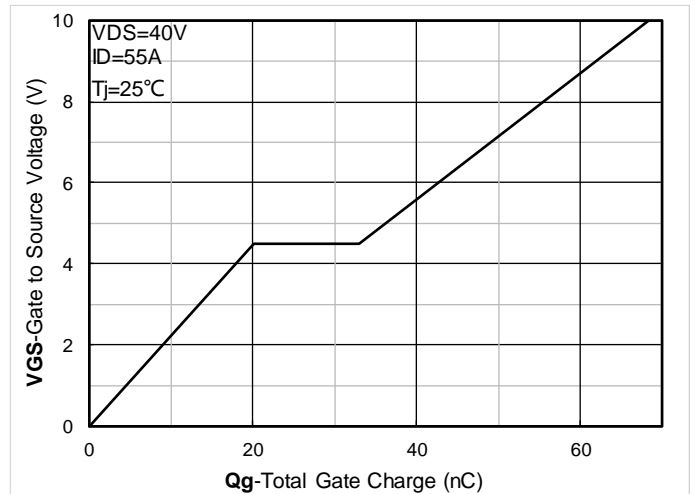


Figure 4. Gate Charge

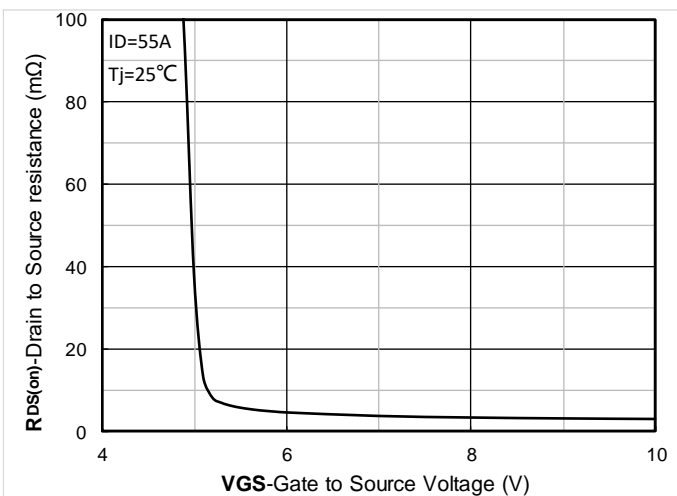


Figure 5. On-Resistance vs Gate to Source Voltage

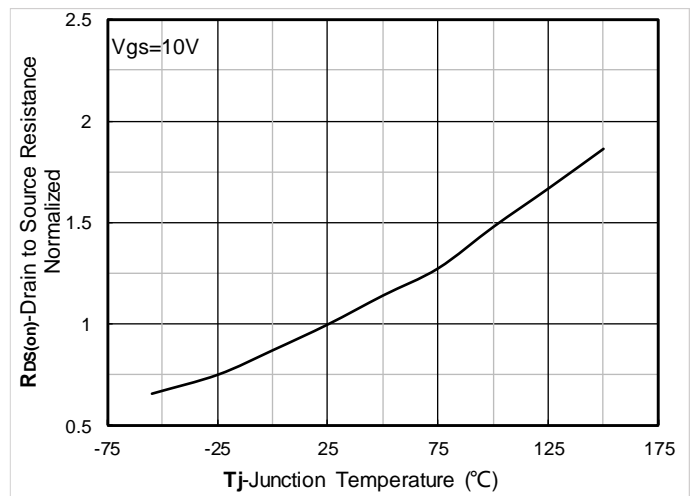


Figure 6. Normalized On-Resistance



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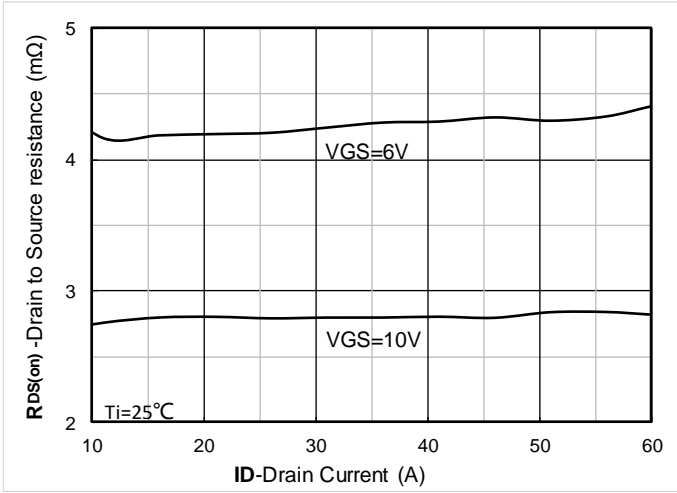


Figure 7. RDS(on) VS Drain Current

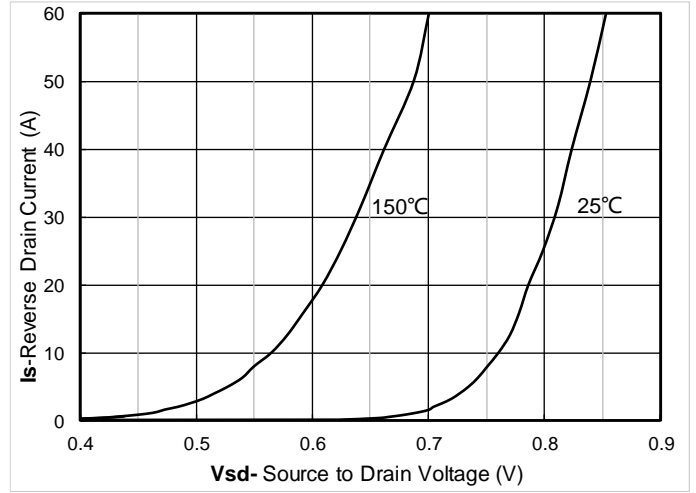


Figure 8. Forward characteristics of reverse diode

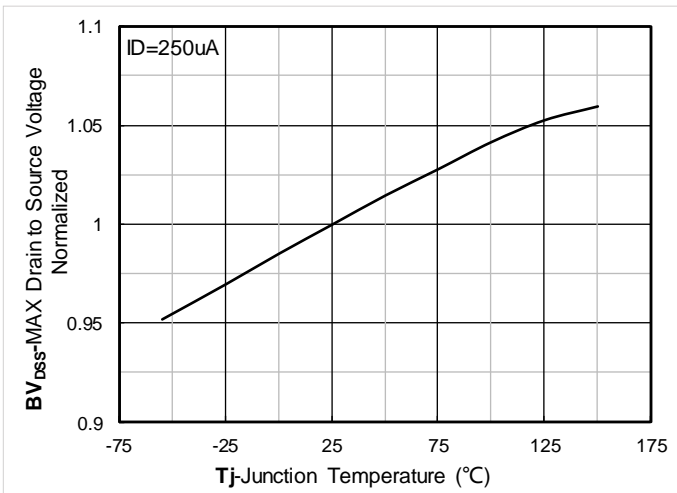


Figure 9. Normalized breakdown voltage

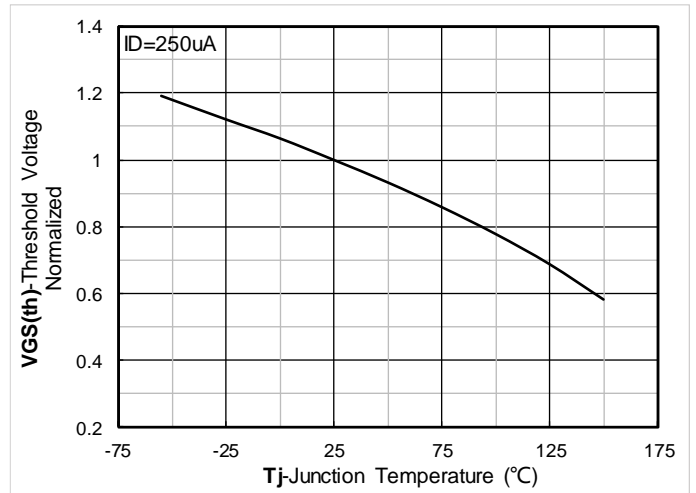


Figure 10. Normalized Threshold voltage

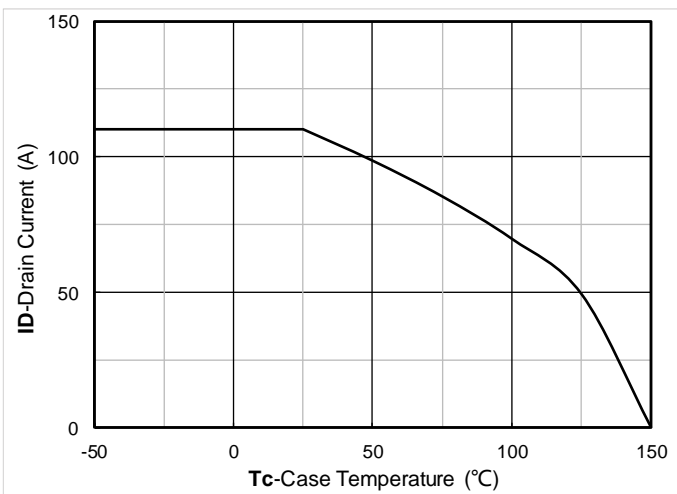


Figure 11. Current dissipation

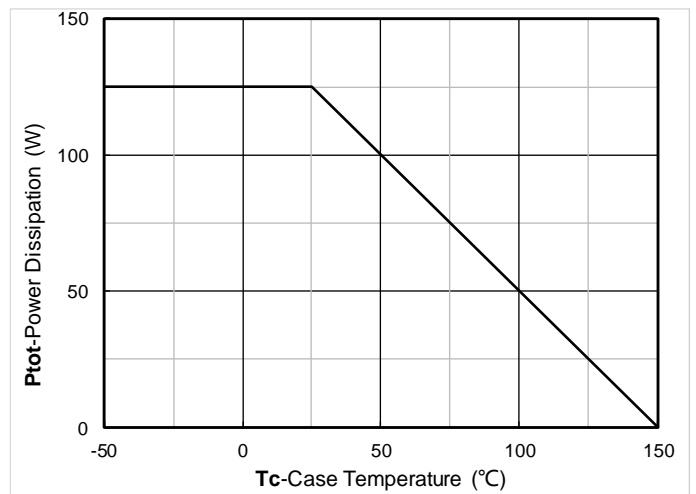


Figure 12. Power dissipation

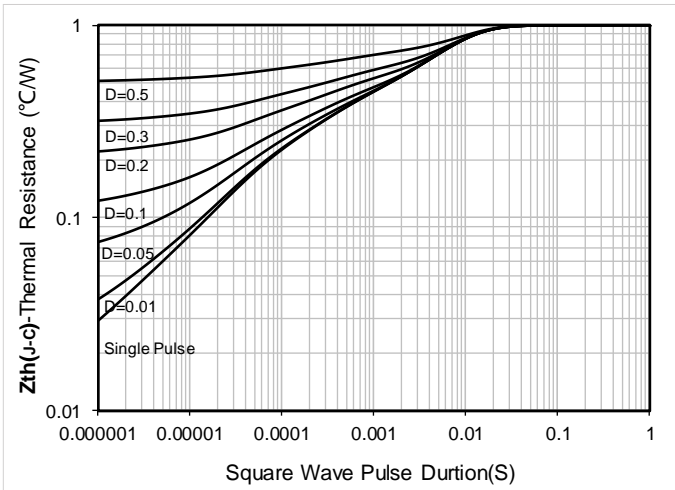


Figure 13. Maximum Transient Thermal Impedance

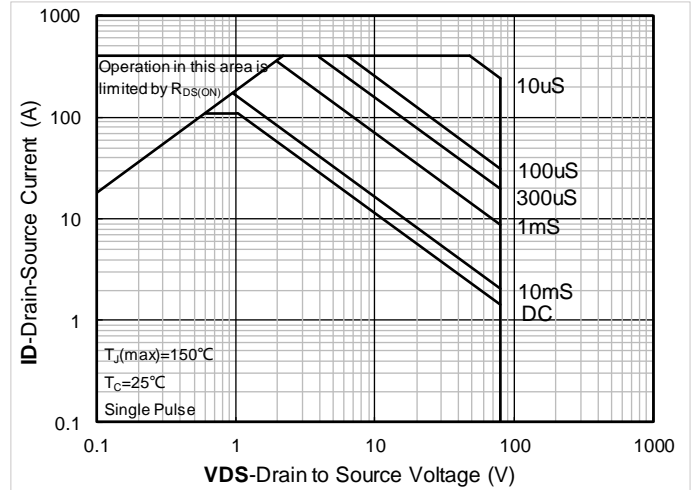


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

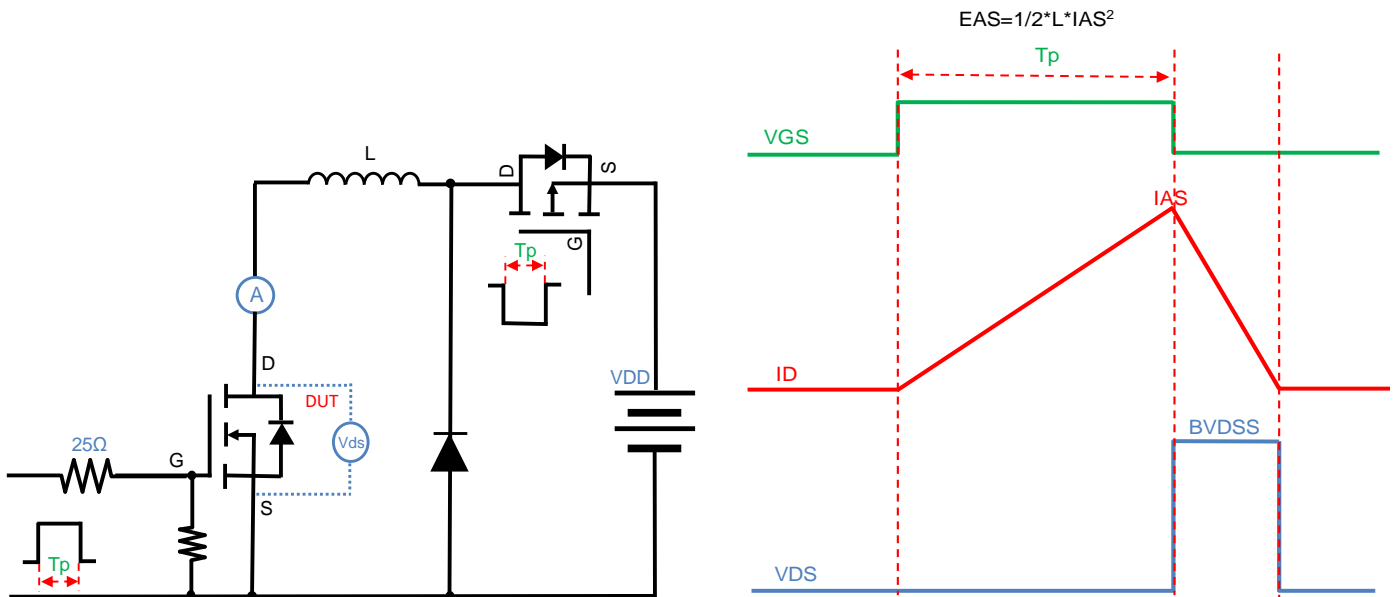


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

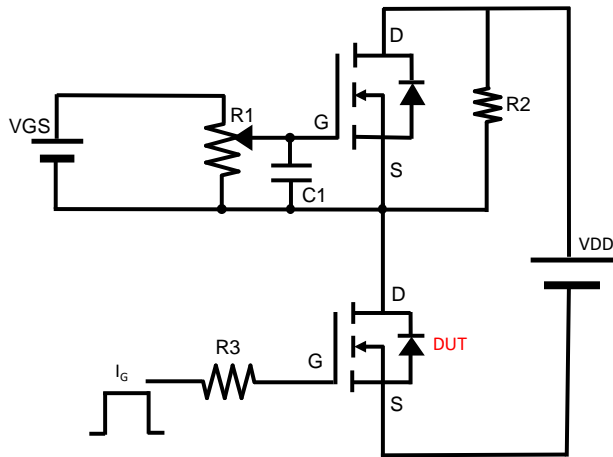


Figure B. Gate Charge Test Circuit & Waveform

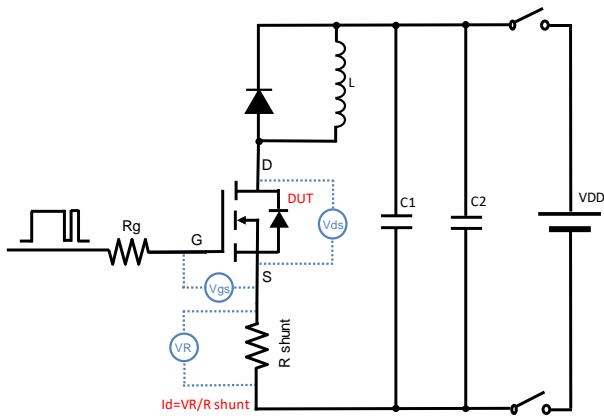


Figure C. Resistive Switching Test Circuit & Waveform

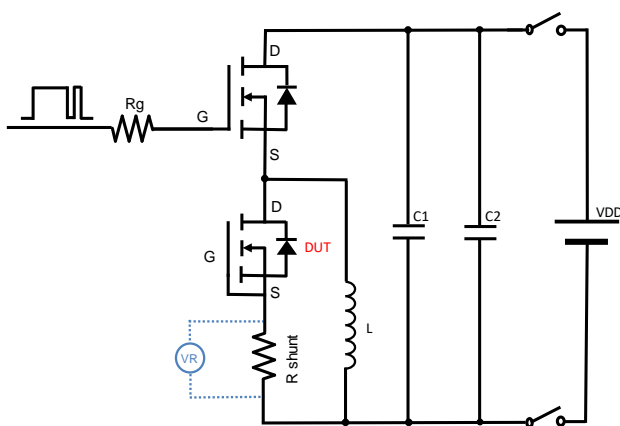
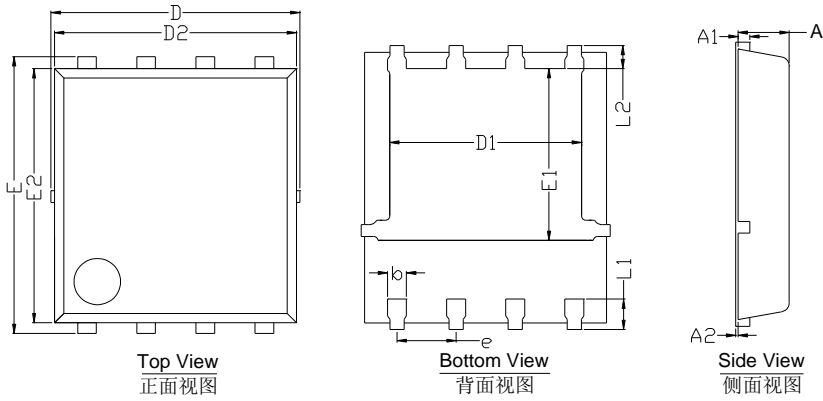


Figure D. Diode Recovery Test Circuit & Waveform

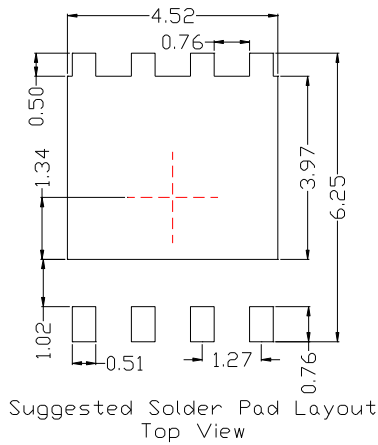


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■ PDFN5060-8L-D-0.95MM Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.05	6.15
A	0.85	0.95	1.00
A1	0.203 BSC		
A2			0.08
D1	4.25	4.35	4.45
E1	3.525	3.625	3.725
D2		5.20	
E2		5.55	
L1	0.45	0.55	0.65
L2	0.68 BSC		
b	0.3	0.4	0.5
e	1.27 BSC		



Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.10\text{mm}$.
 3. The pad layout is for reference purposes only.



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