

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

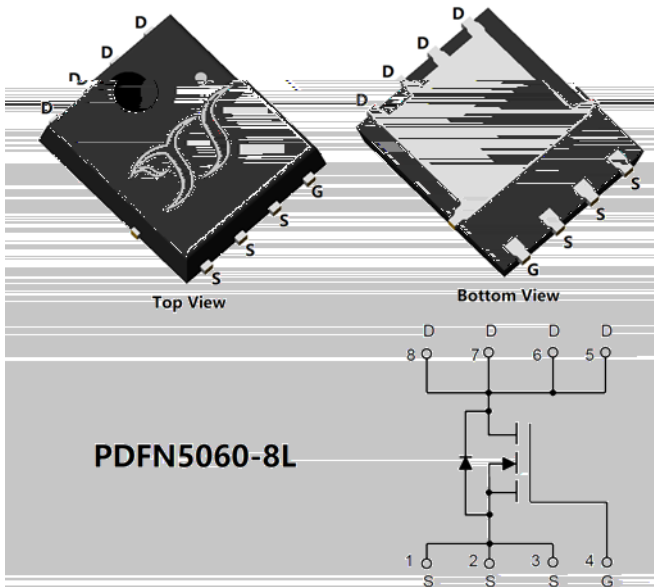
V_{DS}	40 V
I_D	100 A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	<3.5 mohm
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<4.8 mohm
100% EAS Tested	
100% ∇V_{DS} Tested	

General Description

Trench Power LV MOSFET technology
 Excellent package for heat dissipation
 High density cell design for low $R_{DS(ON)}$
 Moisture Sensitivity Level 1
 Epoxy Meets UL 94 V-0 Flammability Rating
 Halogen Free

Applications

DC-DC Converters
 Power management functions
 Backlighting



Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}	40	V
Gate-source Voltage	V_{GS}	± 20	V
Drain Current	I_D	$T_C=25^\circ C$	100
		$T_C=100^\circ C$	63
Pulsed Drain Current ^A	I_{DM}	360	A
Total Power Dissipation @ $T_C=25^\circ C$ ^B	P_D	83	W
Total Power Dissipation @ $T_C=100^\circ C$ ^B	P_D	30	W
Total Power Dissipation @ $T_A=25^\circ C$ ^C	P_D	6.2	W
Single Pulse Avalanche Energy ^D	E_{AS}	400	mJ
Thermal Resistance Junction-to-Case	R_{JC}	1.67	$^\circ C/W$
Thermal Resistance Junction-to-Ambient	R_{JA}	20	$^\circ C/W$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ C$

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG100N04A	F1	YJG100N04A	5000	10000	100000	13 reel



YJG100N04A

Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250 ,	40			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	,
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250 ,	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =20A		2.8	3.5	m
		V _{GS} = 4.5V, I _D =20A		4.0	4.8	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V		0.80	1.2	V
Maximum Body-Diode Continuous Current	I _S				100	A
Gate resistance	R _g	f=1 MHz		3.5		Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V, f=1MHZ		4645		pF
Output Capacitance	C _{oss}			436		
Reverse Transfer Capacitance	C _{rss}			360		
Switching Parameters						
Total Gate Charge	Q _g (10V)	V _{GS} =10V, V _{DS} =20V, I _D =20A		102		nC
Total Gate Charge	Q _g (4.5V)			49		
Gate-Source Charge	Q _{gs}			15.8		
Gate-Drain Charge	Q _{gd}			21.9		
Reverse Recovery Charge	Q _{rr}	I _r =20A, di/dt=100A/us		7.4		
Reverse Recovery Time	t _{rr}			22.3		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =20V , I _D =20A R _{GEN} =3		12		ns
Turn-on Rise Time	t _r			54		
Turn-off Delay Time	t _{D(off)}			120		
Turn-off fall Time	t _f			80		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. The value of R_{JA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.

D. T_J=25°C, V_{DD}=40V, V_G=10V, L=2mH.

■ Typical Performance Characteristics

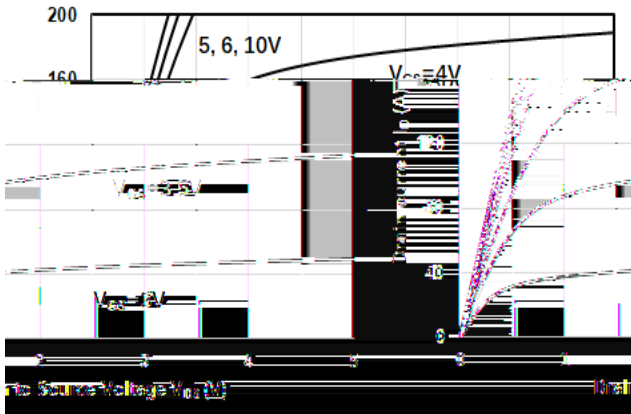


Figure1. Output Characteristics

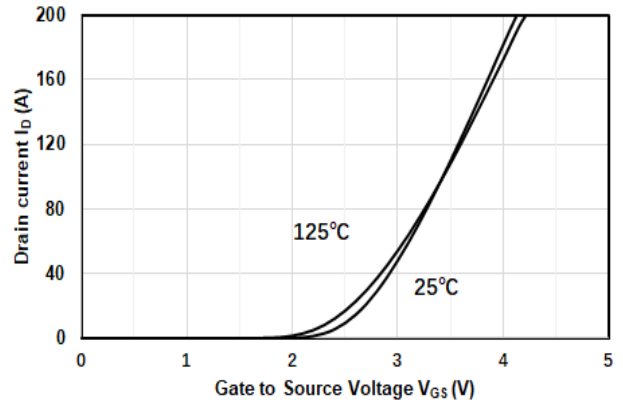


Figure2. Transfer Characteristics

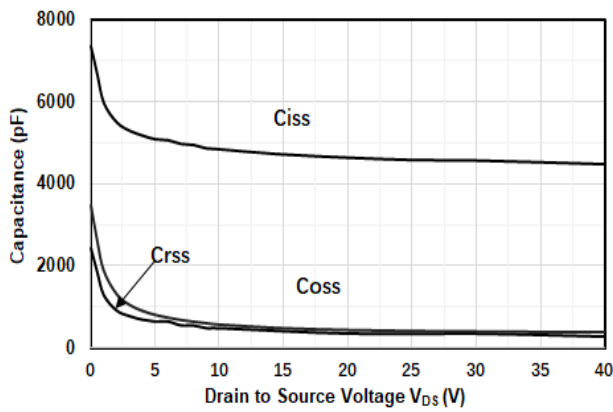


Figure3. Capacitance Characteristics

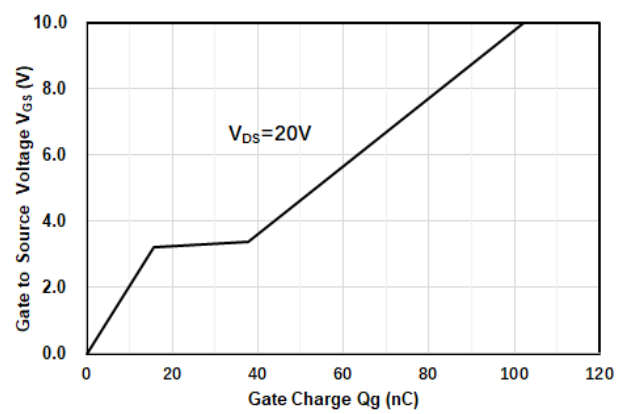


Figure4. Gate Charge

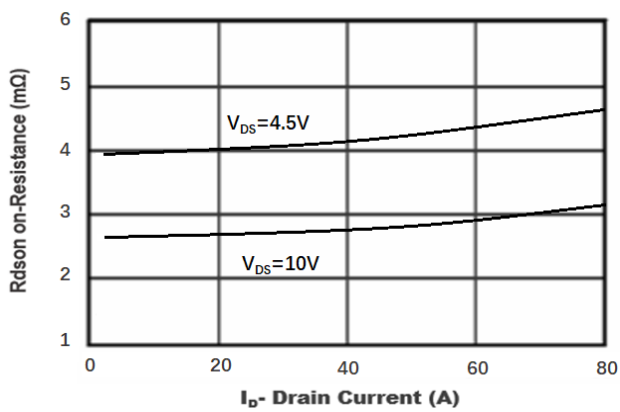


Figure5. Drain-Source on Resistance

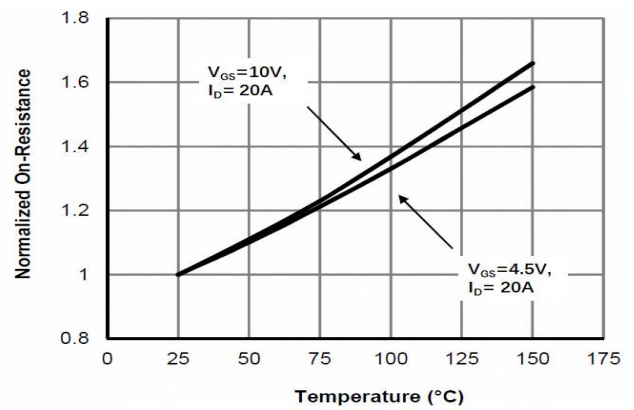


Figure6. Drain-Source on Resistance



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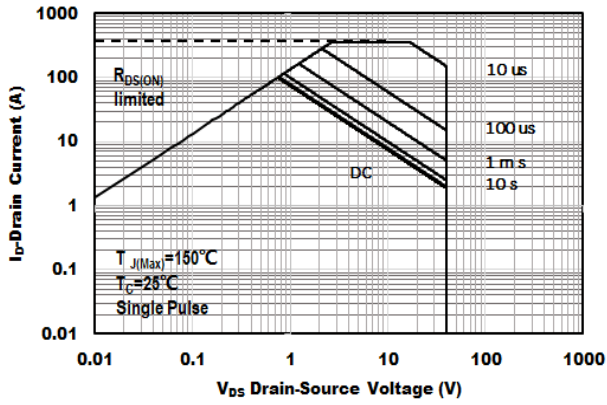


Figure7. Safe Operation Area

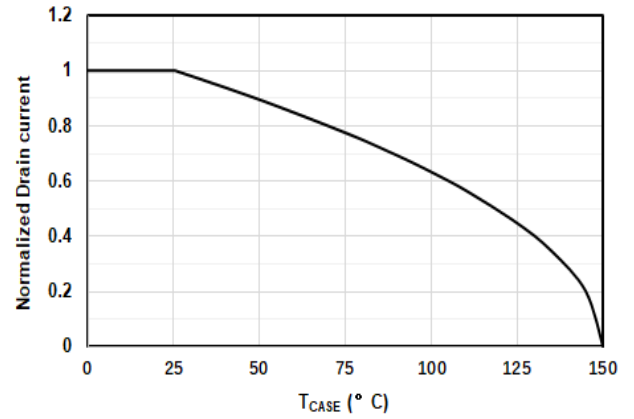


Figure8. Drain current vs. Case Temperature

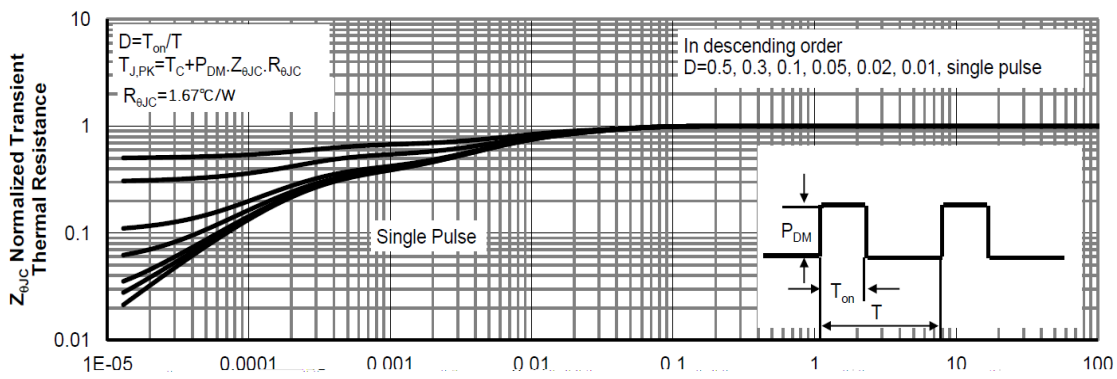
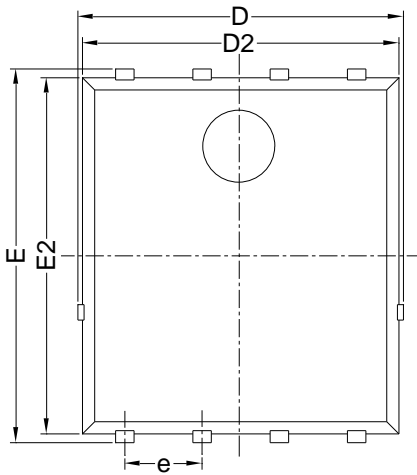


Figure9. Normalized Maximum Transient Thermal Impedance

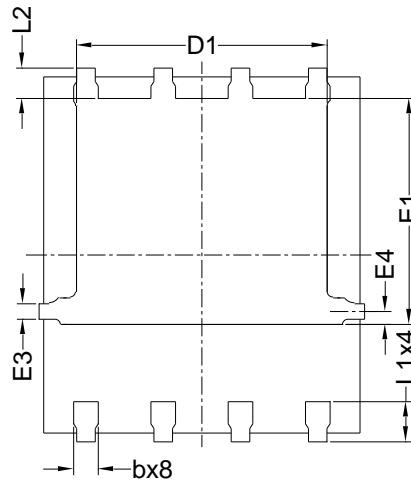


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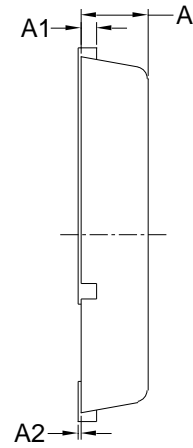
PDFN5060-8L-B-1.1MM Package information



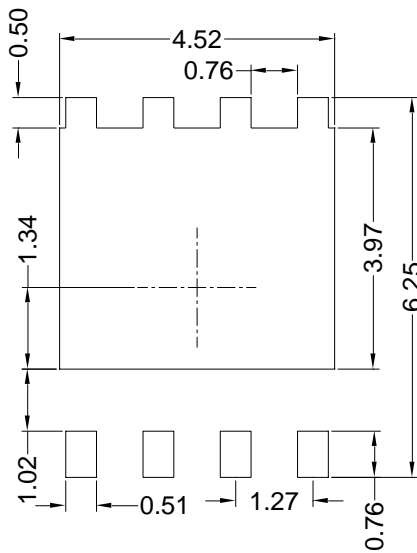
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



YJG100N04A

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