



## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

- $V_{DS}$  30V
- $I_D$  50A
- $R_{DS(ON)}$ ( at  $V_{GS}=10V$ )  $<9m\Omega$
- $R_{DS(ON)}$ ( at  $V_{GS}=4.5V$ )  $<10m\Omega$
- 100% EAS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Trench Power LV MOSFET technology
- Extremely low switching loss
- Excellent stability and uniformity
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- Power management
- Portable equipment

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	30	V
Gate-source Voltage		$V_{GS}$	$\pm 12$	V
Drain Current	$T_A=25^\circ C$	$I_D$	11	A
	$T_A=100^\circ C$		7	
	$T_C=25^\circ C$		50	
	$T_C=100^\circ C$		31	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	120	A
Avalanche energy <sup>B</sup>		EAS	49	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ C$	$P_D$	2.5	W
	$T_A=100^\circ C$		1	
	$T_C=25^\circ C$		104	

$T_C$



# YJD50N03B

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	-	-	1	μA
		V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	-	-	100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.55	0.75	1	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =25A	-	7	9	mΩ
		V <sub>GS</sub> =10V, I <sub>D</sub> =15A	-	7	9	
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	-	7.5	10	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =25A, V <sub>GS</sub> =0V	-	0.85	1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz, Open drain	-	3	-	Ω
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	50	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	-	1560	-	pF
Output Capacitance	C <sub>oss</sub>		-	150	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	135	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =25A	-	39	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	4.5	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	7	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =25A, di/dt=100A/us	-	74	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	86	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =15V, I <sub>D</sub> =25A R <sub>GEN</sub> =2.2Ω	-	5.5	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	20	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	31	-	
Turn-off fall Time	t <sub>f</sub>		-	3	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T<sub>J</sub>=25°C, V<sub>DD</sub>=25V, V<sub>G</sub>=5V, L=0.5mH, I<sub>AS</sub>=14A.

C. P<sub>d</sub> is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in the still air environment with T<sub>A</sub>=25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



Typical Electrical and Thermal Characteristics Diagrams

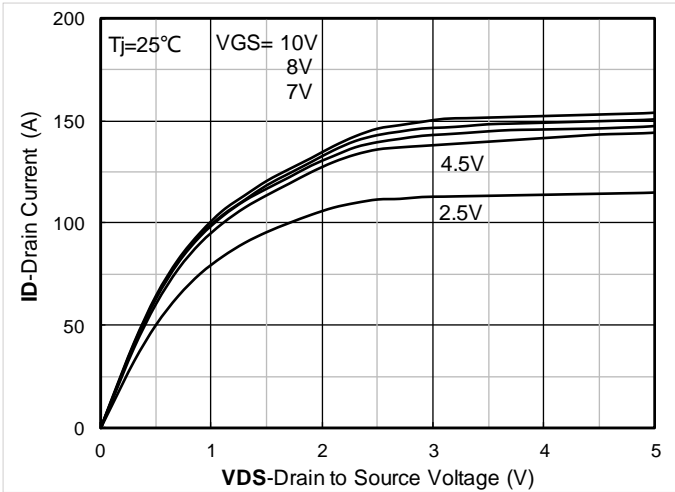


Figure 1. Output Characteristics

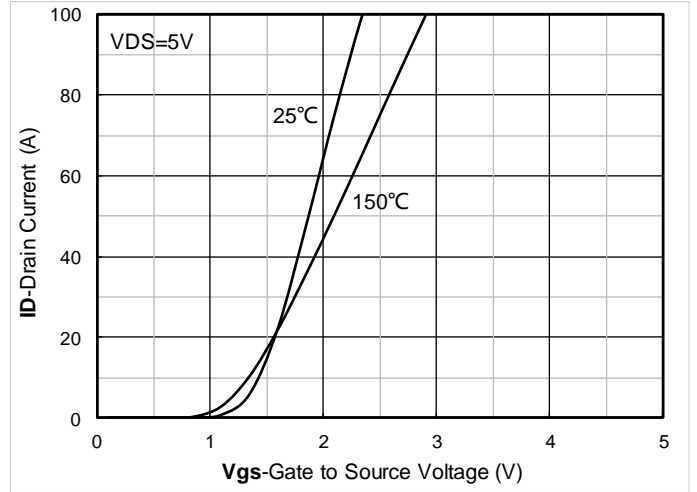


Figure 2. Transfer Characteristics

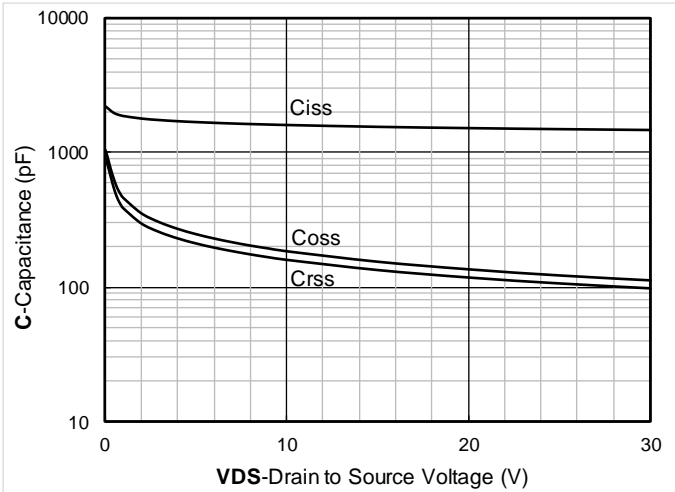


Figure 3. Capacitance Characteristics

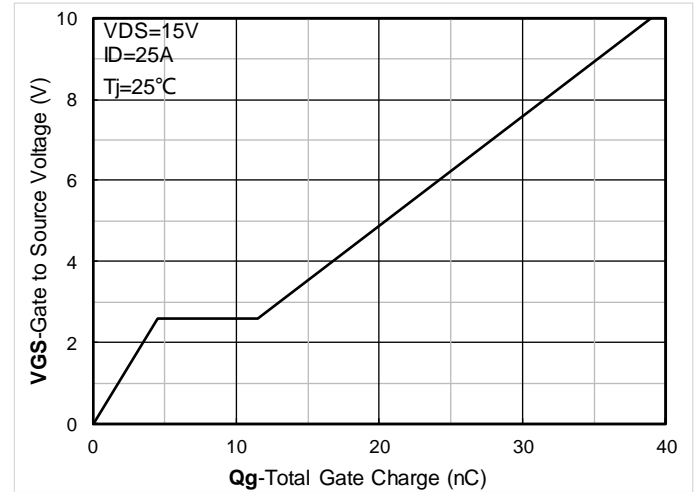


Figure 4. Gate Charge

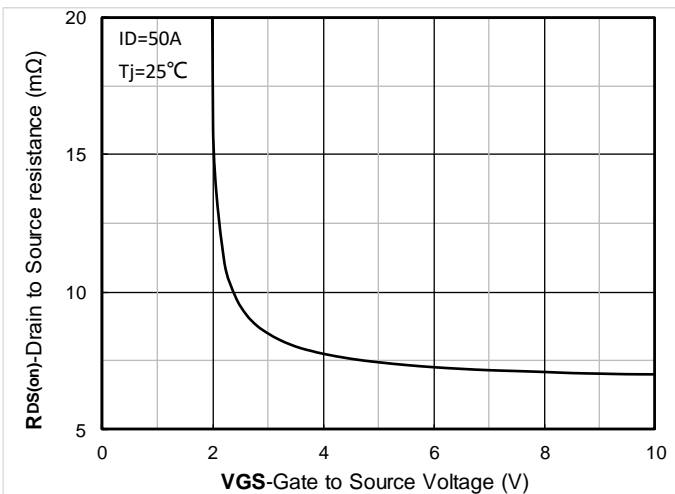


Figure 5. On-Resistance vs Gate to Source Voltage

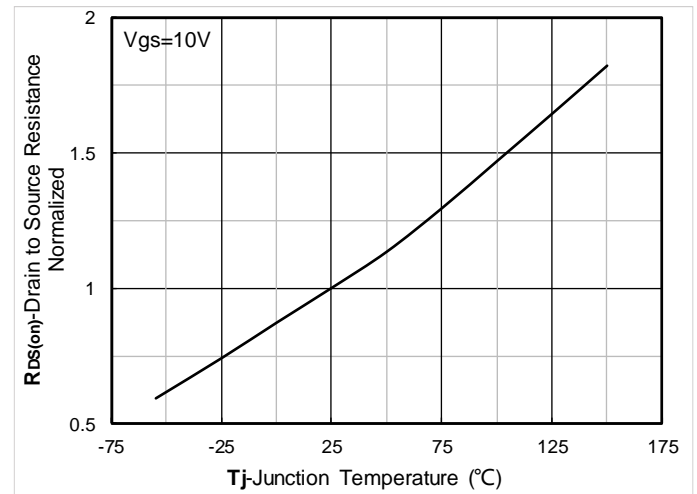


Figure 6. Normalized On-Resistance

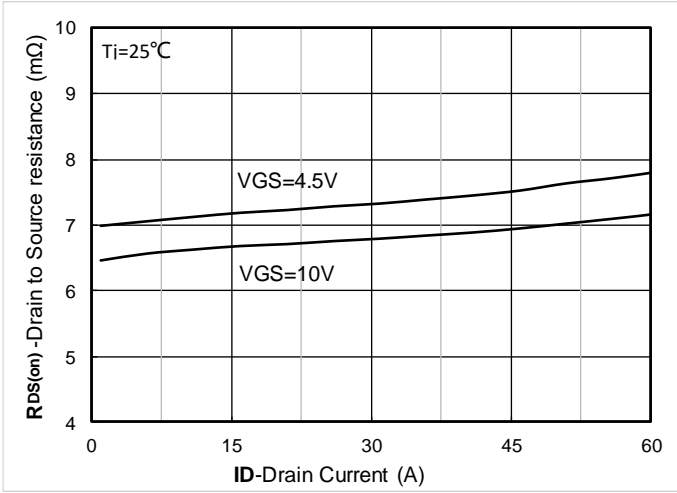


Figure 7.  $R_{DS(on)}$  VS Drain Current

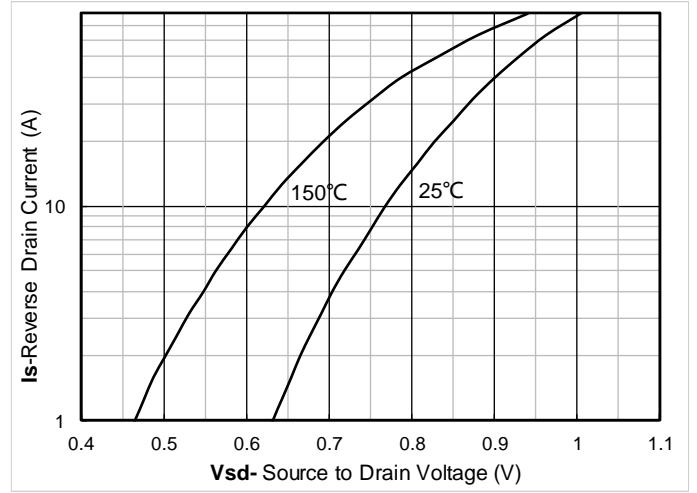


Figure 8. Forward characteristics of reverse diode

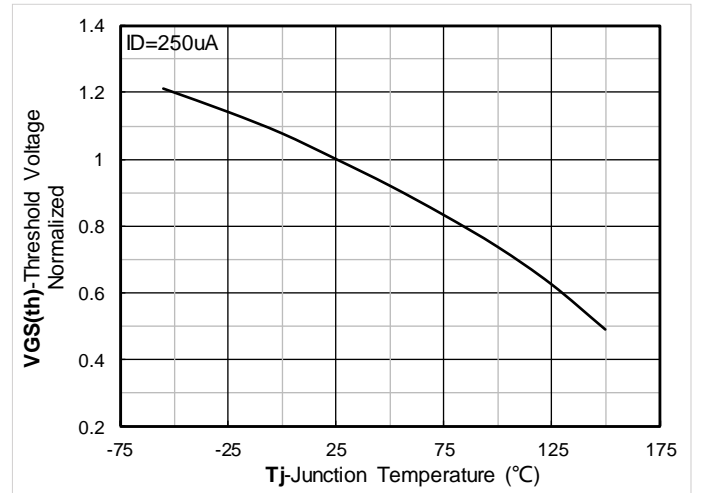


Figure 9. Normalized breakdown voltage

Figure 10. Normalized Threshold voltage

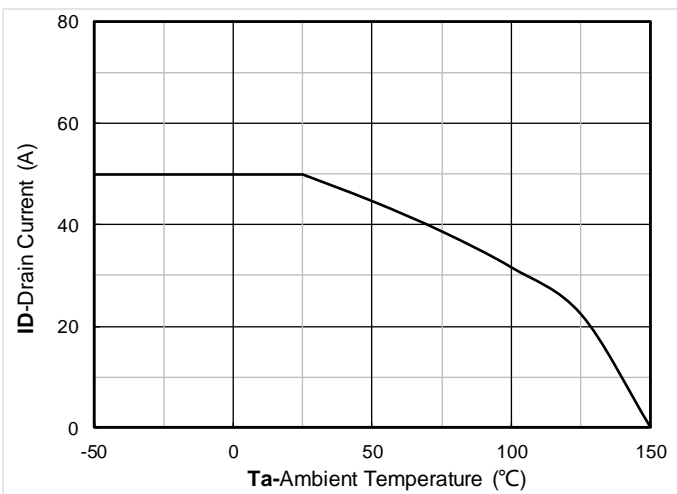


Figure 11. Current dissipation

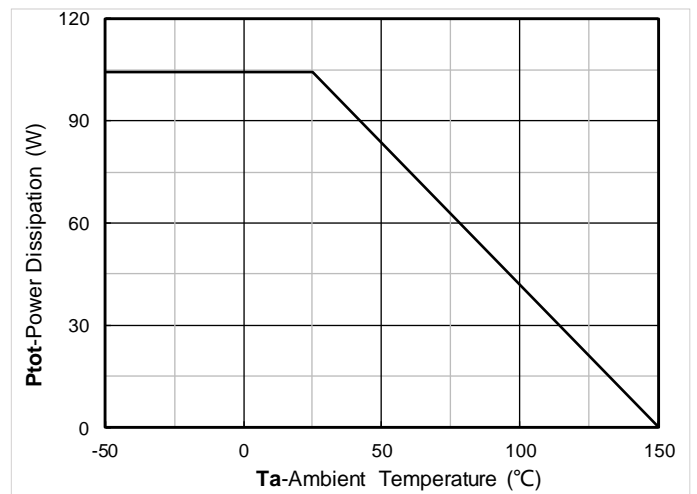


Figure 12. Power dissipation

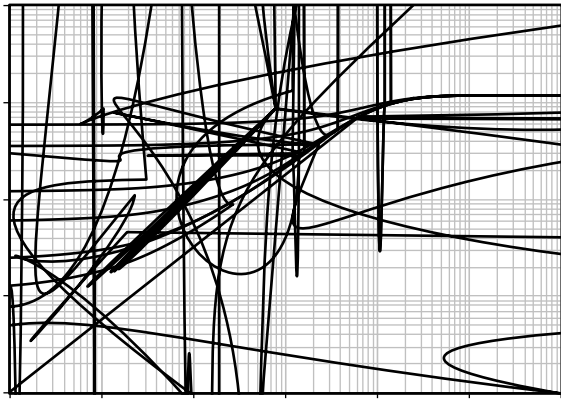


Figure 13. Maximum Transient Thermal Impedance

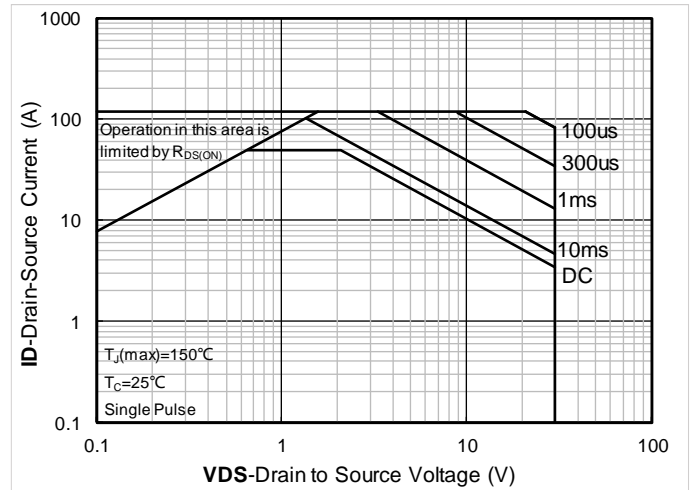


Figure 14. Safe Operation Area

## ■ Test Circuits & Waveforms

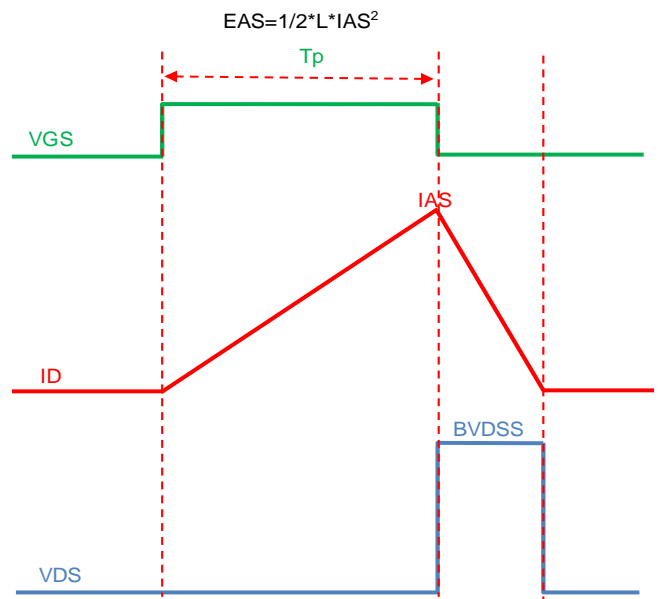
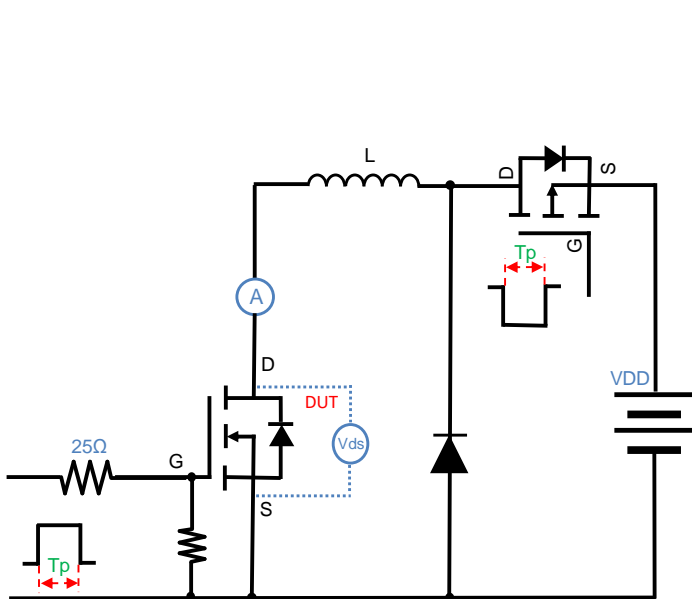


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

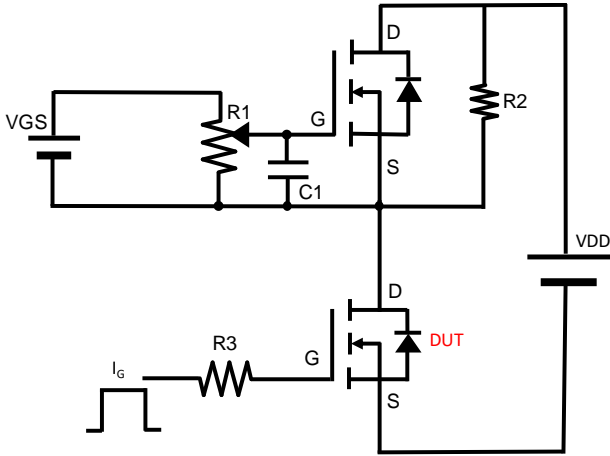


Figure B. Gate Charge Test Circuit & Waveform

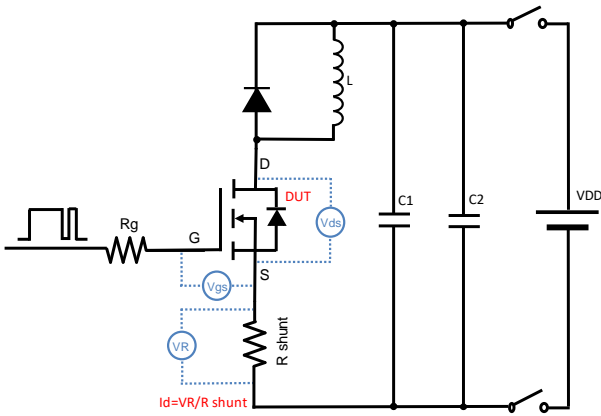


Figure C. Resistive Switching Test Circuit & Waveform

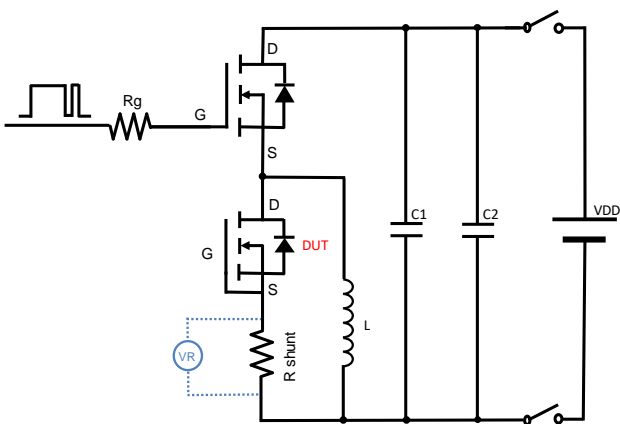
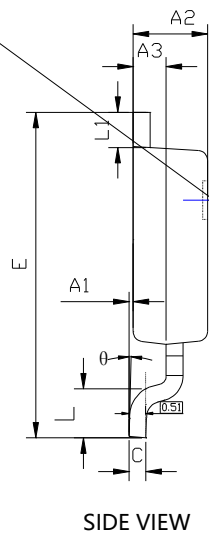
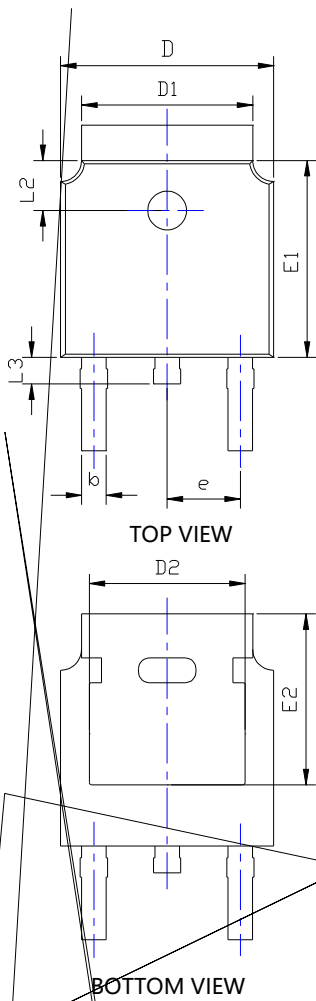


Figure D. Diode Recovery Test Circuit & Waveform



# YJD50N03B

## ■ TO-252-B Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.03					
L2	0.055		0.075	1.400		1.900
L3	0.240	0.310	0.039	0.600		1.000
L4	0.114REF					
θ	0°		10°	0°		10°

NOTE:  
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.  
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



## YJD50N03B

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