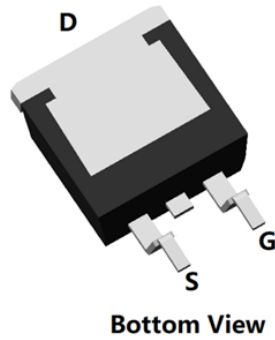
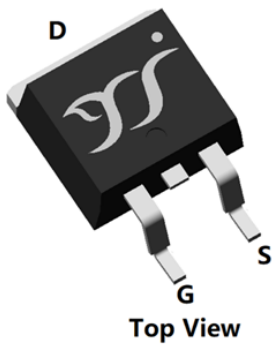
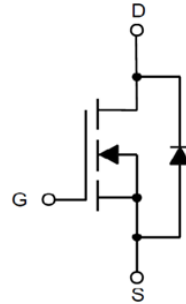


## N-Channel Enhancement Mode Field Effect Transistor



**TO-263**



### Product Summary

$V_{DS}$	60V
$I_D$	200A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	<2.9 mohm
100% EAS Tested	
100% $\nabla V_{DS}$ Tested	

### General Description

Split Gate Trench MOSFET technology  
 Excellent package for heat dissipation  
 High density cell design for low  $R_{DS(ON)}$   
 Moisture Sensitivity Level 1  
 Epoxy Meets UL 94 V-0 Flammability Rating  
 Halogen Free

### Applications

= i h g f i hc ji j j f  
 Isolated DC-DC Converters  
 Motor control  
 Invertors

### Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	60	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current <sup>A</sup>	$T_A=25^\circ C$	$I_D$	25	A
	$T_A=100^\circ C$		15	
	$T_C=25^\circ C$		200	
	$T_C=100^\circ C$		125	
Pulsed Drain Current <sup>B</sup>		$I_{DM}$	600	A
Avalanche energy <sup>C</sup>		EAS	500	mJ
Total Power Dissipation <sup>D</sup>	$T_A=25^\circ C$	$P_D$	4.4	W
	$T_A=100^\circ C$		1.7	
	$T_C=25^\circ C$		260	
	$T_C=100^\circ C$		104	
Thermal Resistance Junction-to-Case		$R_{JC}$	0.48	$^\circ C/W$
Thermal Resistance Junction-to-Ambient <sup>E</sup>		$R_{JA}$	28	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ C$

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJB200G06B	F2	YJB200G06B	800	/	8000	13 reel



# YJB200G06B

## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250 ;	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	;
		V <sub>DS</sub> =60V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C			100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250 ;	2.0	2.8	4.0	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =20A		2.3	2.9	m
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V			1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz	-	2.3	-	
Maximum Body-Diode Continuous Current	I <sub>S</sub>				200	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=100KHZ		4165		pF
Output Capacitance	C <sub>oss</sub>			900		
Reverse Transfer Capacitance	C <sub>rss</sub>			59		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =50A		65		nC
Gate-Source Charge	Q <sub>gs</sub>			11.9		
Gate-Drain Charge	Q <sub>gd</sub>			9.8		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =25A, di/dt=100A/us		63		
Reverse Recovery Time	t <sub>rr</sub>			58		
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =30V, I <sub>D</sub> =25A R <sub>GEN</sub> =2		22.5		ns
Turn-on Rise Time	t <sub>r</sub>			6.7		
Turn-off Delay Time	t <sub>d(off)</sub>			80.3		
Turn-off fall Time	t <sub>f</sub>			26.9		

**Note:**

- The maximum current rating is package limited.
- Repetitive rating; pulse width limited by max. junction temperature.
- V<sub>DD</sub>=50 V, R<sub>G</sub>=25 Ω, L=0.5mH, starting T<sub>J</sub>=25 °C.
- P<sub>D</sub> is based on max. junction temperature, using junction-case thermal resistance.
- The value of R<sub>JA</sub> is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with Ta=25 °C.



## ■ Typical Performance Characteristics

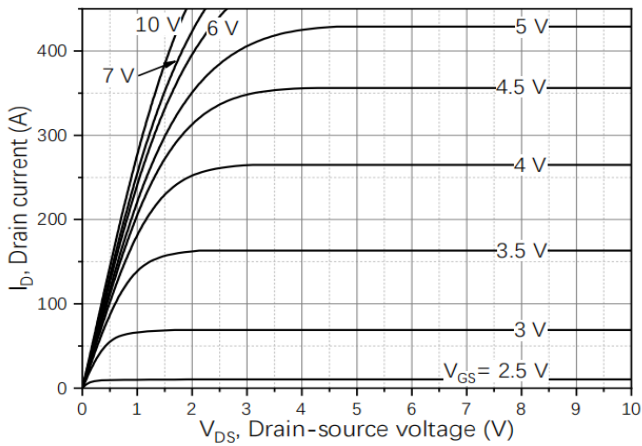


Figure1. Output Characteristics

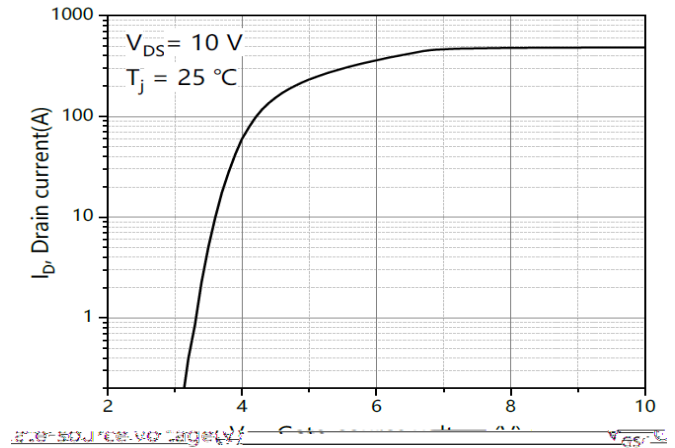


Figure2. Transfer Characteristics

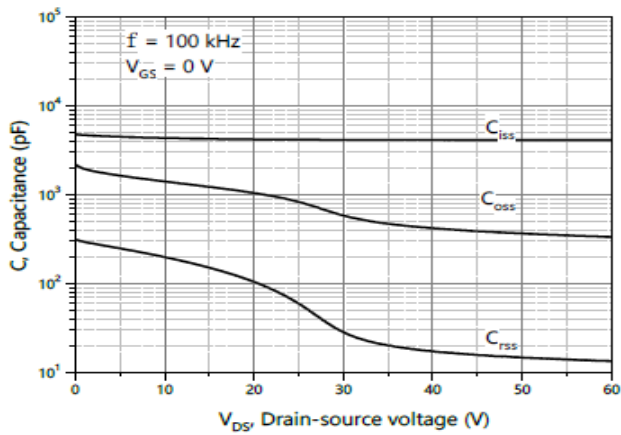


Figure3. Capacitance Characteristics

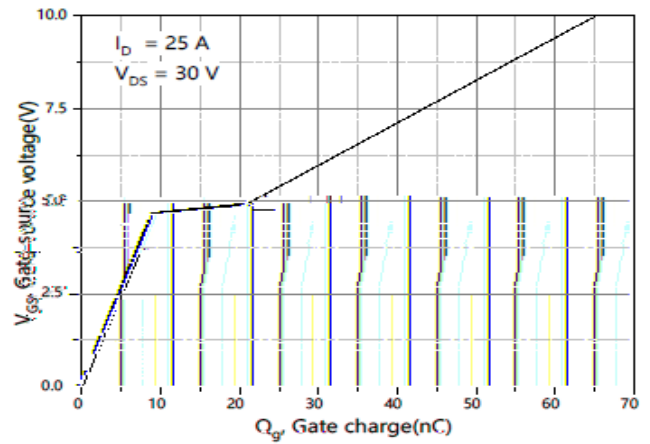


Figure4. Gate Charge

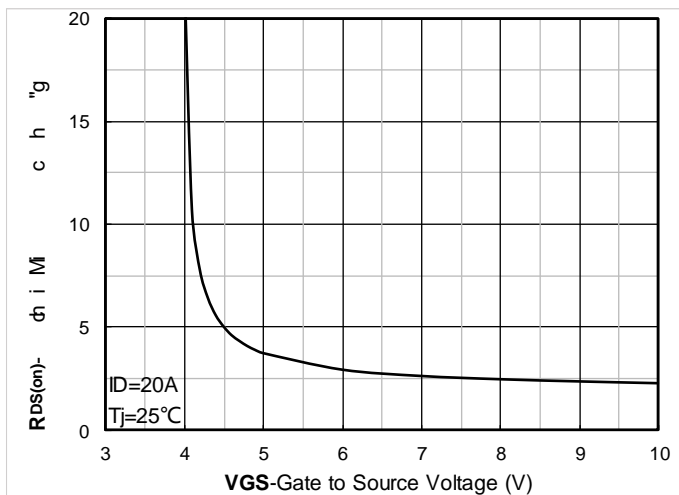


Figure 5. On-Resistance vs Gate to Source Voltage

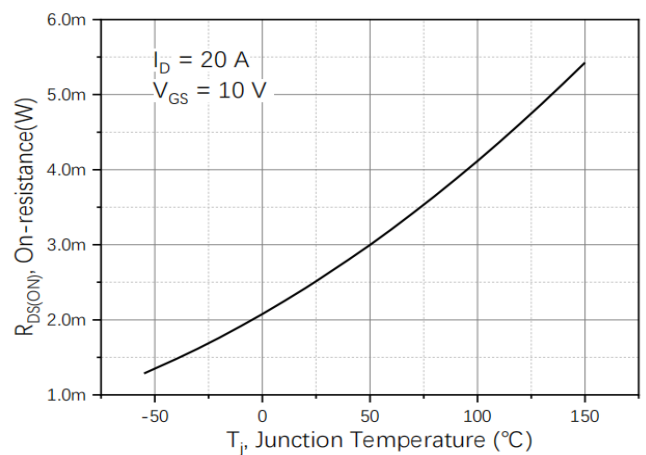


Figure 6. Drain-Source on Resistance



# YJB200G06B

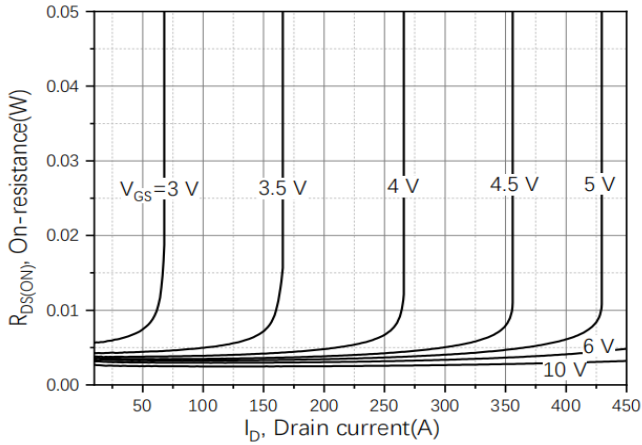


Figure 7. Drain-Source on Resistance

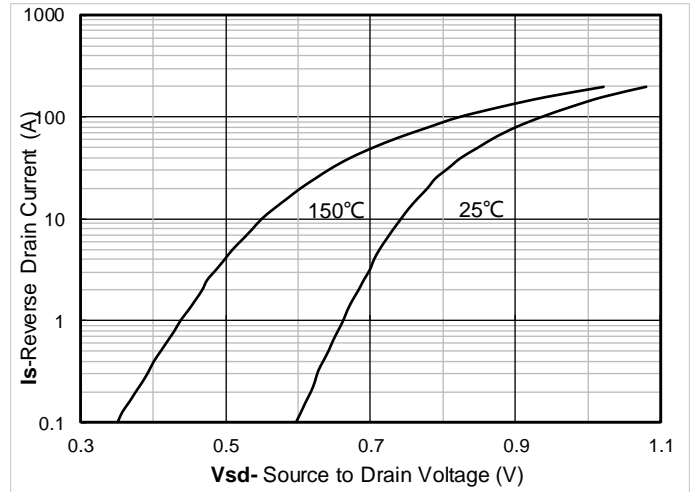


Figure 8. Forward characteristics of reverse diode

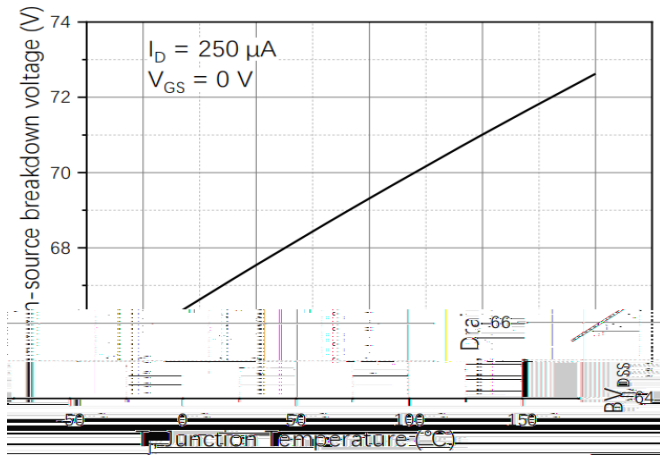


Figure 9. Drain-source breakdown voltage

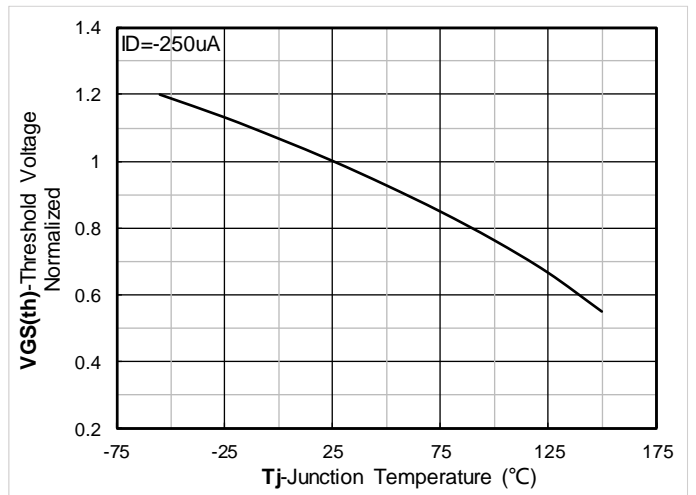


Figure 10. Normalized Threshold voltage

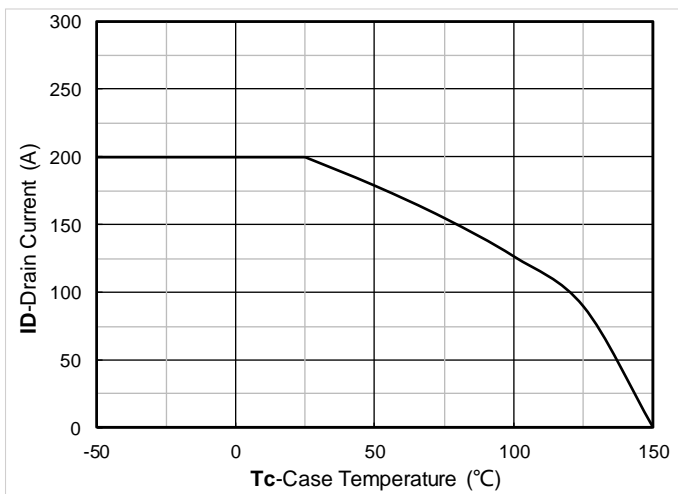


Figure 11. Current dissipation

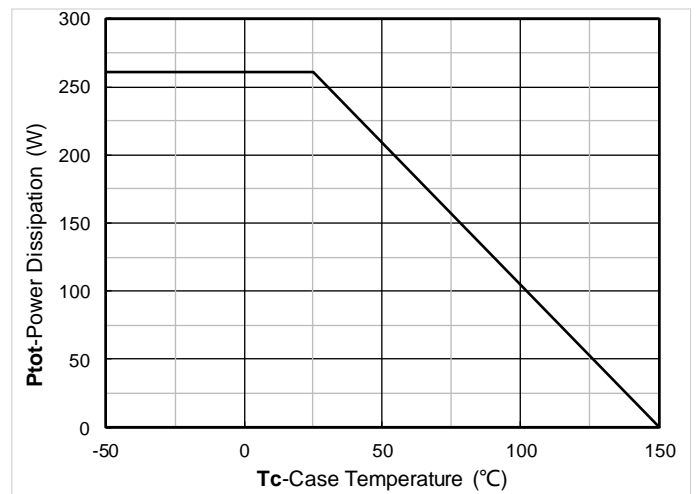


Figure 12. Power dissipation

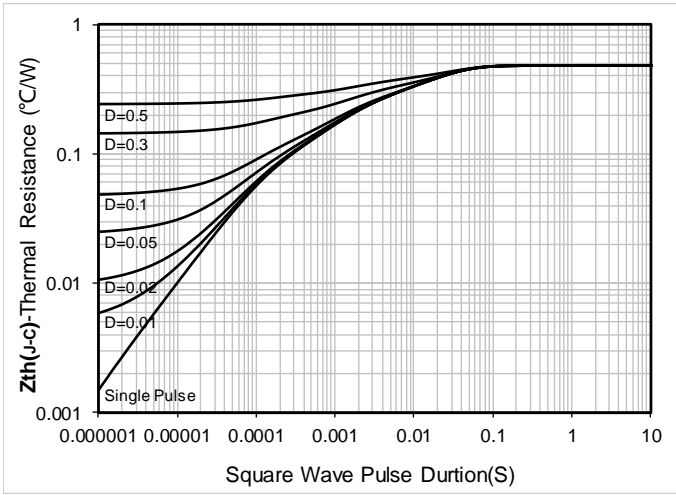


Figure 13. Maximum Transient Thermal Impedance

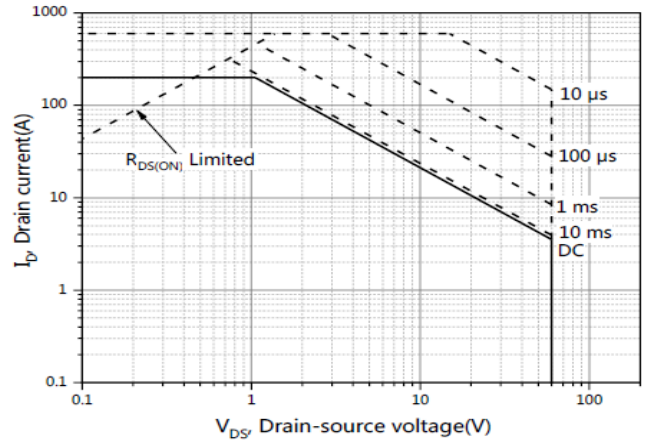


Figure 14. Safe Operation Area

## ■ Test circuits and waveforms

Figure A: Gate Charge Test Circuit & Waveforms

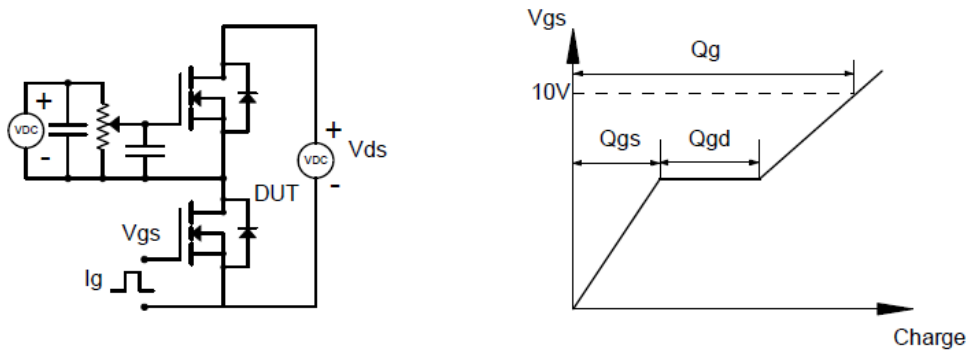


Figure B: Resistive Switching Test Circuit & Waveforms

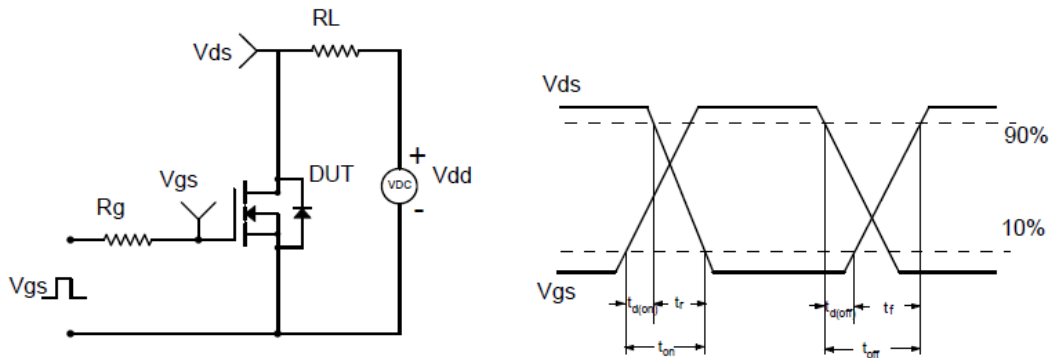


Figure C: Unclamped Inductive Switching (UIS) Test

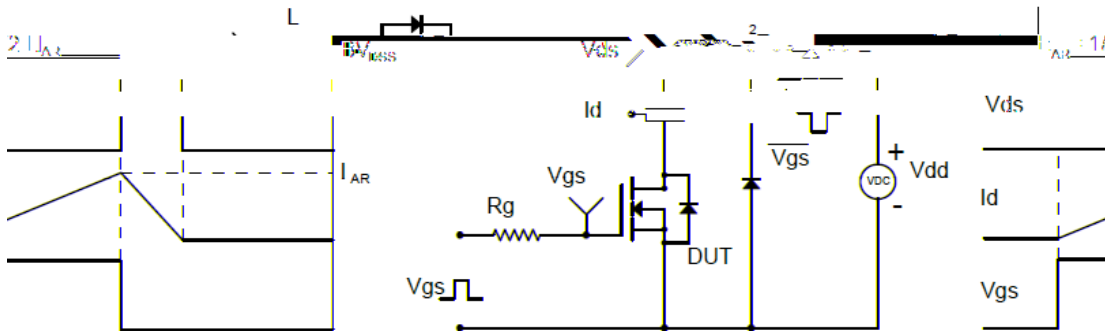
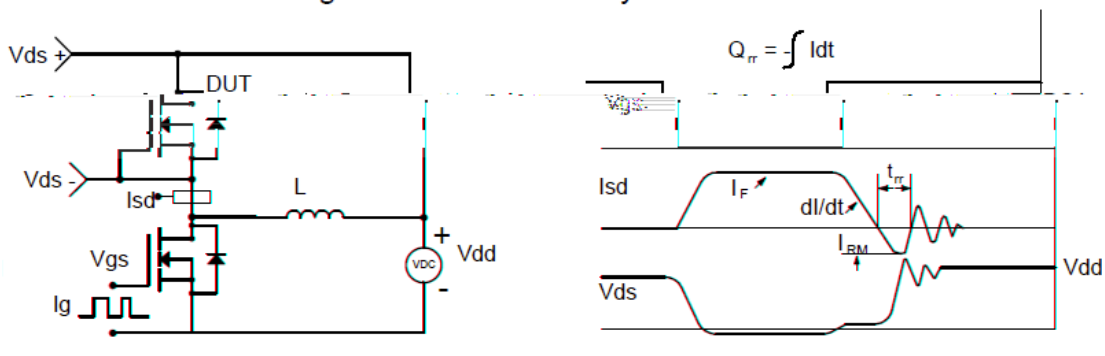


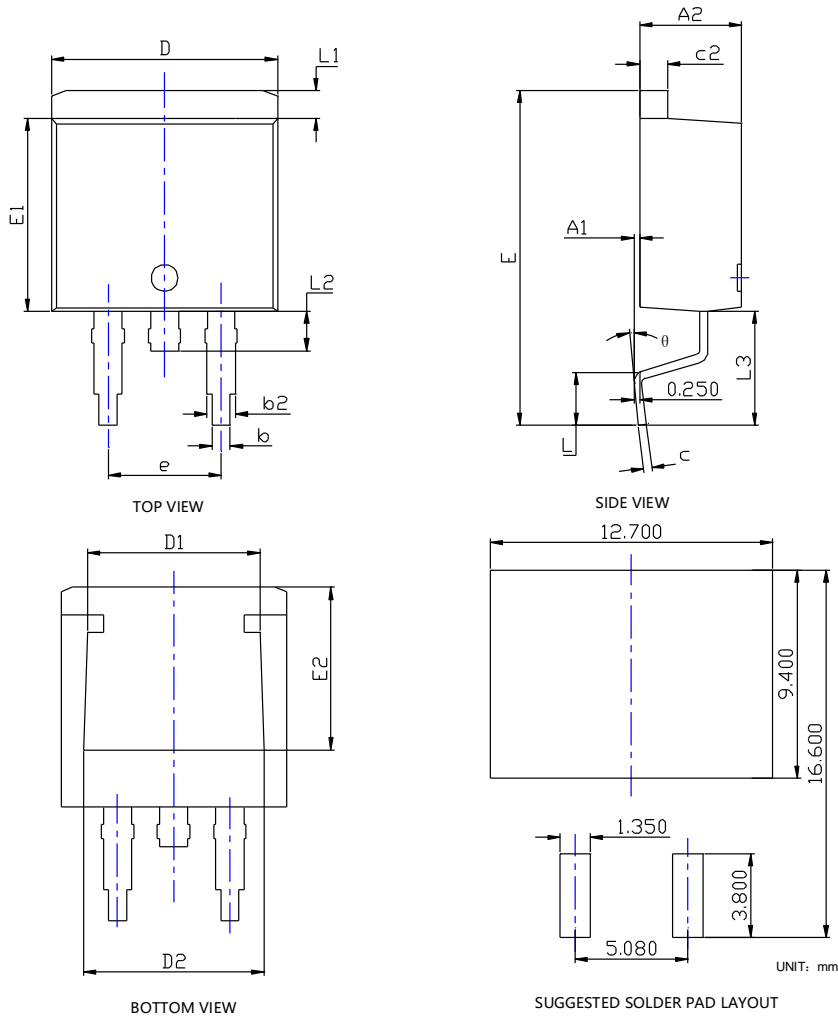
Figure D: Diode Recovery Test Circuit & Waveforms





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## TO-263-HY Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A1	0.000	---	0.010	0.000	---	0.250
A2	0.174	0.180	0.186	4.430	4.580	4.730
b	0.028	0.032	0.036	0.720	0.820	0.920
b2	0.046	0.050	0.054	1.180	1.280	1.380
c	0.013	0.015	0.018	0.330	0.390	0.450
c2	0.048	0.050	0.053	1.220	1.280	1.340
D	0.394	0.400	0.406	10.000	10.150	10.300
D1	0.295	0.307	0.319	7.500	7.800	8.100
D2	0.303	0.315	0.327	7.700	8.000	8.300
E	0.571	0.591	0.610	14.500	15.000	15.500
E1	0.337	0.341	0.348	8.550	8.700	8.850
E2	0.276	0.287	0.299	7.000	7.300	7.600
e	0.200BSC			5.080BSC		
L	0.070	---	0.110	1.790	---	2.790
L1	0.044	---	0.056	1.120	---	1.420
L2	0.030	---	0.070	0.770	---	1.770
L3	0.197REF			5.000REF		
$\theta$	0°	---	8°	0°	---	8°

**NOTE:**

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



## YJB200G06B

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