



# YJB120G08A

## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

$V_{DS}$	80V
$I_D$	120A
$R_{DS(ON)}$ ( at $V_{GS}=10V$ )	<4.5mohm
100% EAS Tested	
100% $\nabla V_{DS}$ Tested	

### General Description

Split gate trench MOSFET technology  
 Excellent package for heat dissipation  
 High density cell design for low  $R_{DS(ON)}$   
 G i c M h c c c F f +  
 j i G OF 3. P-0 Flammability Rating  
 Balogen Free

### Applications

Battery protection  
 Load switch  
 Uninterruptible power supply

### Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	80	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ C$	$I_D$	15	A
	$T_A=100^\circ C$		9.5	
	$T_C=25^\circ C$		120	
	$T_C=100^\circ C$		76	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	480	A
Avalanche energy <sup>B</sup>		$E_{AS}$	506	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ C$	$P_D$	1.72	W
	$T_A=100^\circ C$		0.69	
	$T_C=25^\circ C$		208	
	$T_C=100^\circ C$		83.3	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ C$

### Thermal resistance

Parameter		Symbol	Limit	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	$t \leq 10S$	$R_{\theta J-A}$	14.88	$^\circ C/W$
	Steady-State		72.28	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta J-C}$	0.6	$^\circ C/W$

### Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJB120G08A	F2	YJB120G08A	800	/	8000	13 reel



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## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250 ;	80	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V	-	-	1	;
		V <sub>DS</sub> =80V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C			100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250 ;	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	3.6	4.5	m
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V	-	0.8	1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	120	A
Gate resistance	R <sub>G</sub>	f=1MHz	-	2	-	
Transconductance	G <sub>fs</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =50A		71.5		S
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V, f=1MHZ	-	5666	-	pF
Output Capacitance	C <sub>oss</sub>		-	860	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	7.5	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =40V , V <sub>GS</sub> =10V , I <sub>D</sub> =50A	-	73	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	25	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	12	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =50A , di/dt=100A/us	-	50	-	
Reverse Recovery Time	t <sub>rr</sub>		-	44	-	
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>DS</sub> =40V , V <sub>GS</sub> =10V & L A7- & I <sub>D</sub> =50A	-	27	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	32	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	54	-	
Turn-off fall Time	t <sub>f</sub>		-	17	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T<sub>J</sub>=25°C, V<sub>DD</sub>=50V, V<sub>GS</sub>=10V, L=0.5mH I<sub>as</sub>=45A.

C. P<sub>d</sub> is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R<sub>D</sub> is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25° C.



## ■ Typical Performance Characteristics

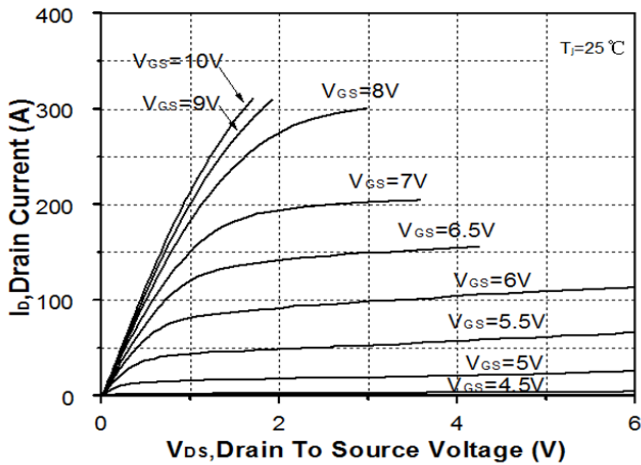


Figure1. Output Characteristics

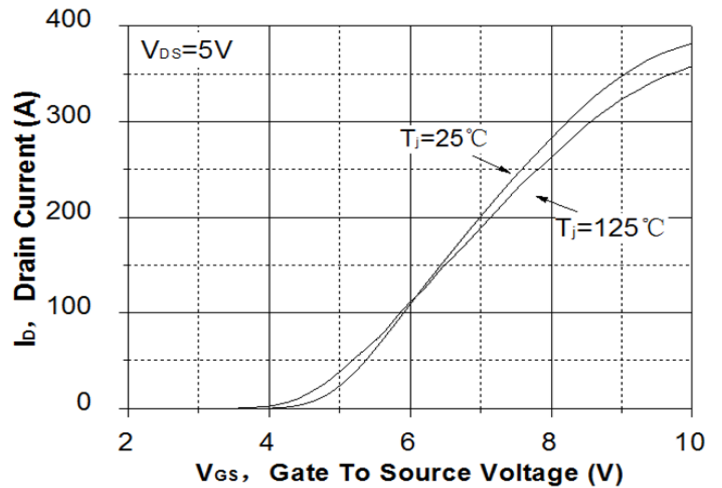


Figure2. Transfer Characteristics

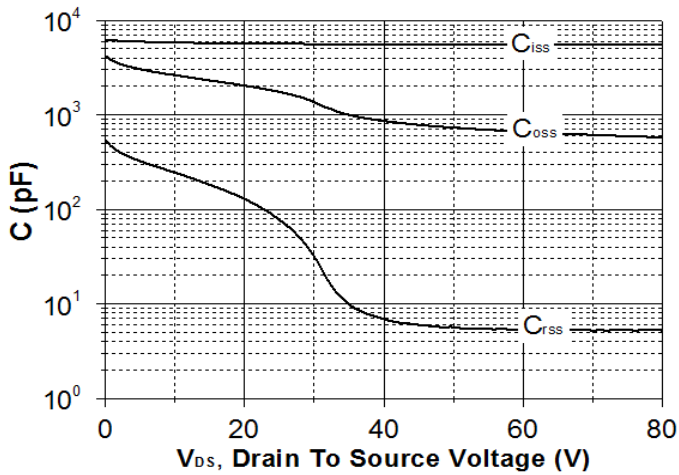


Figure3. Capacitance Characteristics

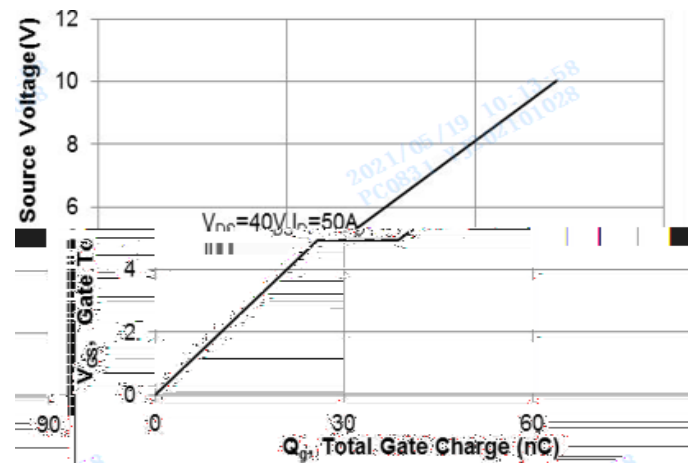


Figure4. Gate Charge

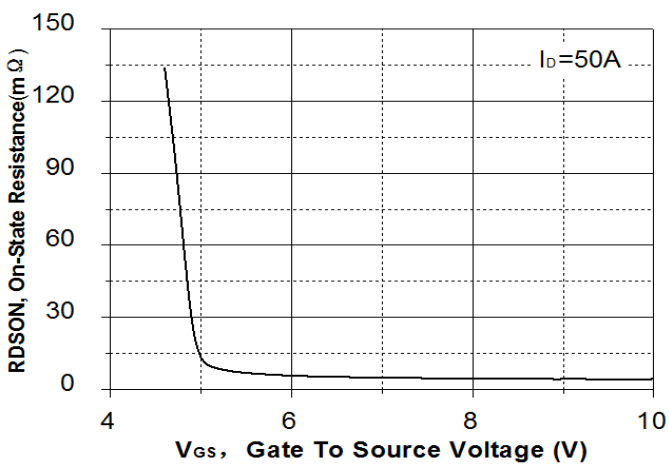


Figure5. On-Resistance vs. Gate to Source Voltage

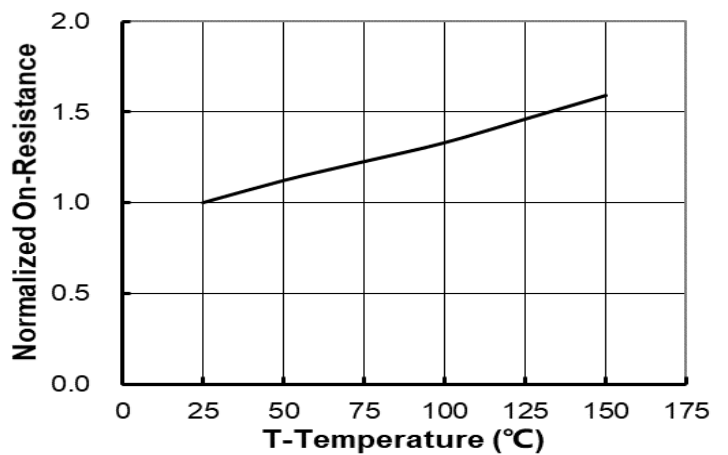


Figure6. Normalized On-Resistance



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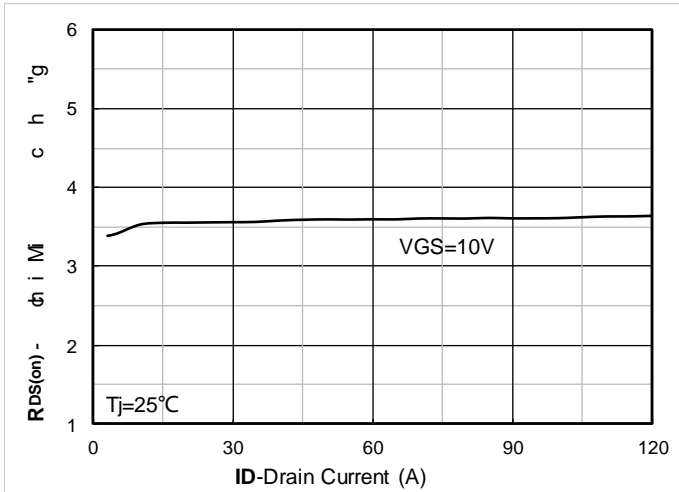


Figure 7. RDS(on) VS Drain Current

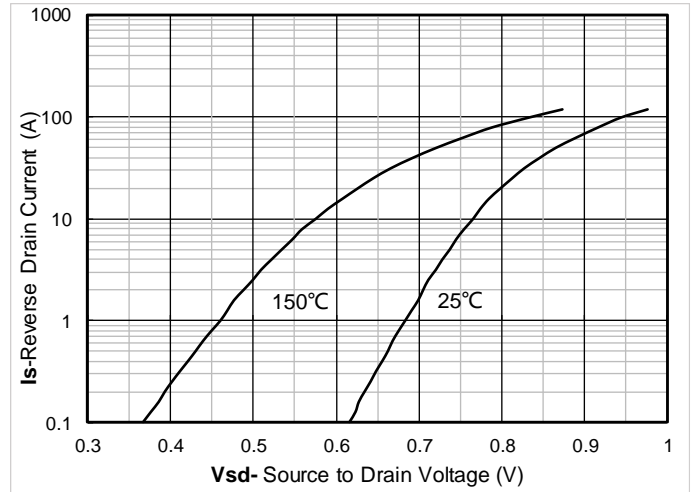


Figure 8. Forward characteristics of reverse diode

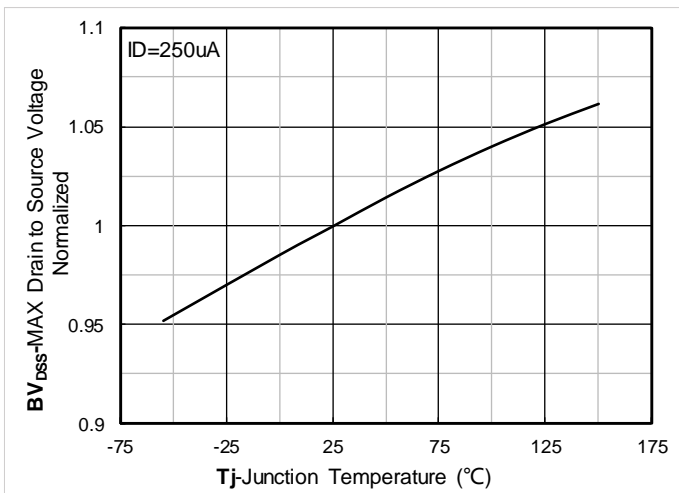


Figure 9. Normalized breakdown voltage

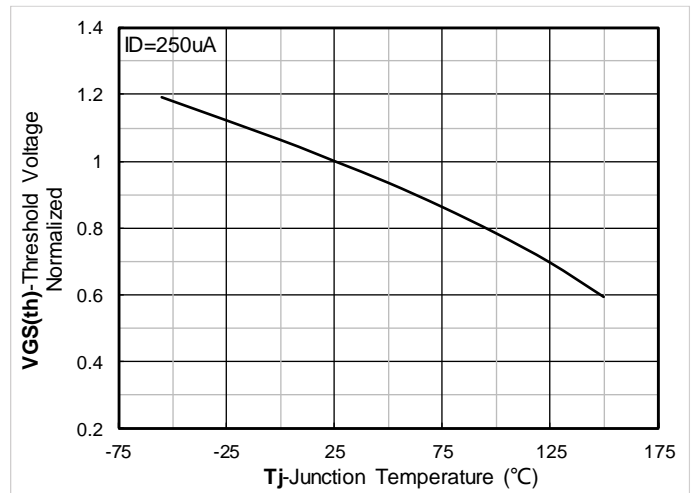


Figure 10. Normalized Threshold voltage

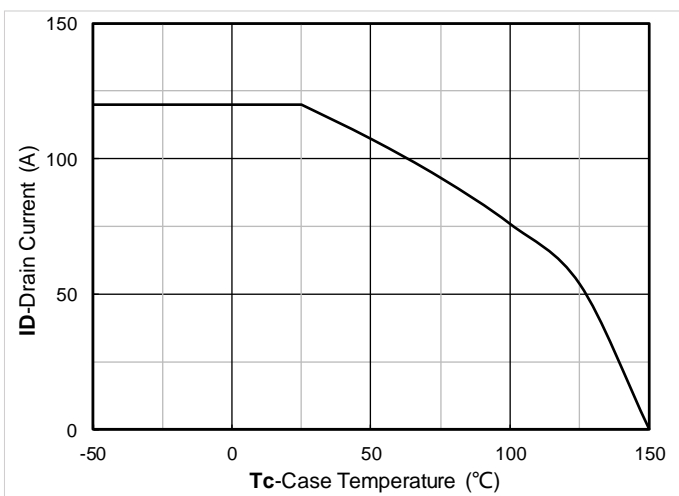


Figure 11. Current dissipation

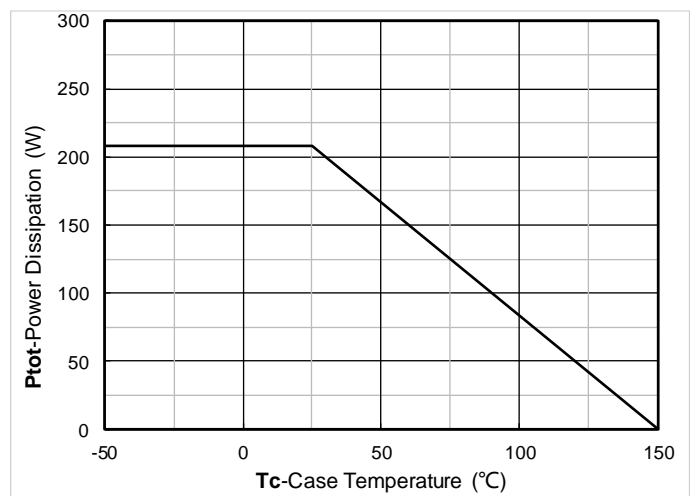


Figure 12. Power dissipation

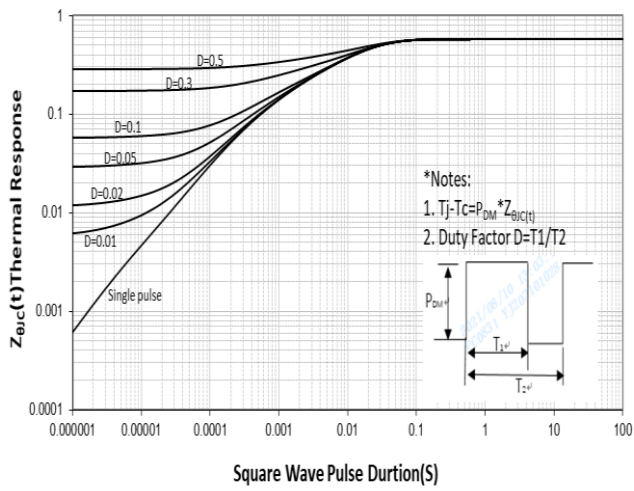


Figure 13. Maximum Transient Thermal Impedance

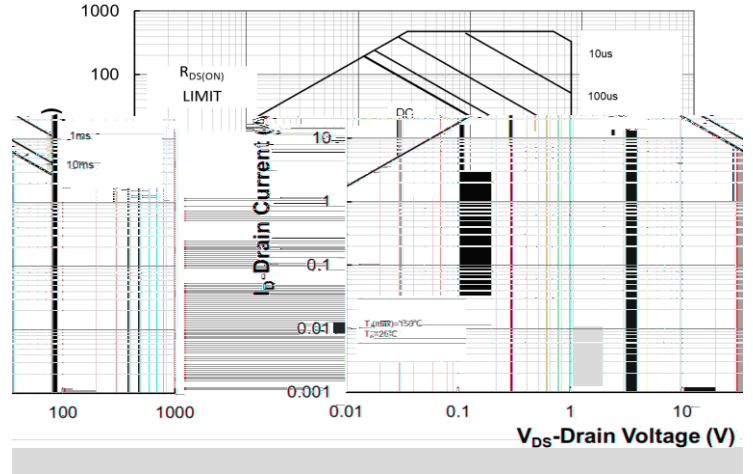
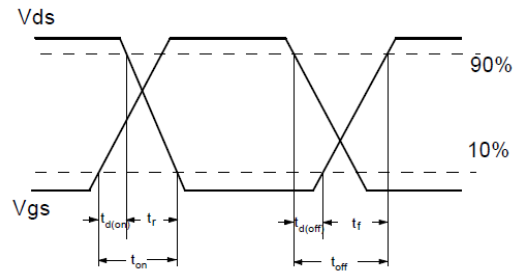
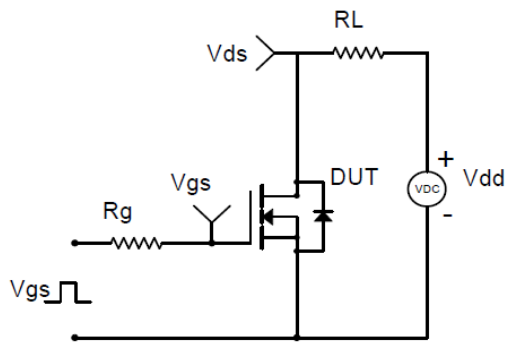
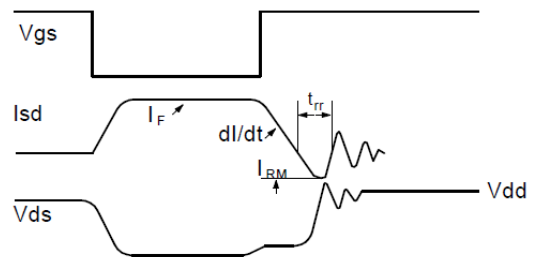
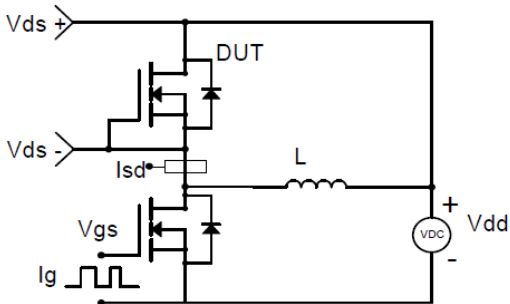


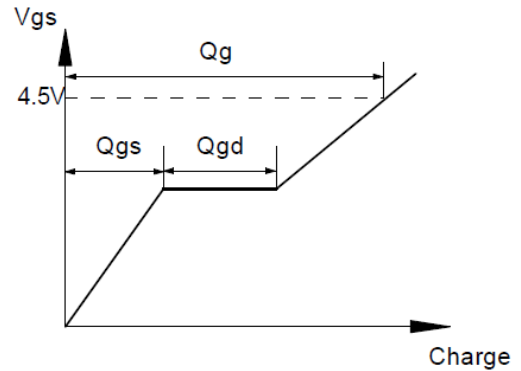
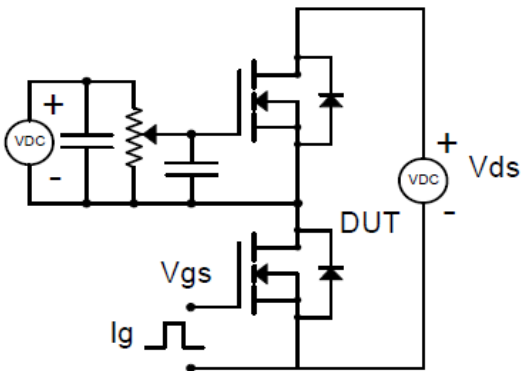
Figure 14. Safe Operation Area



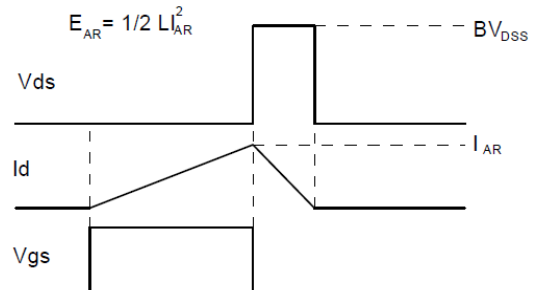
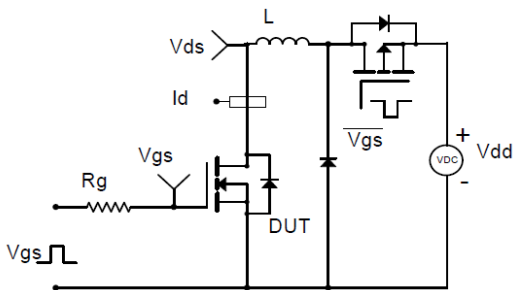
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

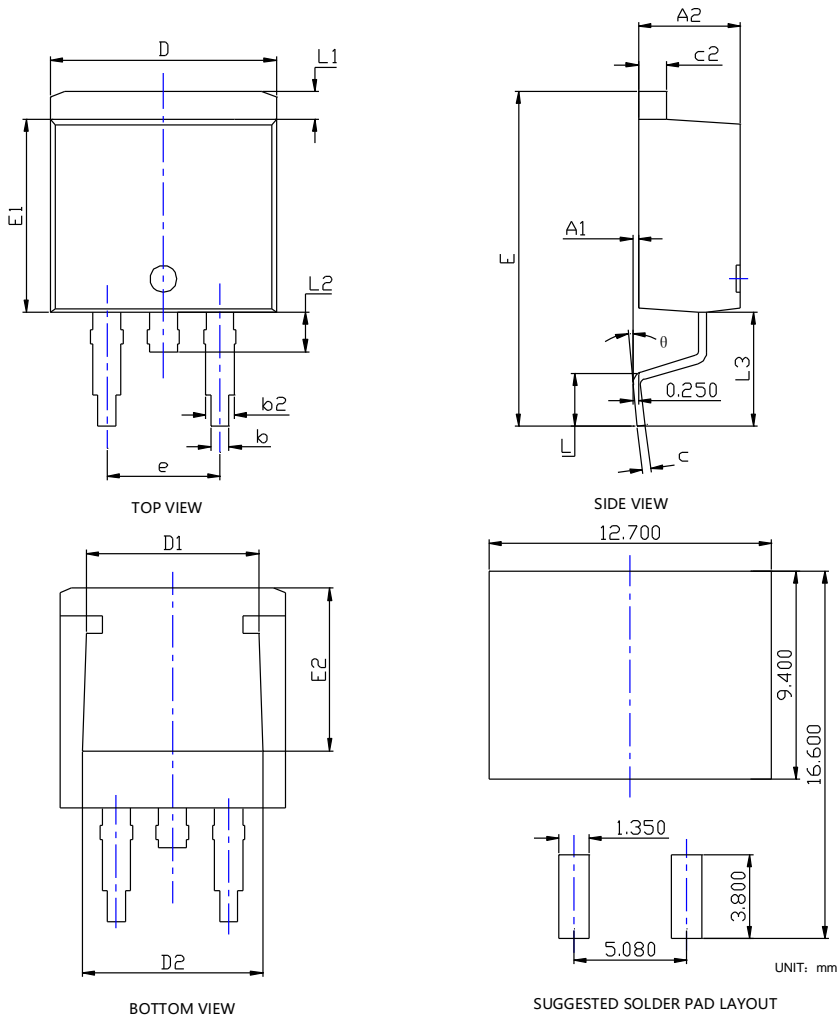


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



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## TO-263-HY Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A1	0.000	---	0.010	0.000	---	0.250
A2	0.174	0.180	0.186	4.430	4.580	4.730
b	0.028	0.032	0.036	0.720	0.820	0.920
b2	0.046	0.050	0.054	1.180	1.280	1.380
c	0.013	0.015	0.018	0.330	0.390	0.450
c2	0.048	0.050	0.053	1.220	1.280	1.340
D	0.394	0.400	0.406	10.000	10.150	10.300
D1	0.295	0.307	0.319	7.500	7.800	8.100
D2	0.303	0.315	0.327	7.700	8.000	8.300
E	0.571	0.591	0.610	14.500	15.000	15.500
E1	0.337	0.341	0.348	8.550	8.700	8.850
E2	0.276	0.287	0.299	7.000	7.300	7.600
e	0.200BSC			5.080BSC		
L	0.070	---	0.110	1.790	---	2.790
L1	0.044	---	0.056	1.120	---	1.420
L2	0.030	---	0.070	0.770	---	1.770
L3	0.197REF			5.000REF		
θ	0°	---	8°	0°	---	8°

**NOTE:**

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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